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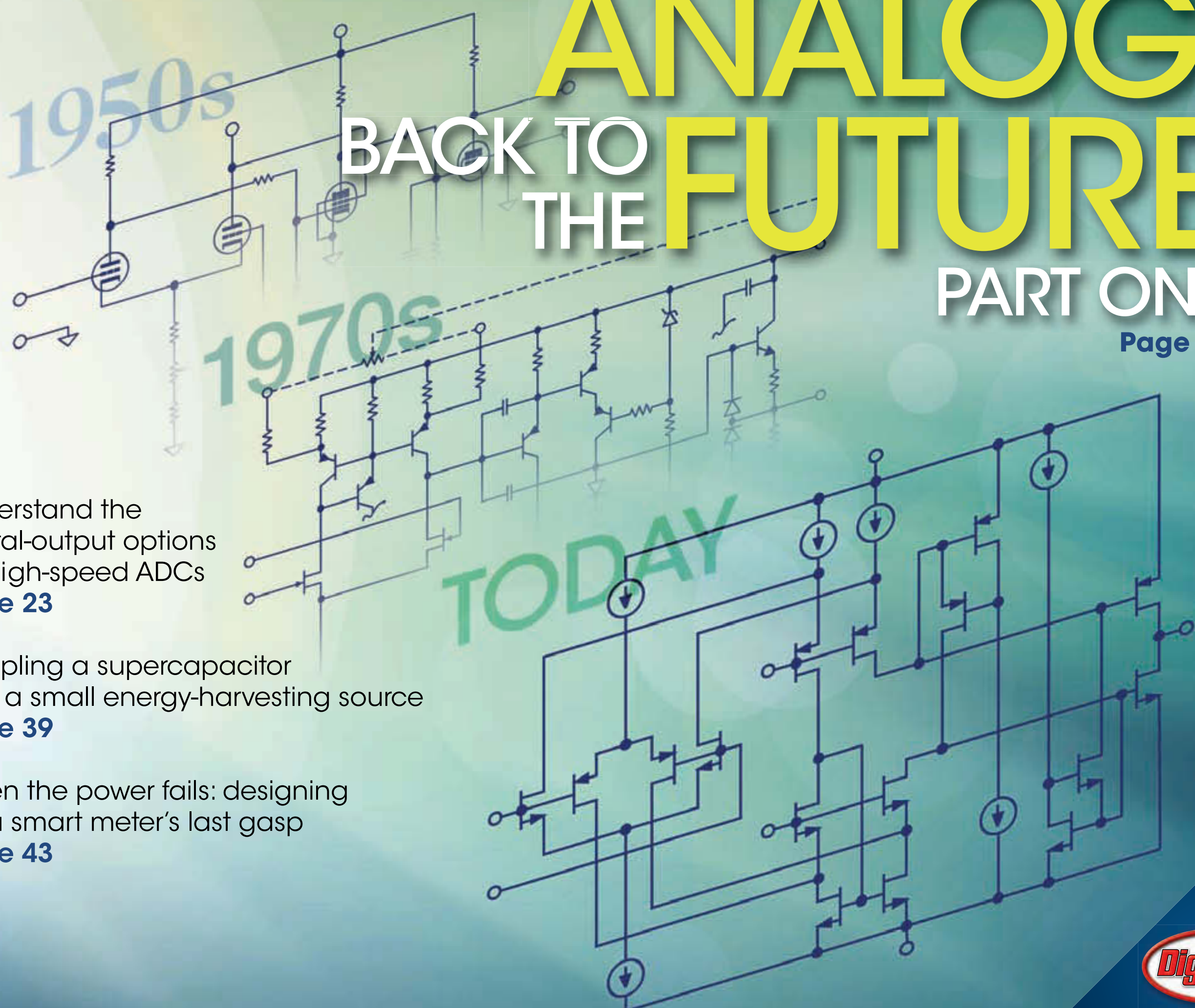

ANALOG: BACK TO THE FUTURE PART ONE

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BEST of CLASS!
Which single distributor comes to mind as being 'best of class' for broadest overall product selection?
SOURCE: 2011 DESIGN ENGINEER AND SUPPLIER INTERFACE STUDY, HEARST BUSINESS MEDIA ELECTRONICS GROUP
2%
4%
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10%
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Distributor E
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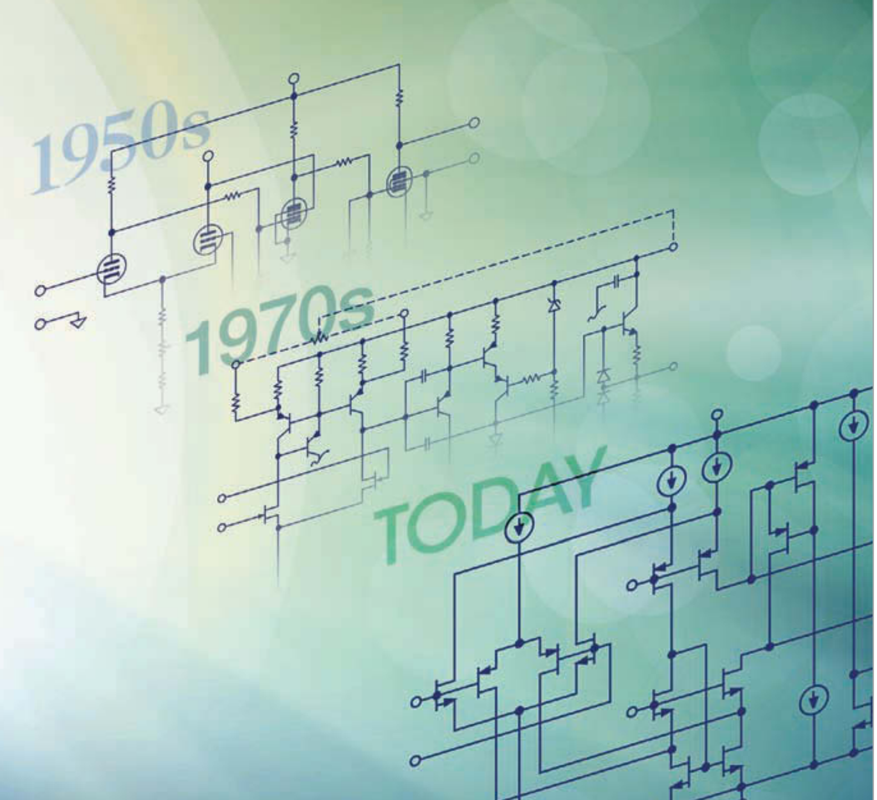

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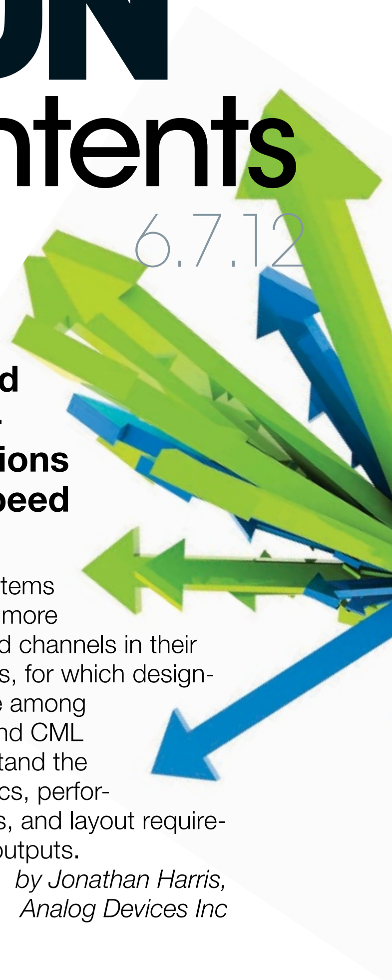
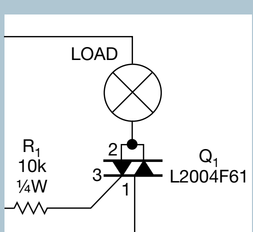
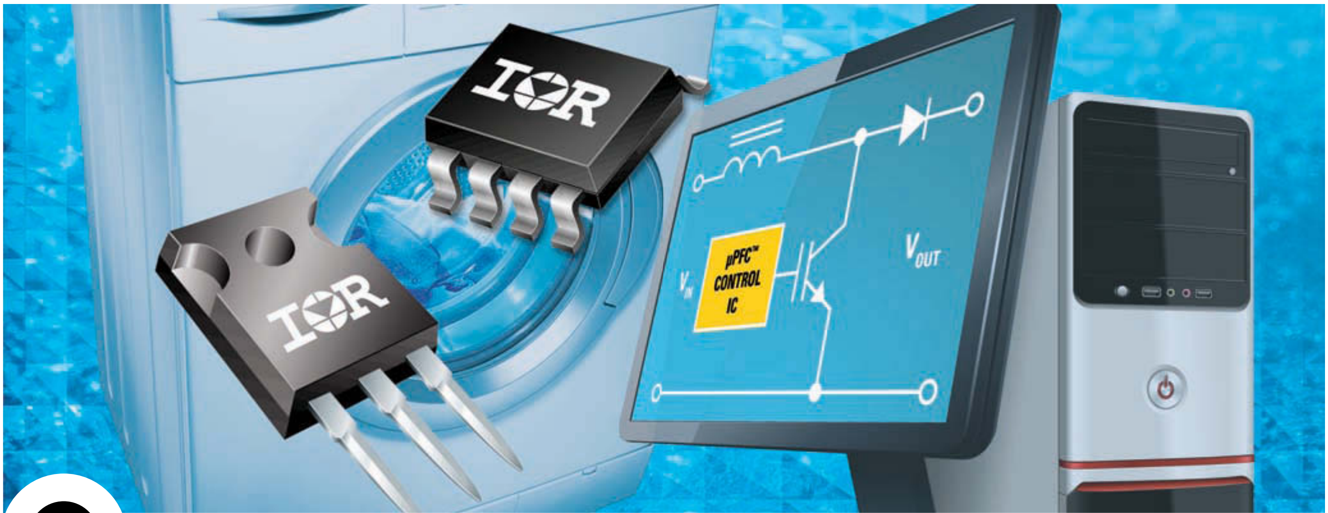


COVER IMAGE:

DESIGNIDEAS



▶ Find out how to submit your own Design Idea: http://bit.ly/DesignIdeasGuide.



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Compact, Powerful CCM PFC from 75W to 4kW+

PFC Control ICs

Part Number	Description
IR1152	Fixed 66KHz switching frequency with brownout protection and dual OVP protection
IR1153	Fixed 22KHz switching frequency with brownout protection and programmable OVP protection
IR1155	Programmable switching frequency and programmable OVP protection

600 V PFC IGBTs for High Power Systems

Part Number	Circuit	I_c @ 100C (A)	$V_{CE(on)}$ (max) (V)	Package
IRGB20B60PD1	Co-Pack	22	2.35	TO-220AB
IRGP20B60PD		22	2.35	TO-247AC
IRGP35B60PD		35	2.15	TO-247AC
IRGP50B60PD1		45	2.35	TO-247AC
IRG4(B/IB)C20W	Discrete	6.5	2.6	TO-220AB; TO-220 FullPak
IRG4(B/IB/P)C30W		12	2.7	TO-220AB; TO-220 FullPak; TO-247AC
IRG4(B/P)C40W		20	2.5	TO-262; TO-220AB; TO-247AC
IRG4PC50W		27	2.3	TO-247AC
IRGP4069		35	1.85	TO-247AC
IRGP4063		48	2.14	TO-247AC
IRGP4066		90	2.1	TO-247AC

The μPFC family of controller ICs radically alters traditional thinking about PFC solutions. The IR115x uses a "One-Cycle Control integrator with reset" technique to deliver the high performance of Continuous Conduction Mode (CCM) PFC with the simplicity and low component count of Discontinuous Current Mode (DCM).

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DEPARTMENTS & COLUMNS

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JOIN THE CONVERSATION

Comments, thoughts, and opinions shared by *EDN's* community

In response to "Debugging the case of the self-powered LED," an editorial by Bill Schweber on misreading the observed symptoms during debugging, http://bit.ly/KfAteA, John Jolley comments:

"Reminds me of a circuit on test, which was showing tens to hundreds of millivolts offset at various nodes. After looking everywhere for leakage and replacing suspect components, I eventually realized [that] the voltages persisted even with the power off but varied as I moved the test probe. LEDs work very well in reverse, as photovoltaics. Green ones seem especially effective."

In response to "Ham radio in the 21st century," a cover story by Doug Grant, K1DG, http://bit.ly/rvBoIE, Tom Straub comments:

"Thanks for the great article on the 'hobby' of amateur radio. Indeed, it was that hobby that got me interested in electrical engineering more than 40 years ago ... still at both today! KS3N"

In response to "Obsolescence by design: short-term gain, long-term loss, and an environmental crime," a blog post by Brian Dipert, http://bit.ly/KsypxY, BobSound commented:

"Regarding planned obsolescence, Detroit tried that back in the '60s, '70s, and '80s. It's not that they couldn't make good cars; they just didn't want to.

It didn't work. People revolted and flocked to imports. Only now are we seeing the public renew interest in American-designed cars, which ... are now every bit as good as the imports."

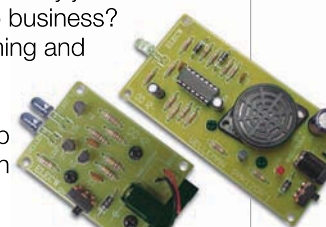
***EDN** invites all of its readers to constructively and creatively comment on our content. You'll find the opportunity to do so at the bottom of each article and blog post. To review current comment threads on EDN.com, visit http://bit.ly/EDN_Talkback.*

CONTENT

Can't-miss content on EDN.com

CLUB JAMECO WANTS TO HELP YOU MAKE MONEY IN THE KIT BUSINESS

What engineer doesn't fantasize about leaving their day job to create a start-up business? Well, stop dreaming and start designing: Club Jameco would like to help you get started in the electronics-kit business.



http://bit.ly/JKt6wk

TOP-DOWN ANALOG FLOWS: MYTH OR REALITY?

Few designs these days are not mixed-signal, meaning that designers have integrated analog functions and digital logic onto the same die. They are using this approach for several reasons, such as reduced cost. Perhaps more important, however, many analog functions now require some digital logic to allow calibration of the analog circuitry.

http://bit.ly/JKZVuU

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You've got insight, and we want you to share it. *EDN* is currently looking for engineers to blog about their specialty, experience, hobbies, or simply life as an EE. We will share and promote your words online and possibly in print to *EDN*'s audience of your peers. Interested? E-mail suzanne.deffree@ubm.com with "*EDN* bloggers wanted" in the subject line.

BY BILL SCHWEBER, CONTRIBUTING TECHNICAL EDITOR

Goodbye, hard-wired switches and circuits: We'll miss you—maybe

The other day, I watched a scene from a 1950s science-fiction movie. It took place in a factory of the future, with a control room lined with a wall of large, dedicated, single-function switches clearly labeled "furnace on," "main conveyor," and so on, just as a real factory from the '50s would. A mechanical switch directly controlled a circuit loop, which provided power to a corresponding actuator, and the reality would involve lots of switches, wires, and control loops.

Zip ahead to the 21st century, and you'll find that control panels didn't quite turn out in that way. Even if there is a labeled switch, it most likely is not directly wired into or part of the control loop. Instead, an I/O port on the system controller senses the switch, detects a switch press, uses software to assess it—most likely requiring some debounce—and takes actions based on the control program. Taking it one step further, in many designs, the switch function is actually "soft" and can change, depending on what is going on and what a display-screen label says that switch's function is at the time.

If a system has a lot of switches, they may be on some sort of internal, low-end network or matrix rather than having one input pin dedicated to each switch-closure contact. Factory-control rooms aren't alone in having this type of system. Today's cars no longer have direct loops between functions such as window controls and window motors; instead, a LAN senses the switch, and a microcontroller interprets it and sends out the necessary actions using the same LAN.

This approach makes sense because it saves wiring cost, weight, and space and provides design flexibility in locating switches and relocating them if a design needs modification. Even hobbies such as model railroading have begun to use networks through the widely adopted DCC (digital-command-control) standard. These changes haven't stopped at sensing through I/O lines or networks. The rise of now-ubiquitous touchscreens and graphical user interfaces has given us controls that don't rely on switches. The screen shows us images or buttons, and we touch it in the appropriate place. It's an efficient approach because it requires neither switches nor I/O sensing but provides lots of flexibility.

One downside to the indisputable efficiency of the soft-key and touchscreen approaches is that they require a longer path, functionally, from initiation to final action. Perhaps users also feel removed from the consequences of their actions and how they implement those actions—a psychological aspect, which is hard to assess. Beyond psychology, though, these new approaches require that more goes right, yet they incorporate technology in which more can go wrong. It's difficult to know what is going on and troubleshoot any problems that come up, and they will.

In the 1950s, you could use a meter to check out a misbehaving switch, loop, or power supply. It was all about basic power and continuity testing, and it was fairly straightforward. Even better, if something failed, you could either fix it or rig a temporary bypass using another switch or loop circuit. With today's flexible, touchscreen-based systems, you get, as the song goes, all or nothing at all.

We aren't going back to those days, and we shouldn't. The wiring virtues of the I/O-port or network-based switch and the flexibility of the touchscreen user interface are simply overwhelming for most products, at both the bill-of-materials and the system-design levels. Along with virtues, however, come shortcomings, and we should keep those shortcomings in mind. I think I'll stick with that big, red, mushroom-topped "kill" switch for critical situations.

Do you think we should retain hard-wired, direct-control mechanical switches and controls and, if so, where should we implement them? Please let me know. **EDN**

Bill Schweber is the editor of Planet Analog *and* Power Management Designline, *both on the Web site of* EE Times, *a sister publication of* EDN. *Contact him at bill.schweber@ubm.com, or comment on this column at www.edn.com/120607ed.*

EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Hall sensors find use in seat-positioning systems, seat-buckle switches, and wipers

The MLX92221 and MLX92241 Hall-effect sensors from Melexis target stringent automotive requirements, such as seat-positioning systems, seat adjusters, seat-belt-buckle switches, wipers, and motor-commutation systems. The devices come with EEPROM, allowing the setting of customer-specific parameters for magnetic switch points, output polarity, off current, and magnet-material temperature-compensation coefficient. Customers can specify characteristics to enable improvements to sensor-module yields, bill-of-materials costs, and performance.

With a wide programmable magnetic range, the MLX92221 and MLX92241 feature Hall-effect sensing elements operating from 2.7 to 24V, allowing them to address automotive, consumer, and industrial applications. The devices integrate protection mechanisms to guard against electrostatic discharge, reverse-supply voltage, and thermal overload. The reverse-supply-voltage protection protects the devices against incorrect connection of the supply line to voltages as high as –24V.

The re-engineered core magnetic-sensor circuit has an offset-cancellation system, allowing faster and more accurate processing; temperature does not affect this processing. A programmable negative-temperature coefficient compensates for the natural tendency of permanent magnets to become weaker at elevated temperatures.

The MLX92221 and MLX92241 come in ROHS-compliant, single-in-line packages for through-hole mounting, or in three-pin TSOT packages for surface mounting. Each costs €0.40, or approximately 50 cents (10,000).

—by Christoph Hammerschmidt

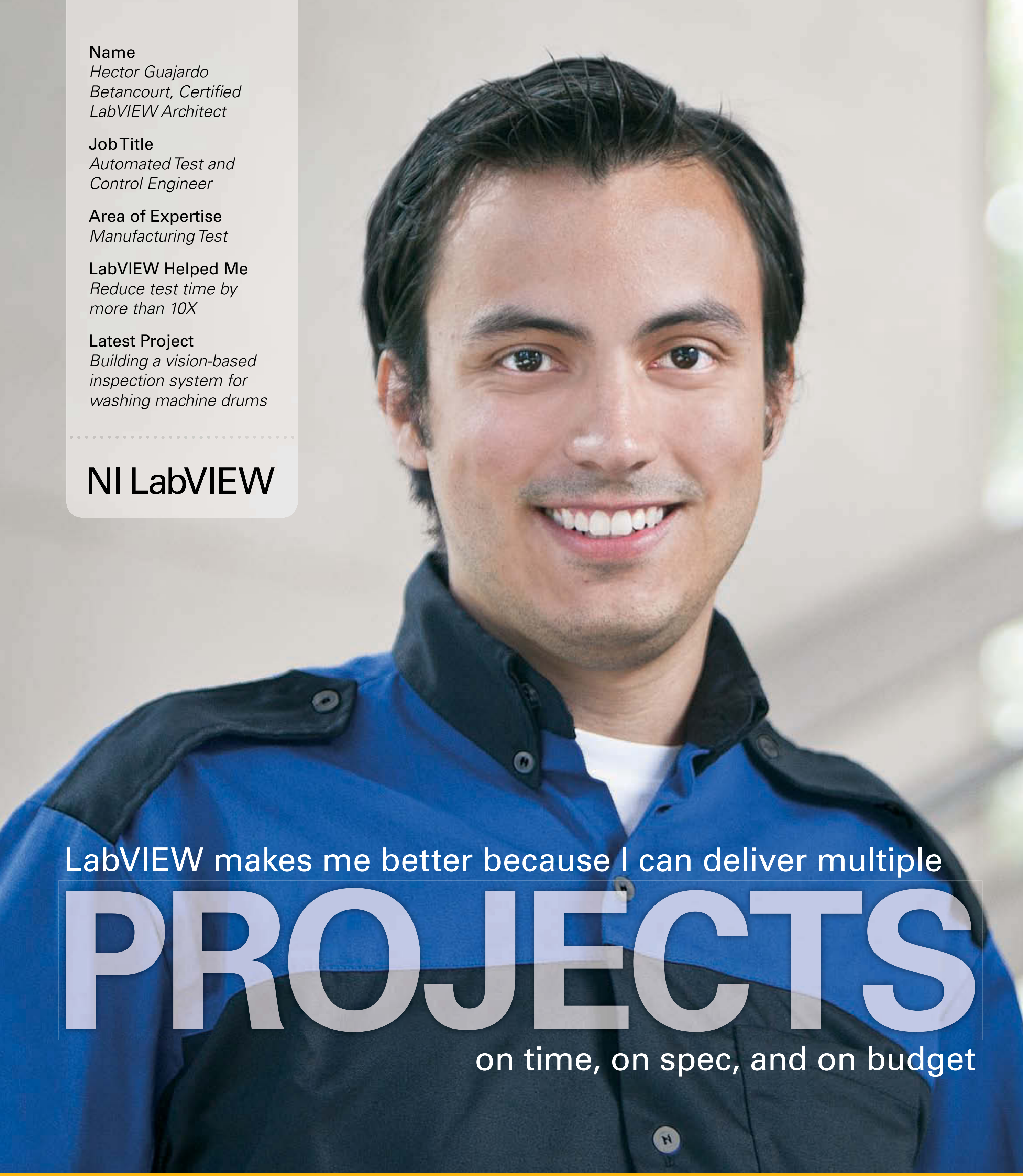
▷**Melexis**, www.melexis.com.

The MLX92221 and MLX92241 Hall-effect sensors target stringent automotive requirements, such as seat-belt buckles.

TALKBACK

"We got a service bulletin from Apple stating something like: 'If the system has failed due to overheating of components, raise the system about 6 inches above a solid surface and let it drop.' What do you know? That fixed them!"

—Engineer William Boyle, in *EDN*'s Talkback section, at http://bit.ly/JMNngU. Add your comments.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Automated Test and Control Engineer
Area of Expertise
Manufacturing Test
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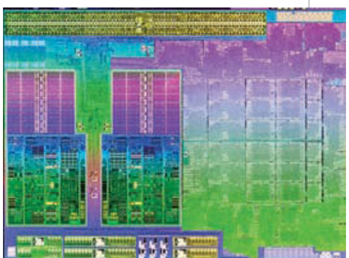
Reduce test time by more than 10X
Latest Project
Building a vision-based inspection system for washing machine drums
NI LabVIEW
LabVIEW makes me better because I can deliver multiple
PROJECTS
on time, on spec, and on budget

AMD x86 notebook goes up against Intel's Ivy Bridge

Advanced Micro Devices' new 32-nm Trinity processors go head to head in the notebook- and desktop-computer markets against Intel's 22-nm Ivy Bridge CPUs. The AMD parts sport upgraded x86 and graphics cores that keep them competitive in performance. Some parts, targeting ultrathin notebooks, consume as little as 17W. AMD claims to have shipped more than a million Trinity chips to PC makers, overcoming the difficulties that it had delivering the last generation of chips.

Intel defined the Ultrabook, a variant of the Apple MacBook Air, as its target, defining a detailed specification and supporting it with a $300 million venture-capital fund. AMD aims to enable similar kinds of systems without requiring adherence to a detailed spec, aiming to enable lower price points.

Trinity parts bring advantages both in higher performance and lower power consumption that will keep AMD competitive in the latest round. The 246-mm^2 Trinity packs 1.303 billion transistors, whereas AMD's previous Llano CPU packed 1.178 transistors into 228 mm^2. Trinity includes two or four new Piledriver x86 cores and a new Radeon 6000 series Northern Islands graphics core. They give the part performance boosts of 50% in graphics and 25% in x86 performance over the previous Llano chip, AMD claims.



The new 32-nm Trinity processors go head to head in the notebook- and desktop-computer markets against Intel's 22-nm Ivy Bridge CPUs.

The Piledriver core follows the Bulldozer core, which itself was an advance over the 45-nm Stars core in the previous Llano client CPU. The device features improved branch prediction and scheduling for both its two integer units and a shared floating-point block. The core runs at 2 to 3.8 GHz with less power leakage than Bulldozer. The new Radeon 6000 series graphics core runs at 424 to 800 MHz to deliver 736 GFLOPS and P1361 on the 3DMark 11 benchmark. The Radeon 6000 series GPU core takes up about half the die of the AMD Trinity CPU.

Trinity is AMD's first chip to use a unified memory controller for both graphics and x86 cores. It sports a new acceleration block for video encoding, and it is AMD's first chip to use PCI Express rather than HyperTransport for I/O connections. The Trinity family spans a power range of 17, 35, 65, and 100W. AMD will offer the device in a BGA-packaged, dual-core, 17W Trinity chip so that it will fit into ultrathin notebooks. AMD claims that at least 10 of its Trinity designs target these notebooks. **—by Rick Merritt**

▷**AMD**, www.amd.com.

Sensor-software library aims at accuracy

Smartphone-compass calibration is commonly off by almost 90°. Such inaccuracy is not helpful to users trying to navigate—to a shop or restaurant, for example—using the compass application in their cell phones. Sensor Platforms aims to address that issue with its new FreeMotion library and software-development kit. The library includes a collection of advanced algorithms and heuristics that interpret sensor data to determine a consumer's position and gestures.

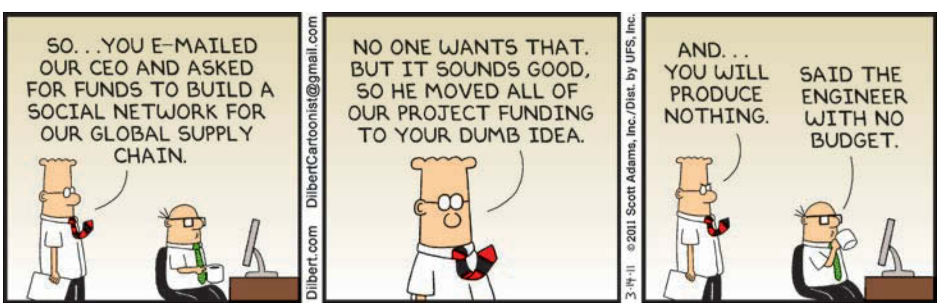
Sensors measure and report physiological data—for example, acceleration in meters per second squared or magnetic-field strength in microtesla. The data, although accurate, are meaningless to an application that needs to know what is happening to the mobile device or what a device user is doing in real time. Furthermore, accurate metrological data does not always reflect the information users require. For example, magnetic materials in everyday environments, such as vending machines and steel frames in buildings, generate magnetic fields that affect the magnetic-field sensors. If users require accurate compass directions, these additional fields interfere with the sensor's ability to measure the earth's magnetic field. FreeMotion Library monitors the environment and prevents magnetic interference to maintain accurate compass heading results.

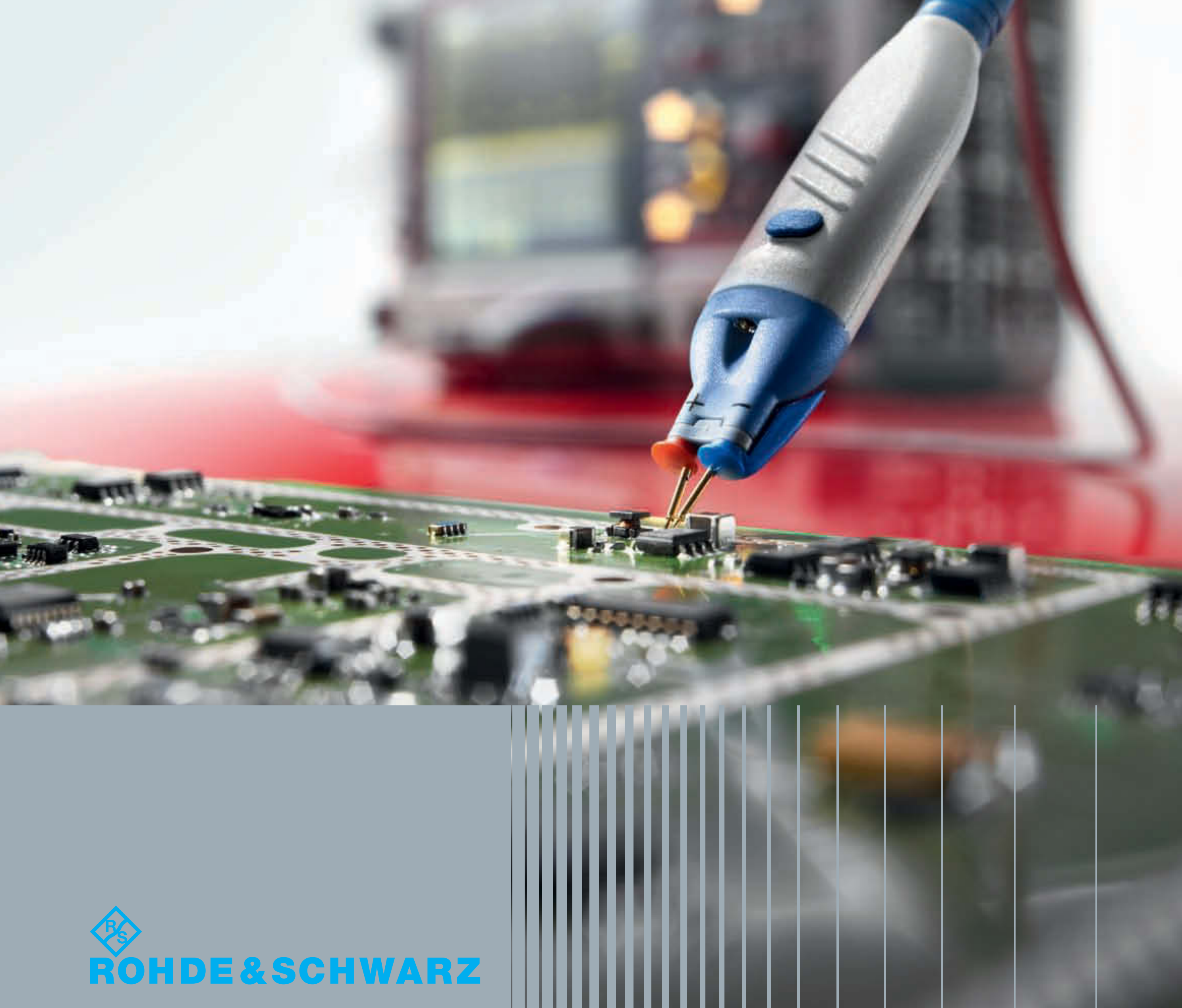
The library works in handheld electronic devices and operates from one processor. Alternatively, it can distribute the workload among a main processor and various intelligent sensors. Sensor Platforms is working with key sensor and platform makers to optimize the FreeMotion library for targeted applications. Features include Android and embedded-Linux support, intelligent resource management to balance power consumption, and a modular-building-block configuration.

—by Steve Taranovich

▷**Sensor Platforms**, www.sensorplatforms.com.

DILBERT By Scott Adams




ROHDE&SCHWARZ

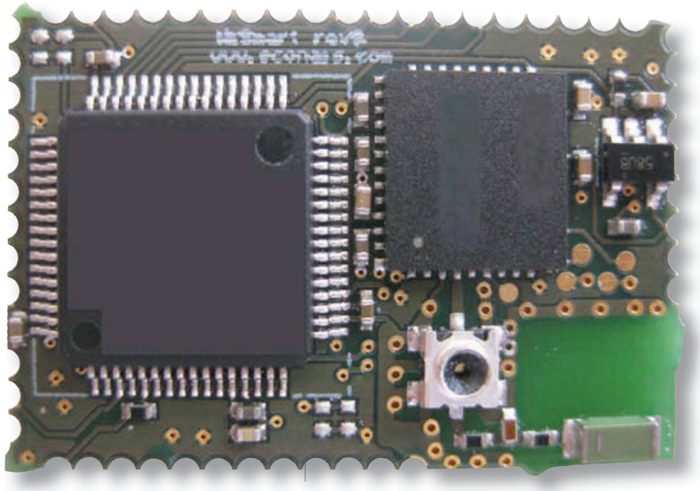
Tiny, low-power Wi-Fi module enables Internet of Things

The ultra-low-power WiSmart EC32Wxx embedded Wi-Fi platform from Econais fits into any electronic device. The module uses the STM32F1x microcontroller and, according to the company, uses the lowest-power-consumption Wi-Fi chip on the market. The device runs a tiny TCP/IP stack, with WPA/WPA2 support, leaving available 115, 243, and 371 kbytes of flash memory for the EC32W10, EC32W11, and EC32W12, respectively, for any third-party application that can use the well-defined API that the module exports. More flash memory is available in bigger versions of the microcontroller.

The EC32W1x features a 3.3V supply, operational modes with current consumption as low as 1.1 μA; receiving power of 48, 50, and 51 mA for the 802.11b, g, and n, respectively; and transmitting power consumption of 237, 219, and 214 mA at 21, 18, and 17 dBm, respectively. The device also supports 802.11 power saving; a BSS (basic-service set) and an IBSS (independent-BSS) mode; and TCP/IP, Telnet, and Web Server support. Interfaces include SPI, UART, ADC, DAC, I^2C, I^2S, microcontroller JTAG, and SDIO.

The module embeds a PCB antenna with range as far as 400m, but designers can optionally mount an external antenna on the board. The WiSmart EC32Wxx measures 27.5×18.5×1.5 mm and sells for less than $15 (1000). Samples sell for $20 per unit, and an available software-development kit costs $249. **—by Rich Pell**

▷**Econais**, www.econais.com.



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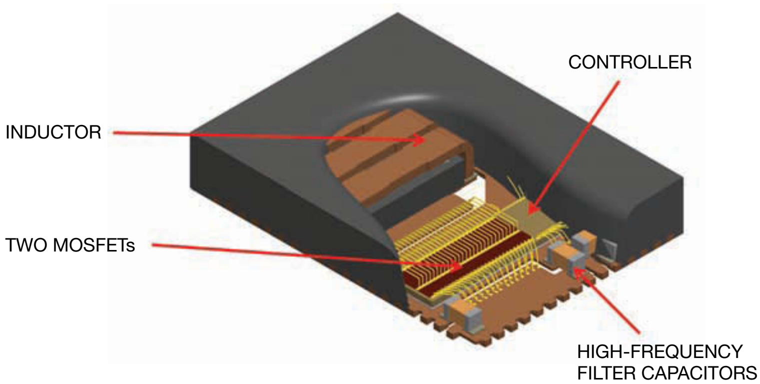
4.5 to 14V dc/dc modules use LDMOS to raise voltage and efficiency, shrink size

Using 0.18-micron LDMOS (laterally diffused metal-oxide semiconductor) technology, Enpirion's new EN2300 dc/dc converter touts an FOM (figure of merit) of 20—the highest in the industry, according to the company. This FOM—gate charge times on-resistance in milli-ohm-nanocoulombs—represents a 40% improvement over alternative LDMOS, 73% over VDMOS (virtually diffused MOS), and 33% over high-performance GaN (gallium nitride). The new process gives Enpirion's modules lots of growing room to increase the EN2300's blocking voltage, although the process can't touch the 600V-and-greater blocking voltages of SiC (silicon carbide).



The EN2300 integrates a controller, two power MOSFETs, high-frequency input capacitors, a compensation network, and an inductor in an IC-like package.

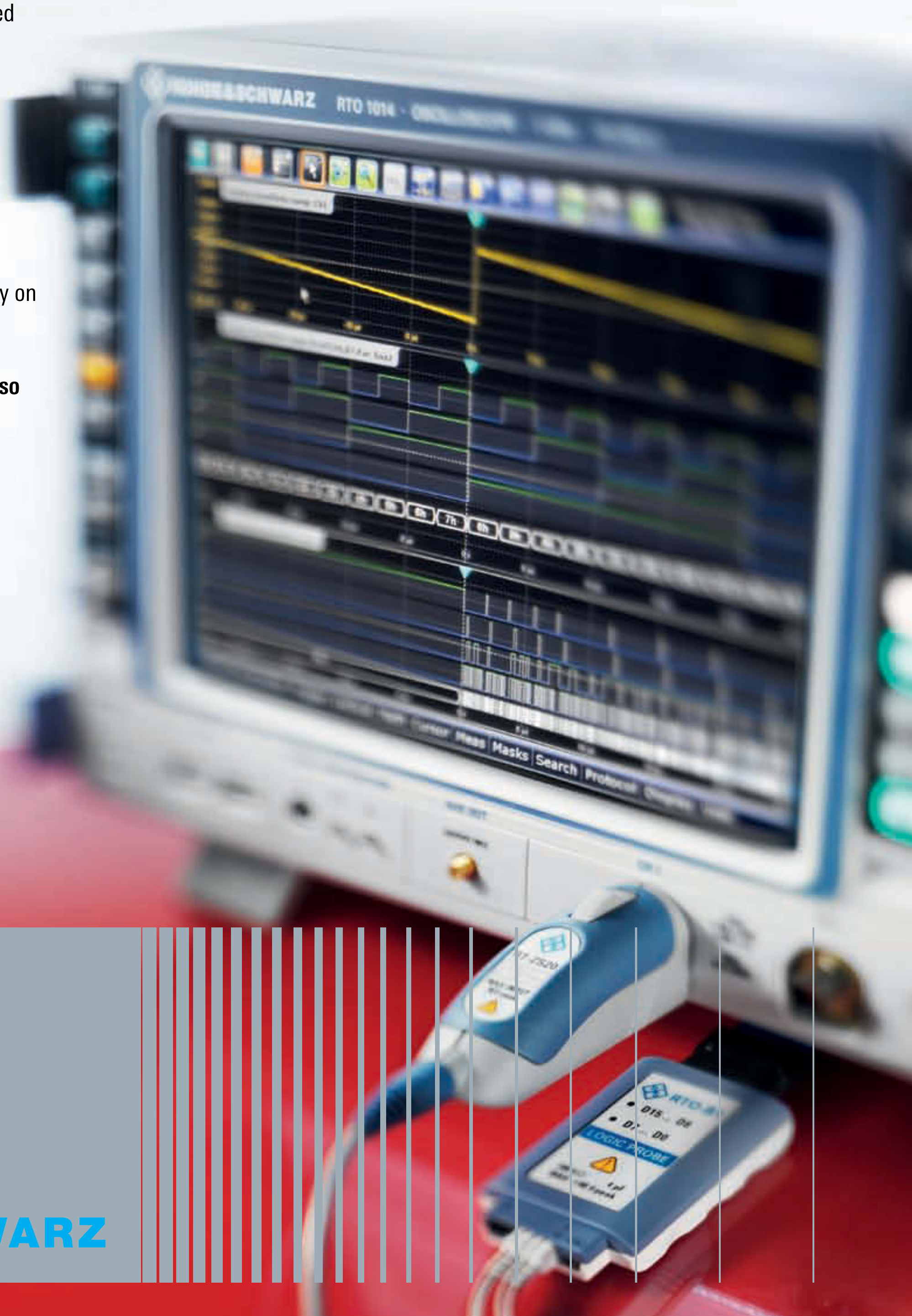
The company refers to its new modules as power systems on chips. They integrate a controller, power MOSFETs, high-frequency input capacitors, a compensation network, and an inductor in an IC-like package. This approach controls package layout and parasitics, removing those headaches from system designers. The EN2300 switches at 2 MHz.

Devices in the family feature 4 to 15A power, along with footprints of 190 to 308 mm^2, respectively. All of the devices achieve as much as 95% efficiency with a flattened efficiency profile of 10 to 100% load.

The EN2340QI, 2360QI, 2390QI, and 23F0QI 12V, fully integrated dc/dc converters sell for $3.56, $4.41, $6.60, and $9 (1000), respectively.

—by Margery Conner

▷**Enpirion**, www.enpirion.com.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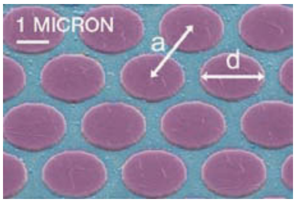
IBM demonstrates terahertz graphene photonics

Many people tout graphene as the miracle material of the future because designers have been able to fabricate formulations of it into conductors, semiconductors, and insulators. IBM has now added photonics to the list by demonstrating a graphene/insulator superlattice that achieves a terahertz-frequency notch filter and a linear polarizer. These devices could be useful in future mid- and far-infrared photonic designs, including detectors, modulators, and 3-D metamaterials.

"In addition to its good electrical properties, graphene also has exceptional optical properties," says IBM Fellow Phaedon Avouris. "It absorbs light from the far-infrared to the ultraviolet. … These frequencies can penetrate paper, wood, and other solid objects for security applications." Unfortunately, there are currently few ways of manipulating terahertz waves, such as polarizing and filtering them. Because graphene operates well at terahertz frequencies, however, IBM has



A scanning-electron-microscope image of a five-layer graphene/insulator superlattice array shows the 2-micron-diameter microdisks in purple.

been creating these types of devices.

Plasmons, the collective oscillation of carriers, can perform terahertz-frequency oscillations in graphene to enable low-loss tunable filters. In single-layer graphene, however, the carrier concentration and resonant frequency are too weak for photonics applications, according to IBM.

By using a multilayer graphene/insulator superlattice, the researchers can pattern transparent devices into photonics-like crystals that distribute the carriers among the layers, effectively enhancing both the carrier density and the resonant frequency.

"Graphene interaction with electromagnetic radiation is particularly strong in the terahertz range," says Hugen Yan, a member of the nanoscale science and technology group at IBM's TJ Watson Research Lab. "However, with a single layer of graphene, the interaction [is] still not strong enough." Using a multilayer-stack structure in microdisk arrays, however, IBM achieves frequency selectivity in the terahertz range, allowing the company to tune the desired resonant frequency.

By patterning the graphene/insulator microdisks in arrays, IBM tuned the disks' resonant frequency by varying their size, the number of layers, their spacing, and the doping of the graphene layers. After analyzing the microdisks, the researchers discovered a unique carrier-density-scaling law for its graphene/insulator superlattices. Unlike conventional semiconductor superlattices, IBM's discovery employs laws governing Dirac fermions, such as quarks, leptons, baryons, and hadrons.

As a result, IBM has been able to demonstrate patterned graphene/insulator stacks implementing widely tunable notch filters with an 8.2-dB rejection ratio and a terahertz linear polarizer with 9.5-dB extinction ratio. IBM implemented these components by laying down wafer-scale alternating layers of graphene and a polymer insulator and then patterning them into microdisks, demonstrating that these graphene/insulator superlattices shielded 97.5% of electromagnetic radiation at frequencies below 1.2 THz.

The research group intends to tune its graphene/insulator superlattices for the infrared frequencies that optical-communications equipment now uses. Fengnian Xia, a member of the Nanoscale Science and Technology Group at TJ Watson Research Lab, also contributed to the work.

—by R Colin Johnson

▷**IBM Corp**, www.ibm.com.

Club helps you make money in the kit business

06.07.12

Maybe you've fantasized about starting the next electronics-kit business—like Sparkfun or Adafruit. These companies started by offering kits or specialized electronic parts and grew into multimillion-dollar businesses. Well, stop dreaming and start designing: Jameco would like to help you get started in the electronics-kit business. The electronics distributor has started Club Jameco, an electronics-project community in which members can design, sell, teach, and learn about electronics projects and kits.

You design a step-by-step project; Jameco then creates and sells the kit for your project and pays you a royalty on every sale. The first $200 in sales for any kit in each quarter yields a royalty payment of 5% of net sales. Sales of $200 to $500 yield 8% of net sales, and sales of more than $500 yield 10% of net sales.

You start by creating a product brief for your kit idea—just a paragraph or so describing the project. Once Jameco approves your brief, it publishes the brief within the Club Jameco community, and members can comment and vote on the project. Voting enables a registered Club Jameco member to design a project for submission to Jameco for a kit. Jameco assigns a price to the kit, but you can get a good idea of the ultimate kit price by adding the kit parts to your Jameco shopping cart.

Your kit will probably need a PCB—no problem because one of Jameco's partners is Bay Area Circuits, which makes custom PCBs for hobbyists. Bay Area makes your kit's PCBs using Gerber files that you upload as part of the project-design step.—by Margery Conner

▶**Jameco**, www.jameco.com.

Buck regulators target automotive designs and more

Automotive-targeted designs involve more than serving the needs of big-battery hybrid and all-electric vehicles. Even gas- and diesel-powered cars must handle higher voltage rails than those in portable, battery-powered products; avoid interference with in-dash AM radios; and have "off" current drain lower than the manufacturer's quiescent allocation—a miserly 15 to 20 mA.

The LT8610 from Linear Technology focuses on the special requirements of automotive regulators. It takes input voltages spanning single digits to 40V, operates at 3.9 to 42V, and can function at cold-crank battery voltages. The device touts efficiency of 96% with 12V input and 5V output and efficiency as high as 94% with 3.3V output, delivering as much as 2.5A through internal switches. The unit switches at frequencies of 200 kHz to 2 MHz, even at low duty cycles, due to a 50-nsec minimum on time. It can thus operate at frequencies beyond the 550- to 1600-kHz AM band, removing it as an in-band interference source.

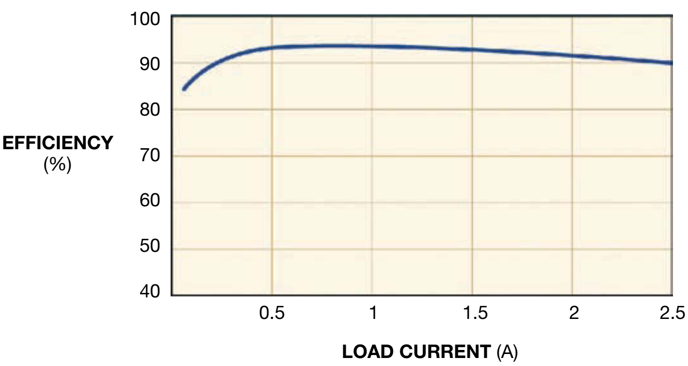
The IC's no-load quiescent current is less than 2.5 μA, making it a small burden on the vehicle's quiescent-current budget. Careful control of the switching slew rate contributes to low overall electromagnetic interference. Output ripple is less than 10 mV p-p, and dropout voltage is 200 mV at a 1A load. It also includes now-standard features, such as output soft-start and tracking, internal compensation, undervoltage lockout, and a thermally enhanced package.

The otherwise-similar LT8611 adds an uncommitted op amp with monitor and control pins. You can use this device as a rail-to-rail current-sense amplifier to implement input or output current regulation and limiting.

The –40 to +125°C LT8610 comes in a 16-lead MSOP and sells for $3.55 (1000); the more auto-compatible version operates at –40 to +150°C and sells for $4.16. The LT8611 comes in a 3×5-mm QFN-24 package and sells for $3.80.

—by Bill Schweber

▷**Linear Technology Corp**, www.linear.com/product/LT8610; www.linear.com/product/LT8611.



The LT8610 and LT8611 synchronous buck regulators support high voltages for automotive designs, along with switching beyond the AM-radio band.

Constant-current wall warts streamline LED-driver design

The lowly wall-wart power adapter finds use in millions of electronics devices as a cost- and power-efficient ac/dc-voltage-regulated power supply. Designers of electronics have, in effect, outsourced their products' ac/dc conversion, voltage regulation, and regulatory compliance to the wall wart for most low-watt power-supply challenges. The designers of my LED desk lamp, for example, outsourced some but not all of its power-conversion and -regulation needs to an ac/dc-voltage-regulated wall wart. Because LEDs are constant-current rather than constant-voltage devices, the lamp still must include current-regulation circuitry; virtually all wall warts provide voltage rather than current regulation.

Addressing this need, power-supply manufacturer Phihong has introduced a line of constant-current wall-wart adapters that provides current rather than voltage regulation. With these products, designers of relatively low-power LED applications, such as desk lamps or under-cabinet lighting, needn't worry about driver design or meeting UL or Energy Star specifications. Phihong's PDA006A series of 6W LED adapters is available with 350-, 700-, or 1000-mA outputs; the PDA012A series of 12W LED adapters is available with 350-, 700-, 1000-, or 1500-mA outputs; and the PDA024A series of 24W LED adapters is available in 700-, 1000-, or 1500-mA outputs.

All of the UL 8750-compliant drivers feature Level V efficiency markings and have power factors greater than 0.9. Other features for the UL1310 Class 2 output drivers include overvoltage, overcurrent, short-circuit, and open-circuit protection. The no-load power draw at 115V ac is less than 300 mW. Preliminary prices for the 6, 12, and 24W devices are $8.66, $13.91, and $19.62, respectively.

—by Margery Conner

▷**Phihong**, www.phihong.com.

Phihong's constant-current wall-wart adapters provide current rather than voltage regulation.

100W-equivalent LED bulbs debut

Philips recently showed off a 100W LED-replacement bulb, which joins the ranks of candidates from GE and Osram Sylvania. Although Philips doesn't discuss production versions of the bulb, it's likely to make its appearance this fall at retailers such as Home Depot and Lowe's at a price of $50 to $70. A typical 100W incandescent bulb has an output of about 1700 lumens, for an efficacy of 17 lumens/W. Philips does not reveal the light output or power draw of the bulb but refers to it as a "true 100W equivalent." The 20W Osram Sylvania bulb, meanwhile, outputs only 1600 lumens.

Like previous Philips LED-replacement bulbs, the Philips unit relies on a secondary phosphor design. A recent update from the company claims that the bulb saves more than 75% in energy, provides 20 times the life of incandescent bulbs, and provides omnidirectional light design with instant light at ignition.

—by Margery Conner

▷**Philips**, www.philips.com.

Philips' 100W LED-replacement bulb should make an appearance this fall at retailers such as Home Depot and Lowe's at a price of $50 to $70.

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UNDERSTAND THE DIGITAL-OUTPUT OPTIONS FOR HIGH-SPEED ADCs

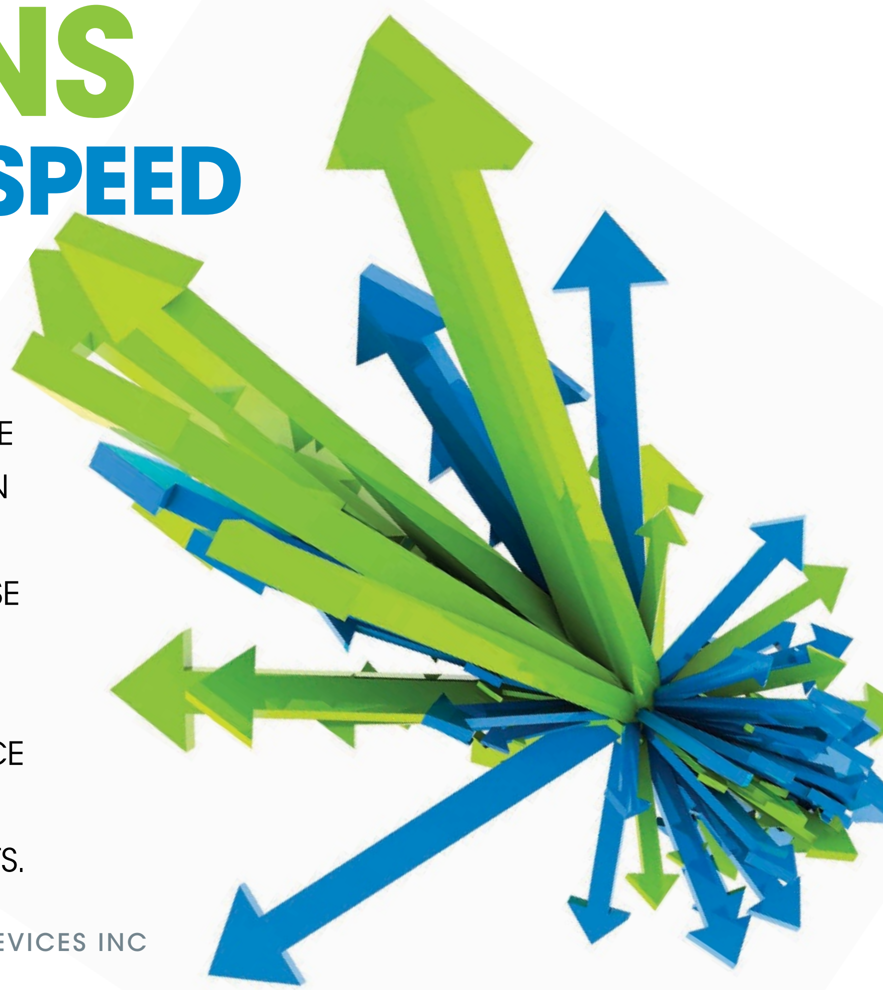

IMAGE: ISTOCKPHOTO.COM

LARGE SYSTEMS ARE USING MORE AND HIGHER-SPEED CHANNELS IN THEIR ANALOG FRONT ENDS, FOR WHICH DESIGNERS MUST CHOOSE AMONG CMOS, LVDS, AND CML OUTPUTS. UNDERSTAND THE KEY CHARACTERISTICS, PERFORMANCE TRADE-OFFS, AND LAYOUT REQUIREMENTS OF THESE OUTPUTS.

BY JONATHAN HARRIS • ANALOG DEVICES INC

With a multitude of ADC choices available for designers, they must consider what type of digital-data outputs to use: CMOS (complementary metal-oxide semiconductor), LVDS (low-voltage differential signaling), or CML (current-mode logic). Each of the digital-output types used in ADCs has advantages and disadvantages that designers should consider for their applications. These factors depend on the sampling rate and the resolution of the ADC, the output data rates, and the power requirements of the system design, among other factors.

CMOS DRIVERS

CMOS digital outputs are common in ADCs with sample rates lower than 200M samples/sec. A typical CMOS driver comprises one NMOS transistor and one PMOS transistor, which connect between the drain-to-drain, or power-supply, voltage, V_{DD}, and ground (**Figure 1a**). This structure results in an inversion in the output. Alternatively, you can use a back-to-back structure to avoid the inversion in the output (**Figure 1b**).

The CMOS output driver has a high-impedance input and a low-impedance output. At the input to the driver, the impedance of the gates of the two CMOS transistors is quite high because the gate oxide isolates the gate from any conducting material. The impedances at the input can range from kilohms to megohms.

At the driver's output, the drain current, I_D, which is typically small, governs the impedance. In this case, the impedance is usually less than a few hundred ohms. The voltage levels for CMOS swing from approximately the power-supply voltage to ground and can therefore be large, depending on the power-supply voltage. Because the input impedance is high and the output impedance is relatively low, one CMOS output can typically drive multiple CMOS inputs.

CMOS outputs also have low static current. Significant current flow occurs only during a switching event on the CMOS driver. When the driver is in either a low state—that is, pulled to ground—or a high state—that is, pulled to the power-supply voltage—little current flows through the driver. However, when the driver is switching from a low state to a high state or from a high state to a low state, a momentary low-resistance path occurs from the power-supply voltage to ground. This transient current is one of the main reasons that designers typically use other technologies for output drivers in ADCs with sampling rates higher than 200M samples/sec.

Another reason is that each bit of the converter requires a CMOS driver. A 14-bit ADC requires 14 CMOS output drivers. This constraint requires the use of more than one converter in a package; the use of as many as eight converters in a package is common, compounding the problem of multiple drivers. For example, using CMOS technology could require as many as 112 output pins for just the data outputs. This arrangement would not only be prohibitive from a packaging standpoint but also would consume more power and increase the complexity of the PCB layout. To combat these issues, manufacturers introduced an interface using LVDS.

AT A GLANCE

- As high-end instrumentation pushes faster ADC speeds and higher channel counts and density, designers must assess converter-output format as well as basic conversion performance.
- The dominant output options are CMOS (complementary metal-oxide semiconductor), LVDS (low-voltage differential signaling), and CML (current-mode logic).
- Issues to consider include power consumption, transients, data and clock skew, and noise immunity.
- Layout considerations also play a role in the selection of a converter output, especially when working with LVDS technology.

LVDS DRIVERS

LVDS offers some advantages over CMOS technology, including the facts that it operates with a signal of only approximately 350 mV and that it is differential rather than single-ended. The lower voltage swing has faster switching and reduces EMI concerns. Because LVDS technology is differential, it also has common-mode rejection, meaning that noise that couples to the signals tends to be common to both signal paths, and the differential receiver cancels out most of it.

You must more tightly control the impedances in LVDS, and the load resistance must be approximately 100Ω. Designers typically achieve this resistance by using a parallel-termination resistor at the LVDS receiver. You must also route LVDS signals using controlled-impedance transmission lines. Single-ended designs require 50Ω impedance, whereas differential designs maintain impedance at 100Ω (**Figure 2**).

As the LVDS-output-driver topology shows, the circuit's operation results in a fixed dc-load current on the output supplies, avoiding the current spikes seen in a typical CMOS output driver when the output-logic state changes. The nominal current source/sink in the circuit is 3.5 mA, which results in a typical output voltage swing of 350 mV with a 100Ω termination resistor. The common-mode level of the circuit is typically 1.2V, which is compatible with 3.3, 2.5, and 1.8V supply voltages.

The most common standard for LVDS is the ANSI/TIA/EIA-644 specification, "Electrical Characteristics of Low Voltage Differential Signaling Interface Circuits." Another is the IEEE standard for LVDS for the SCI (scalable coherent interface). LVDS requires careful attention to the physical layout of the routing of the signals but offers many advantages for converters that sample at 200M samples/sec or more. The constant current of the LVDS driver allows you to drive many outputs without the large amount of current draw that CMOS would require. You can also operate LVDS in DDR mode, which routes 2 data bits through the same LVDS-output driver, requiring half the number of pins that CMOS requires.

LVDS also reduces power consumption for the same number of data outputs. However, as converter resolution increases, PCB layouts have a more difficult task of handling the many data outputs that an LVDS interface requires. The ADCs' sample rates eventually push the interface's required data rates beyond the capabilities of LVDS.

CML DRIVERS

The latest trend in digital-output interfaces for converters is to use a serial data interface with CML-output drivers. Typically, converters that use these drivers have resolutions of 14 bits or greater, speeds of 200M samples/sec or greater, and a requirement for small packages with low power consumption. The latest converters use the current revision of the JESD204 interface, which has a CML-output driver, enabling them to operate as fast as 12 Gbps, dramatically reducing the number of required output pins.

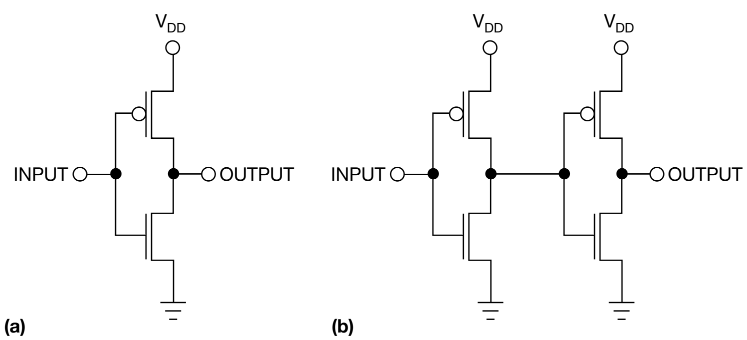

Figure 1 The digital-output driver of a typical CMOS can be an inverted (a) or a non-inverted configuration (b).

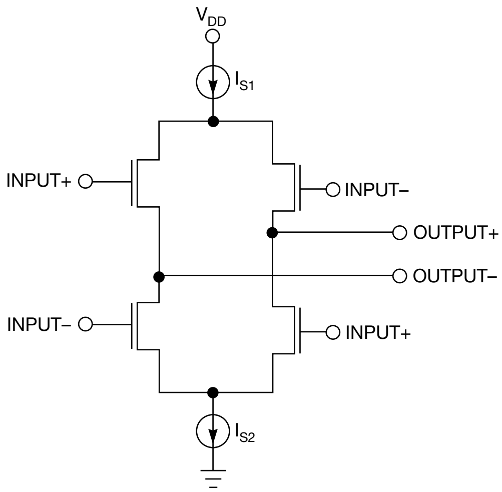

Figure 2 The LVDS-output driver offers controlled input and output impedances.

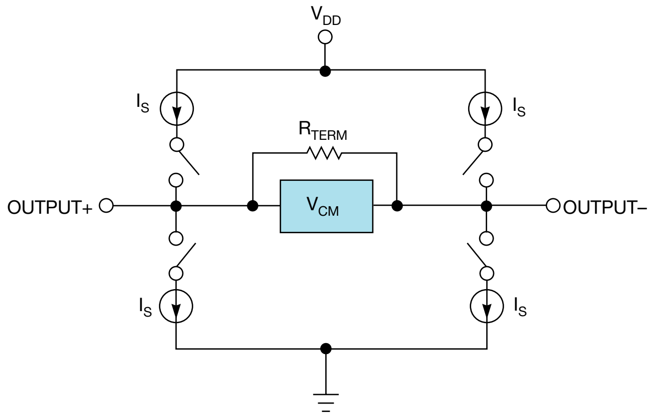

Figure 3 The CML-output-driver inputs to the circuit drive the switches for the current sources, in turn driving the appropriate logic value to the two output terminals.

You need no longer route a separate clock signal because the 8b/10b-encoded data stream, which the standard defines, embeds the clock. The standard also reduces the number of needed data-output pins to a minimum of two. As the resolution, speed, and channel count of the converter increase, the number of data-output pins can scale to account for the greater throughput. However, because a CML-driver interface is typically serial, the interface requires fewer pins than does CMOS or LVDS. The transmitted data in CMOS or LVDS is parallel, which requires more pins.

Table 1 shows the pin counts for the interfaces using an 80M-sample/sec converter with various channel counts and bit resolutions. The data assumes a synchronization clock for each channel's data in the case of the CMOS and LVDS outputs and a maximum data rate of 3.2 Gbps for JESD204 data transfer using the CML outputs. The **table** shows the reasons for the progression to CML, as well as the achievable dramatic reduction in pin count.

Because serial-data interfaces use CML drivers, they also require fewer pins. **Figure 3** shows a typical CML driver for converters with JESD204 or similar data outputs. The **figure** shows the optional source-termination resistor and the common-mode voltage. The inputs to the circuit drive the switches to the current sources, which drive the appropriate logic value to the two output terminals.

A CML driver is similar to an LVDS driver in that it operates in a constant-current mode, giving the CML driver an advantage in power consumption. Operating in a constant-current mode requires fewer output pins and reduces the total power consumption. As with LVDS, this design requires a load termination and controlled-impedance transmission lines having a single-ended impedance of 50Ω and a differential impedance of 100Ω. The driver itself may also have terminations to help with any signal reflections due to the sensitivity of such high-bandwidth signals.

Converters that comply with the JESD204 standard have different specifications for the differential- and common-mode-voltage levels, depending on the speed of operation. Operating at speeds as high as 6.375 Gbps, ADCs using the differential technology have nominal voltages of 800 mV, whereas those using the common mode have approximately 1V voltages. When these systems operate at speeds of 6.375 to 12.5 Gbps, the differential-voltage level is 400 mV, whereas the common-mode level is again approximately 1V. As converter speed and resolution increase, CML outputs are increasingly becoming the desired driver type to deliver the speeds necessary to keep pace with technology demands on converters.

DIGITAL TIMING

Each of the digital-output-driver types has timing relationships that require close attention. Because CMOS and

TABLE 1 PIN COUNTS FOR 80M-SAMPLE/SEC ADCs

Number of channels	Resolution (bits)	CMOS pin count	LVDS pin count (DDR)	CML pin count (JESD204)
One	12	13	Seven	Four
Two	12	26	14	Four
Four	12	52	28	Six
Eight	12	104	56	Six
One	14	15	Eight	Four
Two	14	30	16	Four
Four	14	60	32	Six
Eight	14	120	64	Six
One	16	17	Nine	Four
Two	16	34	18	Four
Four	16	68	36	Six
Eight	16	136	72	Six

LVDS have multiple data outputs, the routing paths of the signals require extra attention to minimize skew. If the difference is too large, the design may not achieve proper timing at the receiver. In addition, you must route and align the clock signal with the data outputs. This task demands careful attention to the routing paths between the clock output and the data outputs to ensure that the skew is not large.

The routing paths between the digital outputs in CML also require attention. There are significantly fewer data outputs to manage, so this task does become easier, but designers cannot neglect it. In this case, you need not worry about timing skew between the data outputs and the clock output because the clock is embedded in the data. However, the CDR (clock-data-recovery) circuit in the receiver requires adequate attention.

In addition to the skew, designers must carefully watch the setup-and-hold times with CMOS and LVDS, including driving the data outputs to their appropriate logic state before the edge transition of the clock occurs and maintaining that logic state long enough after the edge transition of the clock ends. The skew between the data outputs and the clock outputs affects this situation, so it is important to maintain good timing relationships.

LVDS has lower signal swings than CMOS, and it also supports differential signaling. The LVDS-output driver drives a smaller signal to many outputs and draws less current from the power supply when switching logic states than CMOS, making it less likely for problems to arise during a change in logic state. A large number of simultaneously switching CMOS drivers could pull down the power-supply voltage and introduce issues during the driving of the correct logic values to the receiver. LVDS drivers would maintain a constant level of current, thus avoiding this issue. The LVDS drivers are also inherently more immune to common-mode noise due to their use of differential signaling.

The CML drivers have similar benefits to those of LVDS. These drivers also have a constant level of current but, unlike LVDS, require less current due to the serialization of the data. The CML drivers also offer immunity to common-mode noise because they also use differential signaling. However, the disadvantage of LVDS and CML is that their current is constant; thus, even at lower sample rates, the power consumption can still be significant. The advantage of using LVDS or CML over CMOS for converters with higher speeds and resolutions is a significant reduction in both power and pin count.

As converter technology progresses with increased speeds and resolution, the digital-output drivers have adapted and evolved to meet the requirements necessary to transmit data. CML outputs are becoming more popular as the digital-output interfaces in converters make the move to serialized-data transmission. However, today's designs are still using CMOS and LVDS digital outputs. The type of digital output you use depends on the application.

In converters with sampling speeds lower than 200M sample/sec, CMOS is still an appropriate technology. When sampling speeds increase to more than 200M samples/sec, LVDS becomes a more viable option in many applications. CML drivers with a serialized data interface, such as JESD204, can further increase efficiency and reduce power and package size. EDN

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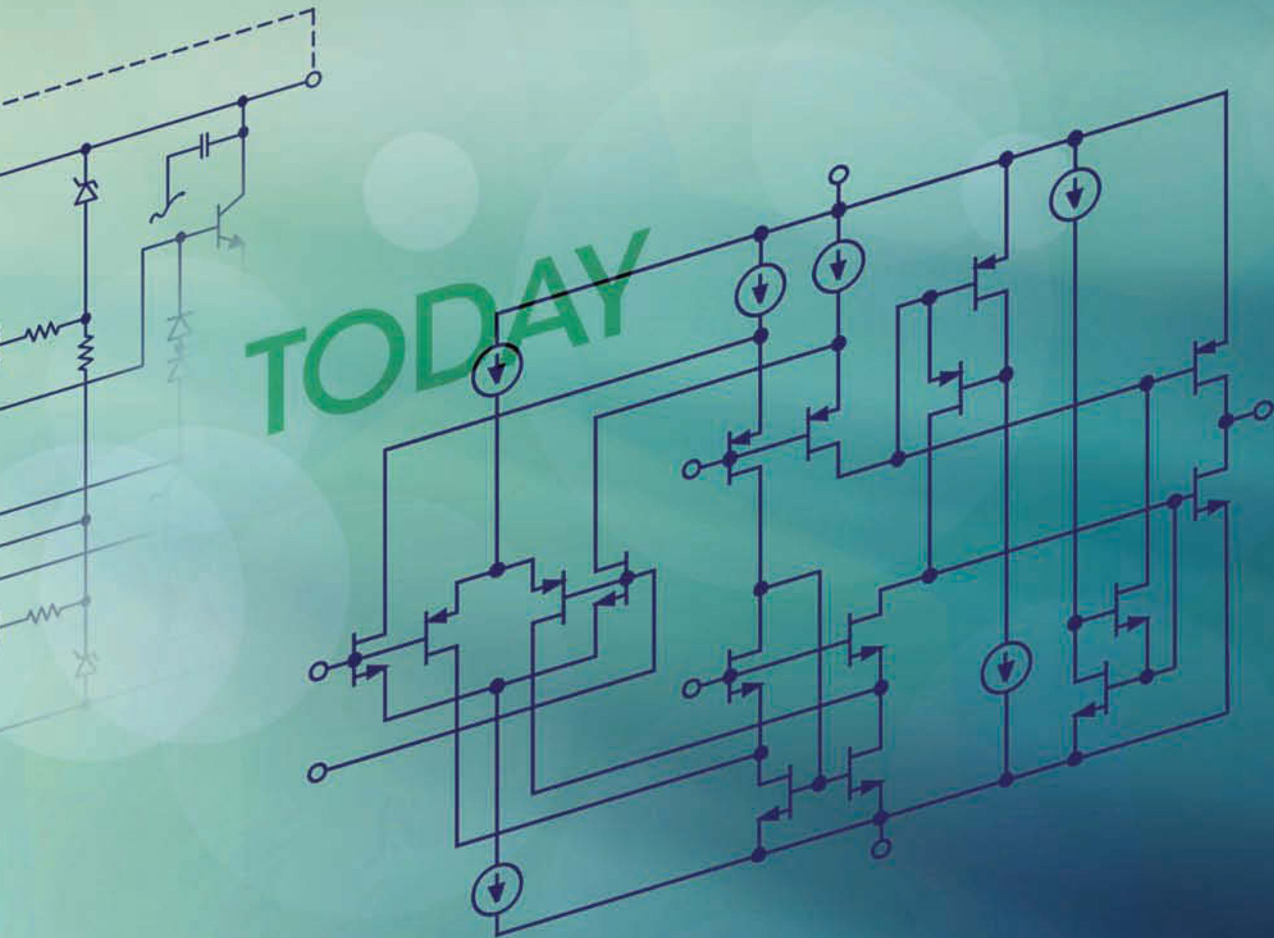
AUTHOR'S BIOGRAPHY

Jonathan Harris is a product-application engineer for the high-speed-converter group at Analog Devices Inc (Greensboro, NC). He has more than seven years of experience as an application engineer supporting products in the RF industry. Harris received a master's degree in electrical engineering from Auburn University (Auburn, AL) and a bachelor's degree in electrical engineering from the University of North Carolina—Charlotte.

ANALOG: BACK TO THE FUTURE PART ONE



A JOURNEY TO THE PAST SHEDS LIGHT ON TODAY'S ANALOG-IC INDUSTRY.

BY STEVE TARANOVICH • SENIOR TECHNICAL EDITOR

IMAGE BACKGROUND(S): SHUTTERSTOCK

Examining history provides an eye-opening education into our predecessors' successes and failures and may provide lessons on what to avoid and what to emulate in our lives. This fact holds true not only in daily life but also in analog-IC and analog-circuit design. Innovative developers and developments were the foundations that led to 21st-century analog products that we now use in design. This article delves into early precision-op-amp development from National Semiconductor, Texas Instruments, and Linear Technology. Future installments will focus on Burr-Brown, Analog Devices, Microchip, and Maxim and on pioneers in analog technology.

GENESIS OF THE OP-AMP IC

By experiencing and learning from their growing pains along the course of IC development, a few designers stand out. Several of these designers were originally with National Semiconductor but are now part of Texas Instruments, and they are guiding chip-design engineers along a new path of success for the next level of ICs that circuit designers so desperately need in today's demanding market. According to Dennis Monticelli, TI fellow, the story of computers is also the story of IC development; you can't separate them. His co-worker, Chief Technology Officer Erroll Dietz, remembers the early days of analog ICs as the "Wild West of electronics." Using design rules that they made up as they went along, these designers worked from transistor-kit parts, used copper-clad breadboards with sockets as design tools, and employed discrete resistors and capacitors (**Figure 1**).

"Kit parts were transistors manufactured in the linear IC-fab lines bonded up in metal can packages," says Mike Maida, a distinguished member of the technical staff at TI. "Design rules [used] spacing to adhere to in IC layouts—for example, base to isolation, emitter inside base, [and the like]. Designers sometimes figured out their own [design rules] for special situations, such as reduced voltages, although the fab engineers had to sign off on them. We had little mylar 'rulers' to measure spacings on the IC composite drawings."

The designers performed simulations using Level 2 Spice, which used an enhanced Grove equation, the most common MOS equation in all simulators. HKJ Ihantola and JL Moll in 1964 developed the equation (**Reference 1**). A discontinuity in transconductance at the time made life difficult for designers. Designs operating at frequencies higher than a few megahertz were difficult to breadboard, for example. "Simulation is a late-'70s thing," says Maida. "No one simulated linear ICs [then]."

"There was a large discontinuity in the Level 2 MOS model for the region between strong inversion and weak inversion," says Don Archer, also a distinguished member of the technical staff at TI. "When operating in the quasi-subthreshold region, model discontinuity was a major problem for convergence, and, when we started, there was no modeling group. We measured kit parts and came up with our own model parameters."

The designers also lacked the ability to capture schematics; they had to manually type the netlist, including emitter, base, and collector values, and manually generate a schematic to check the accuracy of those values. They then added the simulation-node numbers to the hand-drawn schematic. The lines in the netlist might read, for example, Q1 8 7 4 0 NPN1, which would mean that Q_1 is device type NPN1, with a collector node of eight, a base node of seven, an emitter node of four, and a substrate node of zero. They had to type a similar line for every transistor, resistor, and capacitor.

"To look at waveforms, we had to use plot and print [commands] to specify nodes to be printed or plotted," says Farhood Moraveji, technical director at TI. "For more complex circuits with hierarchy, we had to use [a subcircuit command]. Back-end tools didn't exist or were primitive. DRCs [design-rule checks] and LVS [layout-versus-sche-

AT A GLANCE

- National Semiconductor designers provide a snapshot of the challenges of IC design from 30 to 40 years ago and how those experiences brought about today's ICs.
- Designers developed so-called kludge boxes to verify the performance of designs and sometimes later used them in production-test equipment.
- Designers used simulation tools for validation, but they had to first perform manual calculations, and breadboarding was standard practice until the mid-1980s.
- Bob Dobkin, Linear Technology's co-founder, vice president of engineering, and chief technology officer, spent his early design days at National Semiconductor, where his creativity was evident in moving early op amps beyond the 1-MHz-bandwidth barrier.

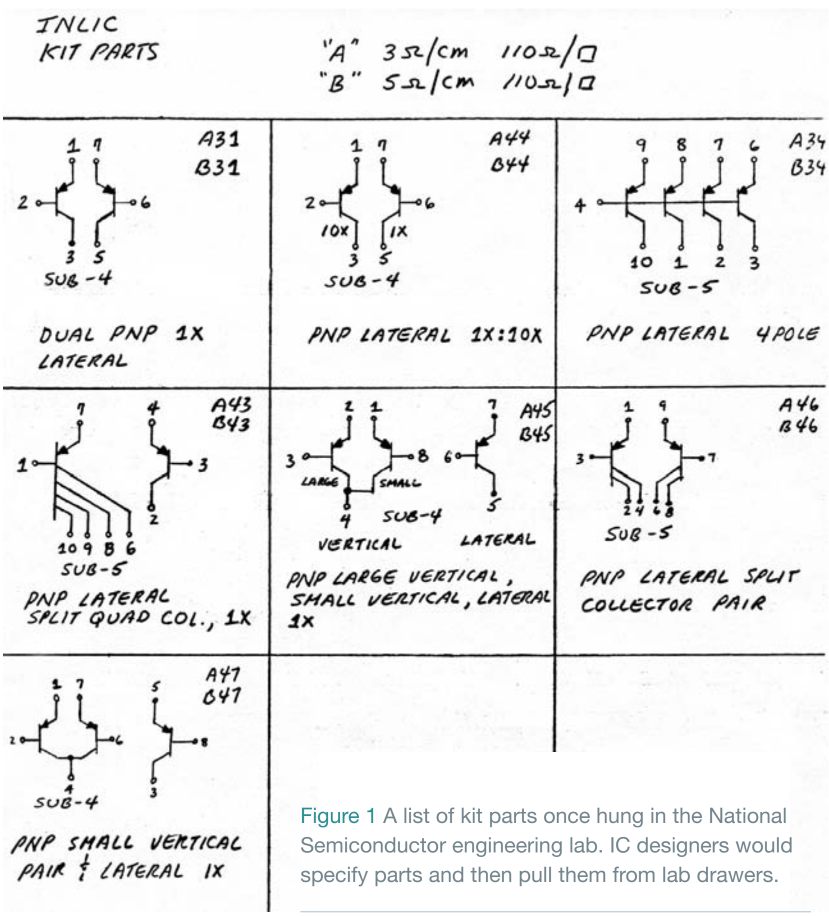


Figure 1 A list of kit parts once hung in the National Semiconductor engineering lab. IC designers would specify parts and then pull them from lab drawers.

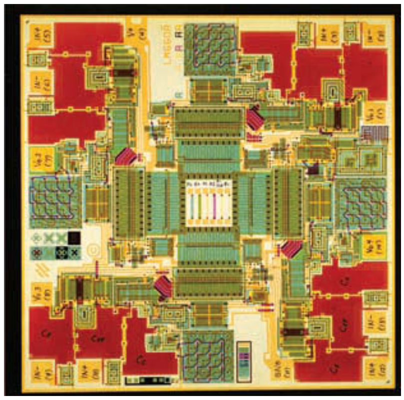


Figure 2 A typical color key was an efficient way to check whether part of the geometry was missing or drawn incorrectly. The first high-performance CMOS op amp, the LMC660, dates back to 1984.

matic] checks were not automatic, and peers used to perform independent, manual LVS checks to verify that the circuit and the layout matched."

Layout tools included a "beer check," during which the designers placed circuit plots onto a light table. "You would invite your peers to the beer check for your IC layout," says Archer. "You would buy them a beer for every mistake they found. We later got a more staid design manager, who insisted we call them layout checks instead of beer checks."

According to Maida, the company also used color keys to compare one layer with another (**Figure 2**). The color keys were printed on Mylar sheets representing one of the physical layers, and each layer was assigned a color, such as red for the base or green for the collector. When the designers stacked the two colors over a light source, they produced a third color. This approach provided an efficient way to check whether a part of the geometry was missing or incorrectly drawn. The designers also developed so-called kludge boxes to verify the performance of the design and sometimes for use in production-test equipment (**Figure 3**).

"Kludge boxes were a necessity in that test equipment did not exist that could measure the performance of the IC," says Moraveji. "These boxes often used some clever measurement tricks, which would also find their way into the data sheet." According to Moraveji, the designers used transistor-kit parts in

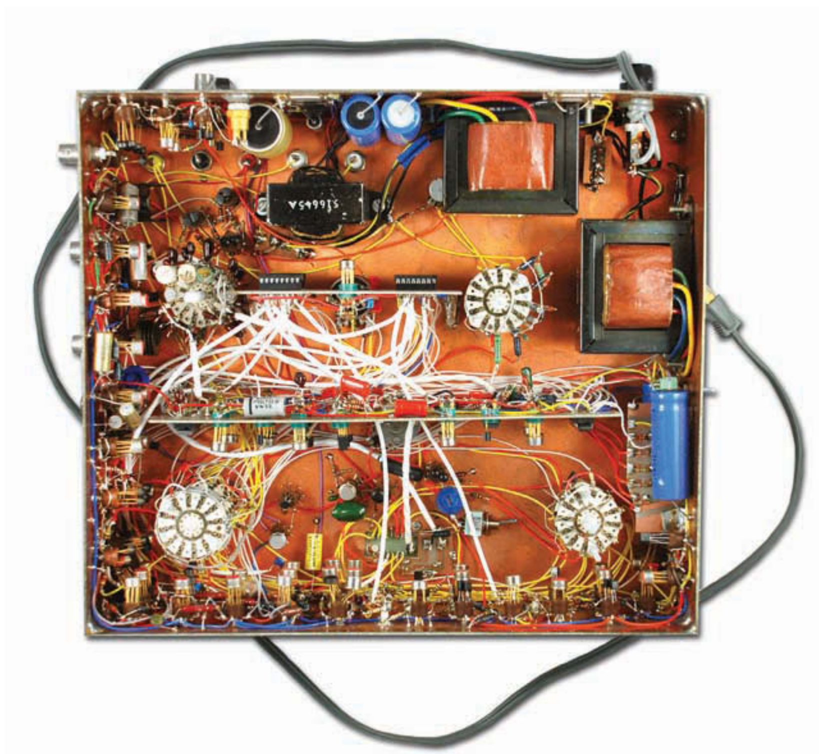


Figure 3 A kludge box for the LM1893 acted as an early test-and-measurement and performance-verification tool.

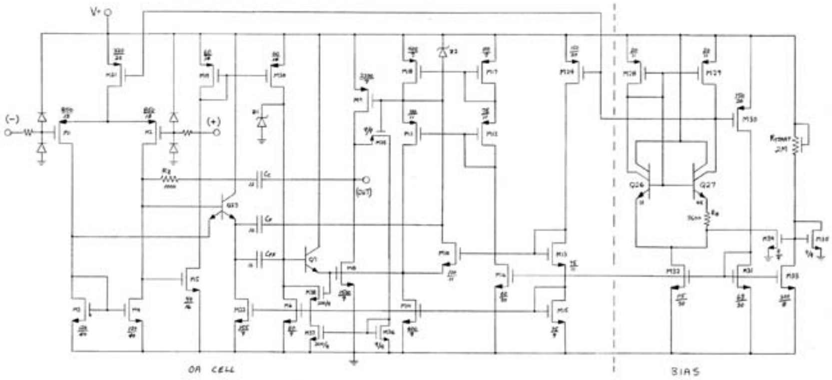


Figure 4 The LMC660 quad CMOS op amp is still selling after almost 30 years in production and has excellent performance, even though it does not contain the thousands of transistors that 21st-century designs contain. TI fellow Dennis Monticelli's name is on the design.

breadboarding a new design idea or to prototype a chip. They performed comprehensive measurements on a breadboard to ensure the validity of a design idea. "Breadboarding was fun, as well as challenging," he says. "During the process, if a component went bad, it was extremely painful to debug and get it to work again. Technicians, who used to do a neat breadboard, were valuable parts of our team in the development phase."

Designers used to be able to get into the transistor-level details and even modify the transistor design to create ICs. Today's designers instead receive standard cells with which to design; they cannot modify them because manufacturing does not support modified designs. In the early days, time to market was less critical than it is now. A 50-transistor circuit—including breadboard design; layout; debugging, which often took place on a probe station; and, typically, some mask changes—would take 18 to 24 months to complete. Now, a period of eight to 10 months is the norm for several-thousand-transistor designs (**Figure 4**).

The designers used simulation tools for validation but first had to perform manual calculations, and developing breadboards was a standard practice until the mid-'80s. Sometimes, they had to use slide rules to make the paper design work before building the breadboard. They also couldn't use many library textbooks because they were developing new designs, especially in CMOS. According to Archer, researching articles in various IEEE journals was often more insightful and useful than using textbooks. And, according to Monticelli, recent engineering-school graduates would try to find a good mentor who used blackboards because there were no whiteboards in those days. You learned by reading the latest published papers and meeting other engineers at the watering holes in Silicon Valley. "In many cases, we had to take a multitude of measurements and then use the data to create an explanation [about] the operation of the circuit," says Dietz.

Moving to plastic-mold compounds caused stress effects that changed low-offset voltages in a chip after the application of the mold. "Sometimes, we would not offer the premium A-grade specs in the plastic package," explains Maida. "The same part often had two or three electrical grades and two or three temperature grades: commercial, industrial, and military." He adds that designers always tested military-temperature-range parts over temperature but almost never tested commercial parts in the same way.

According to Dietz, the op amp served as the canary in the coal mine for uncovering any process problems. The sensitive nature of the tight specs in an analog IC provided warnings when the process started going awry. Designers back then had never heard of the phrase "guaranteed by design." Instead, they "tested the daylights" out of the IC during development. However, Maida claims that this testing was not true for production testing. "Good managers knew what could be put in as a design limit," he says. "The test-everything mentality came in later, toward the late '80s, as [part-per-million] quality levels became important." However, Maida adds, they had to characterize the parts on the bench, which always involved manual measurements and, sometimes, kludge boxes for the tricky measurements, such as settling time, sample-and-hold acquisition time, and linearity.

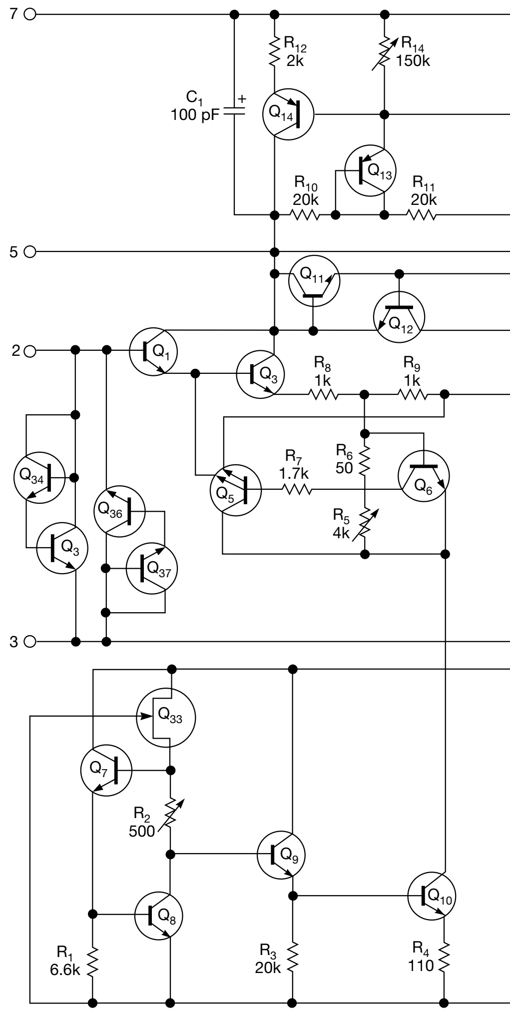
Fast-forward 40 years, and the customer has hundreds if not thousands of op amps and multiple suppliers to choose from, says Dietz. Once engineers get comfortable with an op amp, they tend to use it over and over again. If they need a little better performance, then the chances are that they can find a product that fits the bill. "It is rare that someone comes to us today and asks for a new op amp," he says.

ANALOG-FRONT-END ROLE

Precision op amps are often now parts of the input of integrated analog front ends or integrated into a sensor. Thanks to low output impedance at high frequency, they also drive switched capacitors' input ADCs and have differential outputs at the corrected common-mode level an ADC requires. According to Moraveji, these amplifiers target use in high-dynamic-range ADC-interface applications with low quiescent power, gigahertz-level gain-bandwidth products, and low input noise.

In these modern amplifiers, besides generic specs, such as open-loop gain, supply current, and input offset voltage, other terms, such as third-order intermodulation, represent distortion and SFDR (spurious-free-dynamic-range) degradation distortion at higher frequencies. High-speed digital variable-gain amplifiers now drive ADCs, usually with serial-bus outputs, to interface painlessly with microcontrollers.

Industrial markets still prefer the old standard of using ±15V power supplies. New process technologies can maintain the ±15V power supplies and provide improved performance, lower power, and programmability, according to Maida. Although some of today's designers believe that amplifiers that can operate from 1.8V supplies will save power, these devices can instead burn power to achieve performance specs at this supply voltage. One of the first single-cell-powered op amps was the LM10, which the



late analog pioneer Bob Widlar designed at National Semiconductor in the '70s. This single alkaline-cell-powered op amp was stable because many of its transistors operated at nearly the saturation point, Maida explains.

Designers also want their circuits to drive unlimited capacitive loads, and many designers ask for rail-to-rail performance on the input and the output. Most designs do not require this feature, however. Designers must do a thorough analysis of their circuits' needs to see whether they require rail-to-rail performance to meet the circuits' specs rather than overspecifying their designs. Nevertheless, according to Maida, no one ever lost a job due to overspecifying an op amp. "Ease of use still sells," he says.

Designers must push a design to the process limit but not push it over, so they

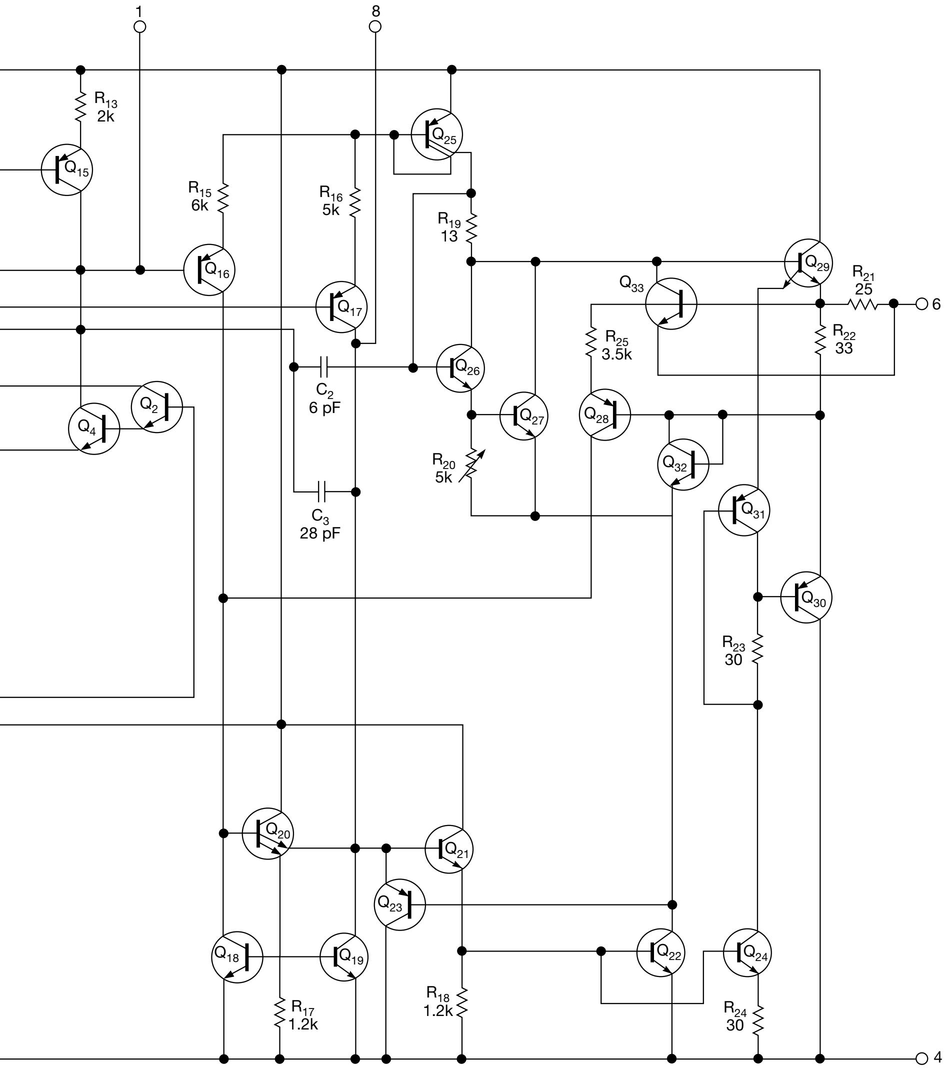
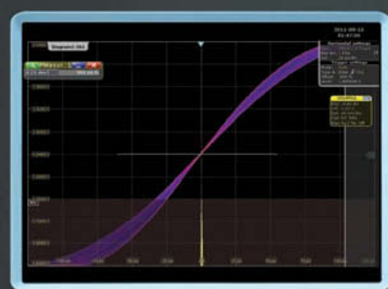


Figure 5 Linear Technology's Bob Dobkin designed the LM318 op amp during his days at National Semiconductor. He employed an architecture that split the input signal into a dc path through the lateral transistors and an ac path with feedforward capacitors that went around the PNP transistors for a 10- to 15-MHz-bandwidth breakthrough.

need to clearly understand the boundaries to get a state-of-the-art design. It's difficult for modern designers to push the limits—often because dice have ever-increasing yield numbers, which are now approximately 90%. IC designers today also must work closely with manufacturing and process teams to achieve the reliable and functional new designs that circuit designers crave. Competent IC designers can work across the boundaries of department functions in modern IC development. They can no longer shoot from the hip because complexities have increased in a process-driven business. Fundamentals remain the same, however, and designers still fight tool issues and push the envelope to get products to customers, says Dietz.

According to Maida, today's engineers must know everything about what is going into the op amp, as well as everything about the load. Data sheets list a large amount of what a design needs, but, he adds, "Nothing beats a good breadboard to take you to the next level of confidence in the design."

"Today's building-block amplifiers are becoming more and more application-specific," says Monticelli. "There



are hundreds—maybe thousands—of product varieties out there from precision to high-speed, but we are seeing more analog front ends, including those that are parts of sensor-interface subsystems. Integration, smaller footprint, and lower power are becoming more prominent today."

Modern op-amp choices from Texas Instruments have evolved to the point at which many products now tout smaller packages; the availability of single, dual, and quad versions; single-supply, low-power, rail-to-rail performance; and ±18V supplies. Such op amps include the company's OPA170 family; zero-drift op amps, such as the OPA180 family with integrated electromagnetic-interference filtering; and low-operating-voltage CMOS op amps, such as the OPA314 family and the chopper-stabilized LMP2015 op amp. These devices represent today's new and creative application-specific architectures and processes.

Bob Dobkin, Linear Technology's co-founder, vice president of engineering, and chief technology officer, spent his early design days at National Semiconductor, during which he moved op amps beyond the 1-MHz-bandwidth barrier with the LM318 (**Figure 5**). No fast PNP transistors then existed; there were only lateral NPNs with 1-MHz bandwidth. Improvements in process technology helped, but the greatest speed gains often resulted from clever topological choices. Dobkin employed an architecture that split the input signal into a dc path through the lateral transistors and an ac path with feed-forward capacitors that went around the PNP transistors for the 10- to 15-MHz-bandwidth breakthrough. "We were limited to a maximum of eight to 10 mask layers to meet good yields," Dobkin says.

Using too many masks yielded too many defects and, hence, poor yield. The company implemented PCB masks, according to Dobkin—"sometimes with a silk stocking!" New processes now have 20 to 30 mask layers and still get good yields. The availability of masks allowed the development of fully complementary processes using PNP and NPN transistors. Designers can now create amplifiers with hundreds of megahertz of bandwidth because special architectures are no longer necessary for achieving high bandwidth.

Linear Technology's offerings in the 21st century include the differential-output, low-power, rail-to-rail, high-speed, successive-approximation-register LTC6362 ADC driver; the high-integration LT6108, which incorporates a precision current-sense amplifier, a voltage reference, and a comparator; and the 500-mA LT1970A power op amp with adjustable precision current limit. EDN

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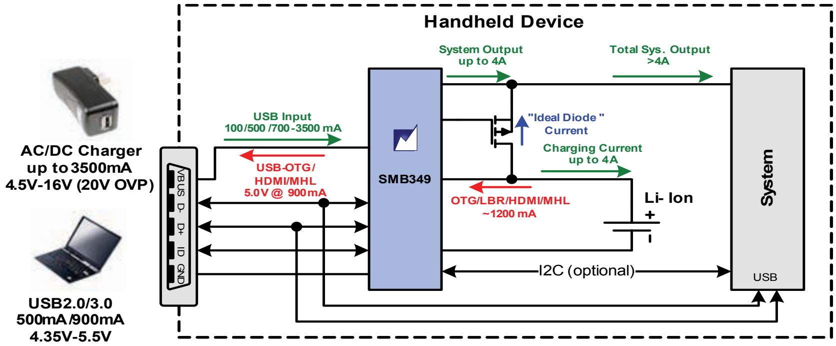

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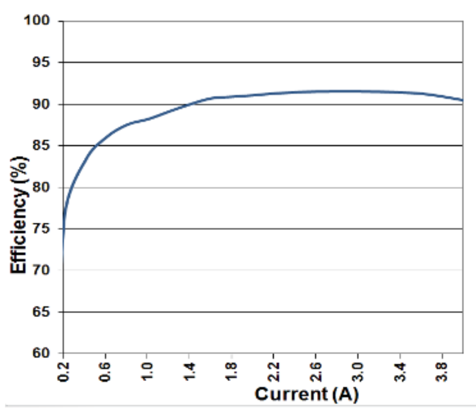

	SMB349	SMB359	SMB347	SMB137C	SMB346	SMB136C
Input Voltage Range (V)*	4.35 to 16 (20)	4.35 to 16 (20)	4.35 to 6.2 (20)	4.35 to 6.0 (18)	4.35 to 6.2 (20)	4.35 to 6.0 (18)
# of Inputs/Outputs	1/2	1/1	2/2	2/2	2/2	1/2
Maximum Charge Current (mA)	4000	4000	2500	1500	1250	1500
Maximum Input Current (mA)	3500	3500	2500	1500	2500	1500
CurrentPath™ Control	√		√	√	√	√
Charge Current Voltage Output	√	√	√		√	
Low-Battery Recovery Mode				√		√
Automatic Power Source Detection **	rev 1.2	rev 1.2	rev 1.1/1.2	rev 1.2	rev 1.1/1.2	rev 1.2
Package	3.2x3.0 CSP-49 5x5 QFN-40	3.2x3.0 CSP-49 5x5 QFN-40	3.0x2.5 CSP-30	3.0x2.5 CSP-30	3.0x2.5 CSP-30	3.0x2.5 CSP-30
Solution Size (mm2)	52	52	32	38	32	35

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Coupling a supercapacitor with a small energy-harvesting source

SUPERCAPACITORS STORE ENERGY AND DELIVER PEAK POWER IN SUPPORT OF ENERGY HARVESTERS. DESIGNERS SHOULD CONSIDER SEVERAL KEY ISSUES WHEN PAIRING THEM WITH SMALL ENERGY-HARVESTING SOURCES.

Small wireless sensors are becoming ubiquitous. Applications for sensors include building control, industrial control, security, location tracking, and RFID. It is much more convenient and cost-effective to autonomously power these sensors with a small energy-harvesting source without expensive wires or batteries that need repeated replacement.

The environment provides infinite ambient energy, including piezoelectric, thermal, vibration, and photovoltaic energy, but at low power, which falls short of the peak power necessary for transmitting data across wireless networks such as IEEE 802.15.4 (Zigbee), 802.11 (WLAN), or GSM/GPRS. A battery or a supercapacitor acts as a power buffer to store enough energy to provide the power bursts needed to acquire and transmit data. These energy-storage devices charge at low power and deliver the burst power when necessary.

SIZING THE SUPERCAPACITOR

Supercapacitor cells typically operate at 2.3 to 2.8V. The most efficient and cost-effective strategy is to limit the supercapacitor's charge voltage to less than the cell-rated voltage and store enough energy for your application.

A simple approach to sizing the supercapacitor is to calculate the energy necessary to support the peak power of the application, P, and set this value equal to $\frac{1}{2}C(V^2_{INITIAL}-V^2_{FINAL})$, where C is the capacitance, $V^2_{INITIAL}$ is the square of the supercapacitor's voltage just before the peak-power burst, and V^2_{FINAL} is the square of the final voltage. However, this **equation** does not allow for any losses in the supercapacitor's ESR (equivalent series resistance). The load sees a voltage of $V_{INITIAL}-ESR\times I_{LOAD}$, where I_{LOAD} is the load current. Because the load voltage decreases, the load current increases to achieve the load power. Referring to **Figure 1**, designers can model supercapacitor discharge as

$$V_{LOAD}=V_{SCAP}-I_{LOAD}\times ESR;$$
$$P_{LOAD}=V_{LOAD}\times I_{LOAD}=(V_{SCAP}-I_{LOAD}\times ESR)\times I_{LOAD}$$
$$=V_{SCAP}\times I_{LOAD}-I_{LOAD}^2\times ESR,$$

where V_{SCAP} is the supercapacitor's voltage.

This **equation** yields the **equation** for the load current:

$$I_{LOAD}^2\times ESR-V_{SCAP}\times I_{LOAD}+P=0.$$

Supercapacitor discharge can then be simply modeled in Excel as

$$I_{LOAD}(t)=[V_{SCAP}(t)-\sqrt{(V_{SCAP}(t)^2-4\times ESR\times P)}]/(2\times ESR);$$
$$V_{LOAD}(t)=V_{SCAP}(t)-I_{LOAD}(t)\times ESR; \text{ and}$$
$$V_{SCAP}(t+dt)=V_{SCAP}(t)-dt\times I_{LOAD}/C.$$

This calculation is important if the load current times ESR is significant compared with the supercapacitor's final voltage. In this case, a simple energy-balance approach would make the supercapacitor's value too small. This undersizing is likely to be the case at low temperatures, when ESR is typically two to three times higher than at room temperature.

The supercapacitor capacitance and ESR should also allow for aging. Supercapacitors slowly lose capacitance and increase ESR over time. The aging rate depends on cell voltage and temperature. Designers should select initial capacitance and ESR so that the end-of-life capacitance and ESR can support the applications.

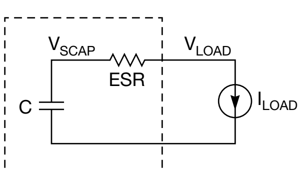

Figure 1 Ideal supercapacitor model; capacitance in series with ESR.

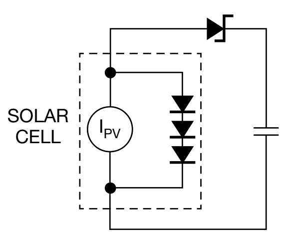

Figure 2 This simple and effective charging circuit targets use in cases in which the open-circuit voltage of a solar-cell array is less than the supercapacitor's rated voltage.

SUPERCAPACITOR CHARGING

A discharged supercapacitor looks like a short circuit to an energy source. Fortunately, many energy-harvesting sources, such as solar cells and microgenerators, can drive into a short circuit and directly charge a supercapacitor from 0V. ICs to interface energy sources, such as piezoelectric or thermoelectric energy, must be able to drive into a short circuit to charge a supercapacitor.

The industry has invested much effort in MPPT (maximum-peak-power tracking) to most efficiently draw power from energy-harvesting sources. This approach is applicable when charging a battery that must charge at constant voltage. The battery charger is typically a dc/dc converter that is a constant-power load to the energy source, so it makes sense to draw that power at the most efficient point using MPPT.

In contrast to a battery, a supercapacitor need not charge at a constant voltage but charges most efficiently by drawing the maximum current the source can supply. **Figure 2** shows a simple and effective charging circuit for cases in which the open-circuit voltage of a solar-cell array is less than the supercapacitor's rated voltage. The diode prevents the supercapacitor from discharging back through the solar cell if it goes dark. If the energy source's open-circuit voltage is greater than the supercapacitor's voltage, then the supercapacitor requires overvoltage protection using a shunt regulator (**Figure 3**). A shunt regulator is an inexpensive and simple approach to overvoltage protection, and, once the supercapacitor fully charges, it does not matter whether the excess energy dissipates.

The energy harvester is like a hose with an endless supply of water filling a barrel, which is analogous to a supercapacitor. If the hose is still running once the barrel is full, the water may overflow. This situation differs from that of a battery, which has a limited energy supply and thus would require a series regulator.

In the circuit in **Figure 2**, the supercapacitor, at 0V, draws short-circuit current from a solar cell. As the supercapacitor charges, the current decreases, depending on the solar cell's voltage/current characteristic. The supercapacitor always draws the maximum current it can, however, so it charges at the highest possible rate. The circuit in **Figure 3** uses the TLV3011 solar cell because it integrates a voltage reference, draws only approximately 3-μA quiescent current, and is an open-drain cell so that the output is open-circuit when the regulator is off. This circuit uses the BAT54 diode because it has a low forward voltage at low currents—that is, the forward voltage is less than 0.1V at a forward current of less than 10 μA.

Microgenerators are ideal for industrial-control applications, such as monitoring rotating machinery, because by definition they will vibrate when they are operating. **Figure 4** shows the voltage-current characteristic of a microgenerator, which is similar to that of a solar cell and which delivers maximum current into a short circuit. A microgenerator also includes a diode bridge, which prevents the supercapacitor from discharging back into the generator, leading to a simple charging circuit (**Figure 5**).

The open-circuit voltage is 8.5V, requiring a dual-cell supercapacitor, such as the CAP-XX HZ202, which operates at 5.5V. A shunt regulator provides overvoltage protection, and a low-current active-balance circuit ensures even distribution between the cells. Linear Technology, with its LT3652, LTC3108, and

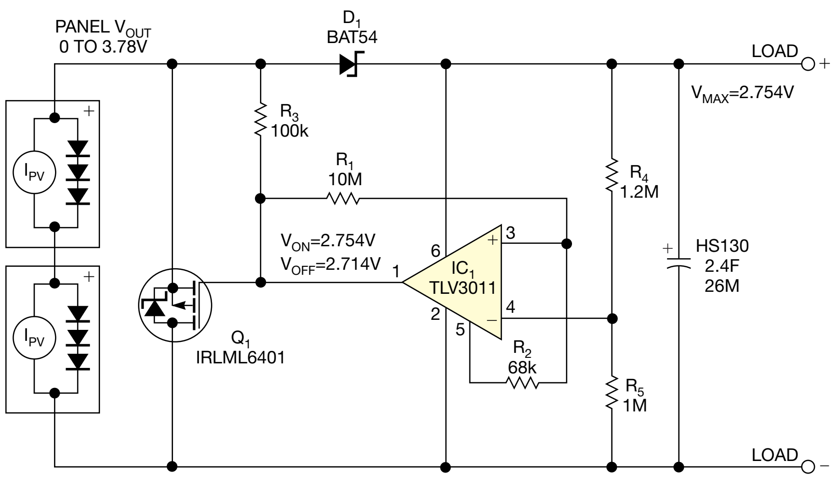

Figure 3 If the energy source's open-circuit voltage is greater than the supercapacitor's voltage, then the supercapacitor requires overvoltage protection using a shunt regulator.

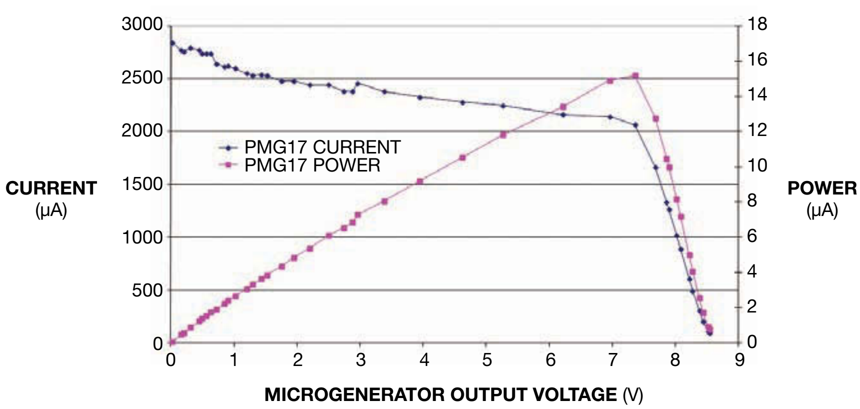

Figure 4 The voltage-current characteristic of a microgenerator is similar to that of a solar cell and delivers maximum current into a short circuit.

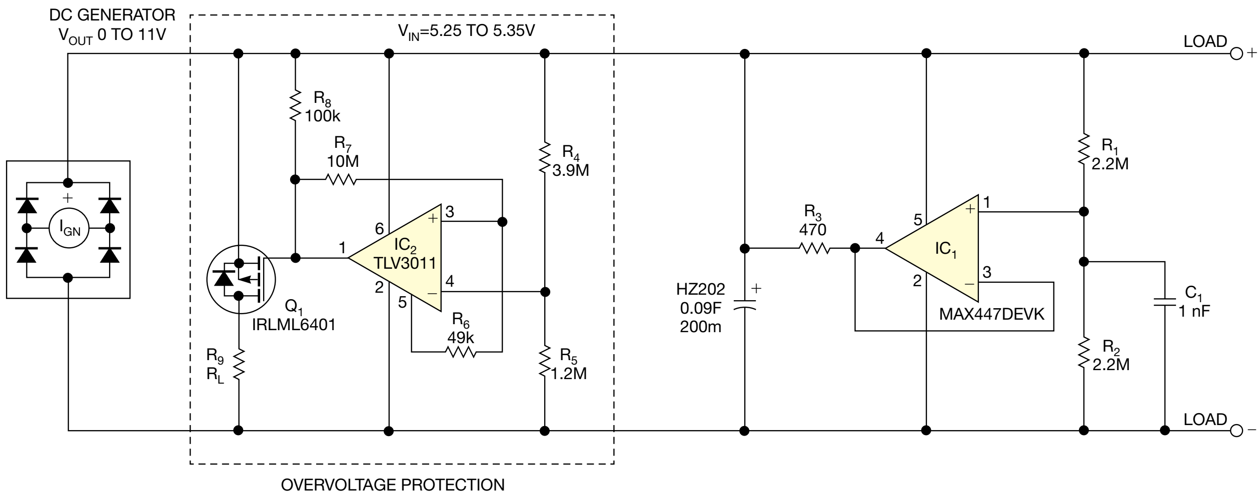

Figure 5 A microgenerator includes a diode bridge, which prevents the supercapacitor from discharging back into the generator, leading to a simple charging circuit.

LTC3625 ICs, and Texas Instruments, with its BQ25504, charge supercapacitors from energy-harvesting sources.

LEAKAGE CURRENT

Because some energy harvesters deliver only a few microamps, leakage current becomes important. Supercapacitors can have leakage currents of less than 1 μA, making them suitable for energy-harvesting applications (**Figure 6**).

When a supercapacitor charges, the leakage current decays over time as the ions in the carbon electrodes diffuse into the pores. The leakage current settles to an equilibrium value, which depends on capacitance, voltage, and time. Leakage current is proportional to cell capacitance. A rule of thumb for equilibrium-leakage-current supercapacitors at room temperature is 1 μA/F. The 150-mF capacitors in **Figure 6** have leakage currents of 0.2 and 0.3 μA after 160 hours. Leakage current increases exponentially with temperature. The time it takes to settle to the equilibrium value decreases with increased temperature as the ions diffuse more rapidly. Thus, these capacitors require a minimum current to charge from 0V. Depending on the supercapacitor, this current ranges from 5 to 50 μA. Designers should consider testing the minimum charging current when selecting a supercapacitor for an energy-harvesting circuit.

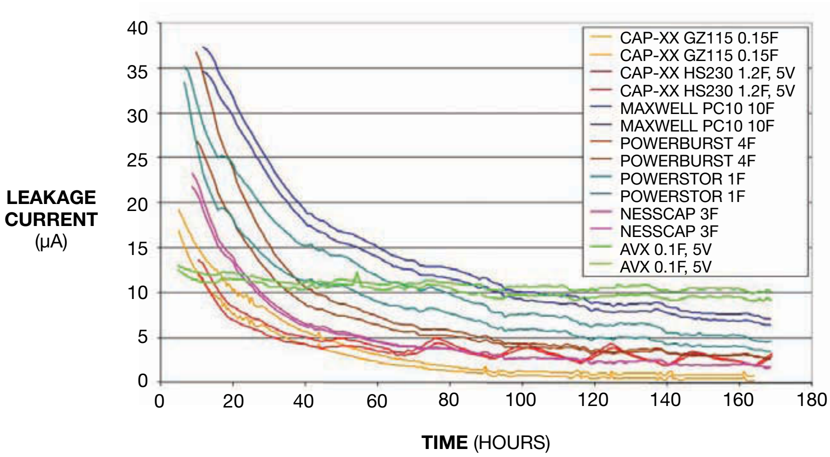

Figure 6 A rule of thumb for equilibrium-leakage-current CAP-XX supercapacitors at room temperature is 1 μA/F.

CELL BALANCING

Circuits requiring that the supercapacitor's terminal voltage is greater than the cell-rated voltage require several supercapacitor cells in series to reach the rated voltage, such as 5V or 12V. In this case, a cell-balancing circuit is necessary; otherwise, one of the cells could go into an overvoltage condition because the cells all have slightly different leakage currents, with different voltage-to-leakage-current characteristics. Because they are in series, however, they must all have the same leakage current. To achieve this goal, the cells redistribute charge among themselves; in doing so, one cell may go into an overvoltage state. Cells at varying temperatures or aging over time at different rates can exacerbate this problem. The simplest balancing circuit is a resistor in parallel across each cell. Depending on the leakage current of the supercapacitor and the operating temperature, the resistor's value typically ranges from 1 to 50 kΩ, but the leakage current through the balancing circuit is too high for

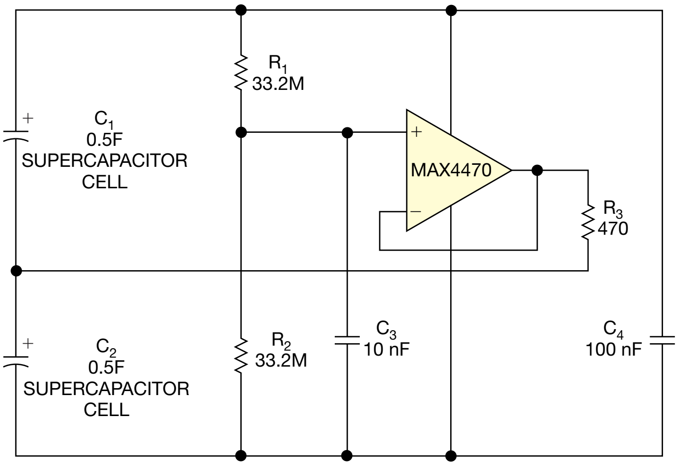

Figure 7 Low-current active-balance circuits target use in energy-harvesting applications.

most energy-harvesting applications. A better approach for energy-harvesting applications is to use a low-current active-balance circuit (**Figure 7**).

The MAX4470 op amp in the **figure** has a supply current of 750 nA and a rail-to-rail input and output. R_3 limits the output current in the event that one cell causes a short circuit. The resulting design draws 2 to 3 μA after 160 hours of balancing a 0.5F CAP-XX HW207 supercapacitor (**Figure 8**). To suit a log scale, the absolute value of cell-balancing current can be positive or negative.

TEMPERATURE PERFORMANCE

A major advantage of supercapacitors for energy-harvesting applications is their wide temperature performance. Examples include powering location-tracking units using vibration transducers, which may be operating in subzero temperatures, or solar panels in winter sunlight. Supercapacitor ESR at –30°C is typically two to three times ESR at room temperature, so the device can still deliver peak power even at low temperatures. In contrast, the internal impedance of thin-film batteries may reach several kilohms at such low temperatures.

COMPLEMENTING BATTERIES

In some applications, supercapacitors are alternatives to batteries; in others, they support them. In some situations, a supercapacitor may be unable to store sufficient energy, necessitating the use of a battery. For example, when the ambient-energy source—the sun, for example—is intermittent, as it would be at night, then the device must store energy not just for peak-power delivery but also to support the application for an extended time. If the needed peak power exceeds the amount the battery can supply—for GSM calls or low-power transmission in cold temperatures, for example—then the battery can charge the supercapacitor at low power, and the supercapacitor can deliver the high power bursts. This arrangement also means that the battery never cycles deeply, extending battery life. Supercapacitors store energy by physical-charge storage, not chemically as in batteries, so supercapacitors have an effectively infinite cycle life.

When a supercapacitor charges from a battery to supply peak-power bursts, there is a critical interval between bursts where if the bursts arrive more often, then it is more energy-efficient to always leave the supercapacitor on charge. If the bursts arrive less often, however, it is more energy-efficient to charge the supercapacitor just before the peak-power event. This interval depends on several factors, including the charge that the supercapacitor absorbs before reaching equilibrium leakage current, the self-discharge characteristic of the supercapacitor, and the charge the circuit draws from the supercapacitor to supply the peak-power event. This choice is available only if you know beforehand when the peak-power event will occur, and that is not possible if it is in response to an unpredictable event, such as battery failure or an external stimulus. EDN

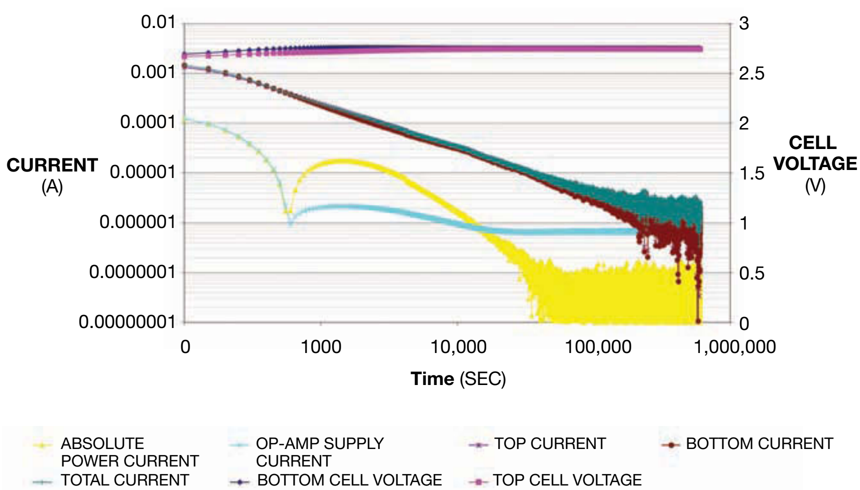

Figure 8 This design draws 2 to 3 μA after 160 hours of balancing a 0.5F CAP-XX HW207 supercapacitor.

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BY DANIEL PRUESSNER • FAIRCHILD SEMICONDUCTOR

When the power fails: designing for a smart meter's last gasp

POWER-SUPPLY DESIGNERS HAVE SOME OPTIONS FOR COST-EFFECTIVELY PROVIDING ENERGY AFTER POWER LOSS.

Smart-meter designers have an unusual predicament: The meter receives its power from the same bus that the meter is monitoring. When the meter loses power, it must record state information to flash memory or send out a wireless signal—the meter's "last gasp." Some utilities also disconnect subscribers from the grid during power outages to minimize the inrush demands when power is ultimately restored. Disconnecting a subscriber after loss of power also requires stored energy in either electrical or mechanical form.

The problem of efficiently and cost-effectively providing holdup energy typically falls to power-supply designers, who have various options for solving this problem. Here we evaluate the benefits and costs of these options in a flyback switch-mode power supply.

Figure 1 shows a basic offline flyback circuit. The supply accepts 85 to 265V ac and generates a 3.3V-dc, 5W output. The holdup requirement of the load is 50% power, or 2.5W, for 0.5 sec, or 1.25J. The **figure** highlights three sections for energy storage. Option A stores the holdup energy in the high-voltage capacitor, C_{BUS}. Option B stores the energy in a 20V intermediate-voltage capacitor with a downstream dc/dc buck regulator that steps down the voltage to the load's working voltage at 3.3V. Option C is simpler and stores energy in a large capacitor at the output.

ELECTRIC-POTENTIAL ENERGY

Because all of the options involve storing energy as electric potential in a capacitor, you should review the relationship of voltage, capacitance, and potential energy, as the following **equation** shows:

$$U_E=\frac{1}{2}CV^2,$$

where U_E is potential energy, C is capacitance, and V is voltage. The following **equation** calculates a change in the potential energy for a given change in the voltage across the capacitor:

$$\Delta U_E=\frac{C(V_F^2-V_0^2)}{2},$$

where V_F is the final voltage and V_0 is the initial voltage. The following **equation** shows the change in voltage for a given change in potential energy:

$$\Delta V=\sqrt{\frac{2}{C}}\times(\sqrt{U_F}-\sqrt{U_0}),$$

where U_F and U_0 are the final and initial potential energy, respectively.

PRIMARY-SIDE CAPACITANCE

The first option is to increase the capacitance of the high-voltage bulk electrolytic capacitor, C_{BUS}, on the primary side. This capacitor typically stores just enough energy to continue power conversion during the ac cycle valleys—in this case, 1/120 sec, or 8.3 msec, for a full-wave rectified input. When voltage from the line disappears, the converter continues to run and consume energy from C_{BUS}. The voltage on C_{BUS} eventually reaches a point at which the voltage cannot ramp sufficient current through the primary-side inductor to sustain

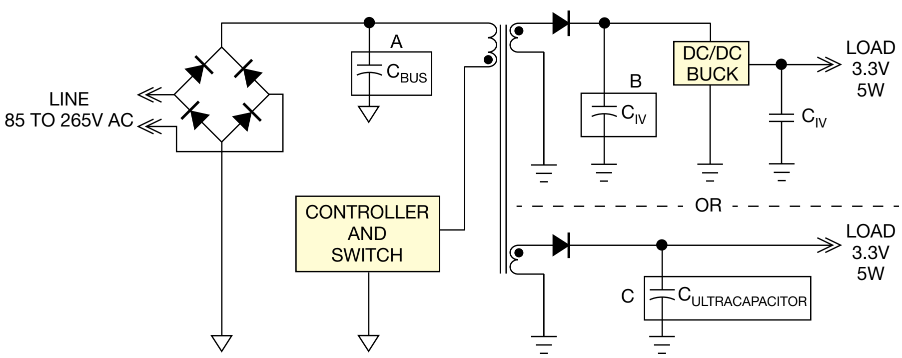


Figure 1 In a basic flyback circuit, Option A stores the holdup energy in the high-voltage capacitor, C_{BUS}. Option B stores the energy in a 20V intermediate-voltage capacitor with a downstream dc/dc buck regulator that steps down the voltage to the load's working voltage at 3.3V. Option C is simpler and stores energy in a large capacitor at the output.

the output. The voltage on the auxiliary output, from which the controller draws its power, also drops to the controller's undervoltage-lockout level. After this drop, the controller shuts off, and the output falls to 0V (**Figure 2**).

The supply must hold up the output under all conditions, so we will focus on the worst case: when source power disconnects shortly after the ac zero-crossing at low line input. Because the supply draws half-power during holdup, the supply operates normally. It has enough voltage to impose across the inductor to reach the required primary-side peak current—down to 70% of the minimum input voltage requirement. You can therefore estimate that the supply can operate down to 70V on C_{BUS}. Solve for the capacitance to provide the 1.25J of holdup energy and set V_0 to the minimum rectified ac line voltage because the bus-ripple voltage is negligible when the bulk capacitance is large:

$$C_{REQ}=\frac{2\times\Delta U_E}{V_0^2-V_F^2}=510\ \mu F.$$

This capacitance is large, and these capacitors must have a minimum voltage of 400V. One benefit of using the primary side is that it can store a large amount of energy if the minimum line voltage is fairly high. For instance, if the minimum line voltage were 190V ac, then the same holdup would require only 68F. **Figure 3** shows the holdup-time curve for this supply.

Storing energy in the primary side can be expensive. Large-value, high-voltage capacitors can get pricey, and the leakage current through them increases with voltage and value. Most designs try to minimize the primary-side loop to minimize electromagnetic-compliance problems. Using capacitors with diameters of 30 mm may make this task difficult.

You must also take into consideration the efficiency of the power supply. Energy stored in the primary side must be processed through the converter, which includes the switch, the inductor, and the secondary-side diodes, and the efficiency of the converter will decrease this energy. Many flyback converters are 75 to 85% efficient, so the primary-side energy must increase by 20%.

INTERMEDIATE VOLTAGE

Option B involves adding a secondary dc/dc regulator on the isolated side of the supply. A synchronous buck regulator fulfills this function with minimal parts. Several available products integrate the controller with high- and low-side switches and drivers. The buck regulator would operate at a higher frequency than the flyback converter and would provide lower voltage ripple to the load.

Holdup energy is stored at an intermediate voltage on the secondary side. The regulated secondary side provides a less varied quantity of stored energy—in contrast with storing energy in the primary side, in which the line voltage may vary and the holdup energy varies with the line voltage squared. The energy storage in the secondary capacitor is straightforward:

$$U_E=\frac{1}{2}\times C_{IV}(V_{IV}^2-V_{OUT}^2),$$

where C_{IV} is the intermediate-voltage capacitance feeding the dc/dc converter and V_{IV} is the intermediate voltage.

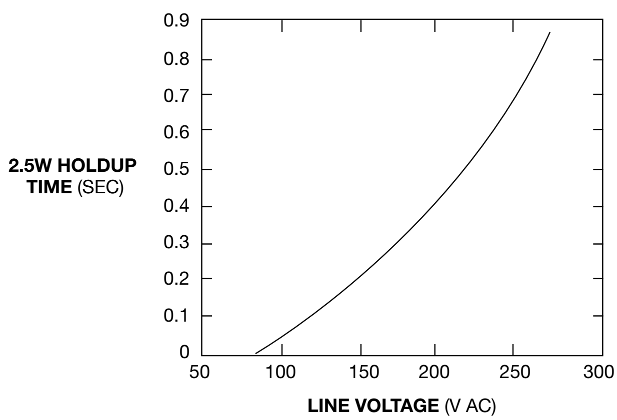


Figure 3 One benefit of storing energy in the primary side is that it can store a large amount of energy if the minimum line voltage is fairly high. For instance, if the minimum line voltage were 190V ac, then the same holdup would require only 68F, which is more manageable, as this curve shows.

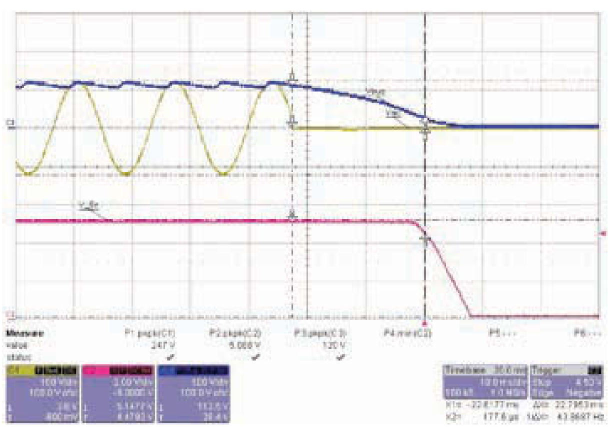


Figure 2 The voltage on the auxiliary output, from which the controller draws its power, also drops to the controller's undervoltage-lockout level. After this drop, the controller shuts off, and the output falls to 0V.

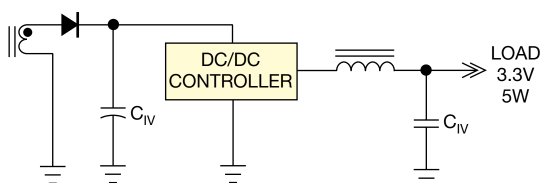


Figure 4 Because of the significantly reduced current and, therefore, current ripple, you can size C_{IV} based on the holdup-energy requirement, and it will have an insignificant amount of heating.

TABLE 1 PARTS AND COST COMPARISON

Option	Parts	Price (10,000)
Primary side	400V, 560-μF capacitor (minus 20 cents of the 10 μF needed for other designs)	$3.26
Intermediate voltage	1600-μF capacitor, FAN2103 dc/dc, 10-μH inductor	$2.04
Supercapacitor	2x2F, 2.4V supercapacitor	$3.12

In flyback designs, current flows through the secondary of the transformer only during part of the switching cycle, meaning that the output-current ripple is large on an rms-versus-dc basis, and it is up to the output capacitor to smooth the time-varying current into dc. Designers must rate capacitors for the effective-series-resistance-caused heating, which impedes the current ripple. This requirement can frequently lead to oversizing the output capacitors to meet end-product lifetime or mean-time-between-failure goals.

With the secondary regulator, the current draw from the intermediate voltage is a fraction of the load current. For this example, with a V_{IV} of 20V, a full-load dc draw of 1.52A would draw 0.25A from the 20V rail. Because of the significantly reduced current and, therefore, current ripple, you can size C_{IV} based on the holdup-energy requirement, and it will have an insignificant amount of heating. **Figure 4** shows the extra components for the secondary regulator.

A secondary-side regulator provides lower voltage ripple than does a standard flyback output. The additional parts will add to bill-of-materials or PCB-space costs; however, you can source these parts as SMD components. The regulated intermediate voltage will provide a more reliable minimum and maximum holdup time than that of primary-side energy storage.

SUPERCAPACITOR

The final option is to store energy directly in the load capacitors. Supercapacitors are dense in both capacitance per volume and capacitance per dollar. This feature makes them well-suited for storing holdup energy directly at the output. Many supercapacitors have voltage of only 2.3 to 4V. Storage of 1.25J at 3.3V requires approximately 1.1F of capacitance. This amount holds the output within 10% for 0.5 sec.

At boot-up, the capacitors look like a short circuit on the output. Many modern flyback controllers have built-in overload and short-circuit protection. These features will need to be slowed down for the supply to boot properly. Unfortunately, this slowdown combined with the increased output capacitance will greatly reduce the bandwidth of the supply feedback and will reduce transient response performance.

Because the output is regulated, this option also has reliable minimum and maximum holdup times. Booting into a large capacitance can pose a challenge for protection features and for sequencing with other supplies in the meter.

Each option for storing energy requires extra or specialized parts. **Table 1** shows the parts and cost comparison for each option.

Storing energy in the primary side is the simplest way to increase holdup time; however, it is the weakest approach, with the holdup time varying more than 1-to-100 across the line range. Storing energy in the output capacitors is also fairly straightforward, provided that the application can accommodate the relaxed protection features. The supply requires slower overload and short-circuit protection to boot up into the large output capacitance. Storing energy in an intermediate voltage is the most complicated approach. It requires the design of an additional power train. However, the benefits are significant: The supply is responsive, has a well-defined holdup time, and is 30% cheaper than the other storage options. EDN

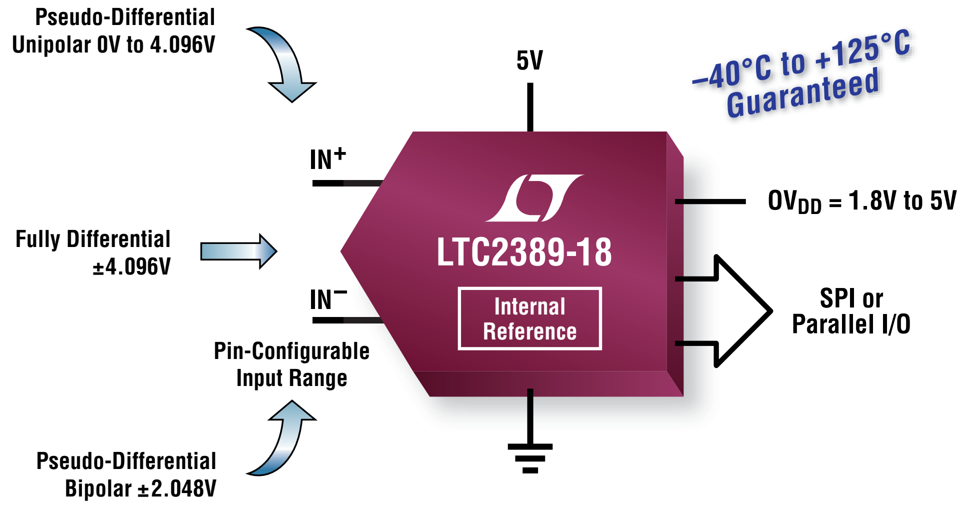
ACKNOWLEDGMENT

This article originally appeared on EDN's *sister site*, SmartEnergy Designline, *http://bit.ly/xgbUuY.*

AUTHOR'S BIOGRAPHY

Daniel Pruessner received a bachelor's degree in electrical engineering from the University of Texas at Dallas. He worked in power transmission and distribution at Dow Chemical before joining Fairchild Semiconductor in 2009. Pruessner is a part of Fairchild's Americas Global Power Resource Lab. He designs offline-switch-mode power supplies for smart-meter, lighting, and consumer-electronics applications.

18-Bit 2.5Msps SAR ADC 100dB SNR



All-in-One ADC with Configurable Input Ranges and Digital I/O

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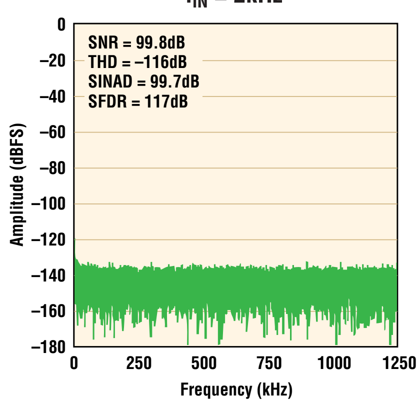
16-Bit 96dB SNR	2389-16
Power Consumption	162.5mW

32k Point FFT f_{SMPL} = 2.5Msps, f_{IN} = 2kHz



Features

- 2.5Msps Throughput Rate
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- ±3LSB INL (max), ±0.9LSB DNL (max)
- Pin-Configurable Analog Input Range:
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LINEAR TECHNOLOGY

Design an ultra-low-noise S-band amplifier

Korkut Yegin, Yeditepe University, Istanbul, Turkey

Engineers often perceive RF-low-noise-amplifier design as a difficult task. Obtaining a low-noise figure with high stable gain can be challenging—even intimidating. However, with the recent evolution of GaAs (gallium-arsenide) heterojunction FETs, you can design amplifiers with a less-than-1-dB noise figure and high stable gain (**Reference 1**). This Design Idea describes a low-noise amplifier with a 0.77-dB noise figure.

Manufacturers usually specify low-noise amps' input/output matching, noise figure, gain, stability, 1-dB compression point, second- and third-order intermodulation products, out-of-band rejection, and reverse isolation. Many of these parameters depend on each other, so it can become complicated to satisfy all of these design criteria in a timely manner (**references 2** and **3**). **Figure 1** shows a flexible amplifier structure that satisfies all of these design criteria.

The design was created and simulated using Microwave Office AWR. NEC's NE3509M04 GaAs HJFET (heterojunction field-effect transistor) acts as the low-noise, high-gain transistor. The reactively matched amplifier input provides low noise and high gain using the optimum reflection coefficient value that the data sheet provides. Active biasing and bootstrapping are common design practices for FETs to prevent variations in drain-to-source current especially over temperature. However, this design implements a small, cost-effective, self-biasing circuit that adds no complexity to the circuit. The biasing point for the transistor is a drain-to-source voltage of 2V, and the drain current is 15 mA, at which the transistor produces an acceptable RF gain of approximately 16.5 dB.

Another design goal for the circuit is the unconditional stability of the low-noise amp. Internal feedback of the transistor and excessive gain at the out-of-band frequencies are the primary causes of instability for this type of circuit. The design uses S parameters from the manufacturer to analyze stability. Although the L_1, R_1, and C_2 branch maintains low-frequency dc-to-video-frequency stability for the HJFET, the combination presents as an open circuit to S-band operation and aids in the noise match of the transistor. C_5, C_8, C_9, and L_3

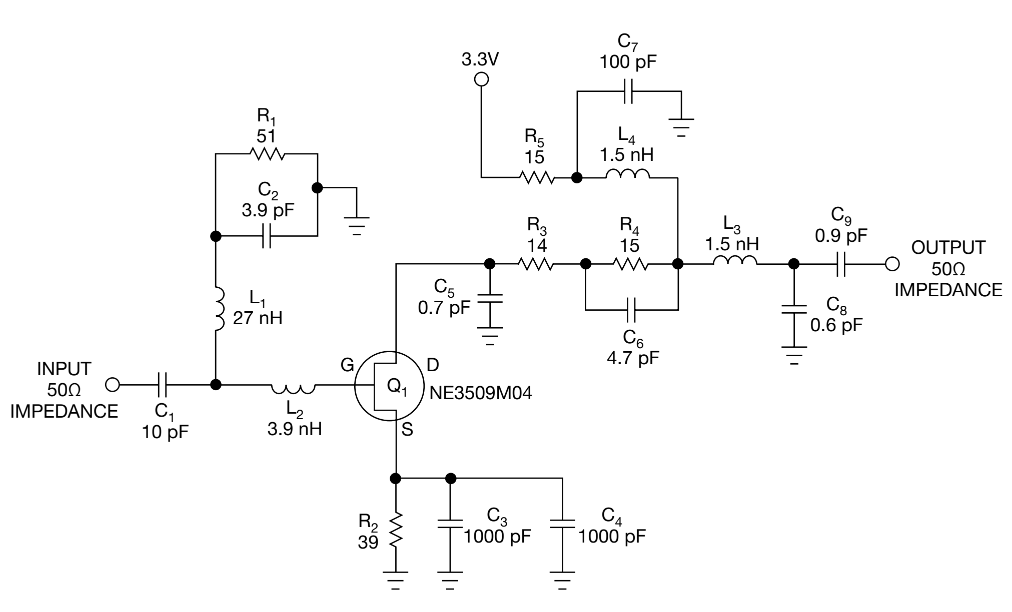

Figure 1 You can design a low-noise S-band RF amplifier with a GaAs heterojunction FET.

▸To see and comment on all of *EDN*'s Design Ideas, visit www.edn.com/designideas.

primarily achieve the output's reactive matching and higher frequency stability. Capacitor C_6 essentially shorts the bias resistor on the drain line without limiting the maximum stable gain. R_3 on the bias line maintains the stability of the amplifier. Shunt capacitor C_5 also sinks high-frequency components and harmonics at the drain to ground. The ground vias at the source terminal create a small inductance for inductive degeneration of the amplifier for a good noise match.

Figure 2 shows a two-stage amplifier with a bandpass filter between the amplifier stages. The developers manufactured the design on a standard four-layer, 62-mil-thick FR4 substrate. Unlike cost-effective, two-layer designs, this design uses additional layers for dc routing and passive antenna isolation from high-gain-amplifier stages to prevent any potential signal leakage and feedback that may cause amplifier instabilities. The resulting structure achieves a 0.77-dB noise figure at room temperature, 28.5-dB gain, −16-dBm input power at 1-dB compression, and a −5.8-dBm third-order-intercept point. The output voltage-standing-wave ratio is 1.3-to-1. You can increase the third-order-intercept level by increasing the drain bias current at the expense of an increased noise figure.

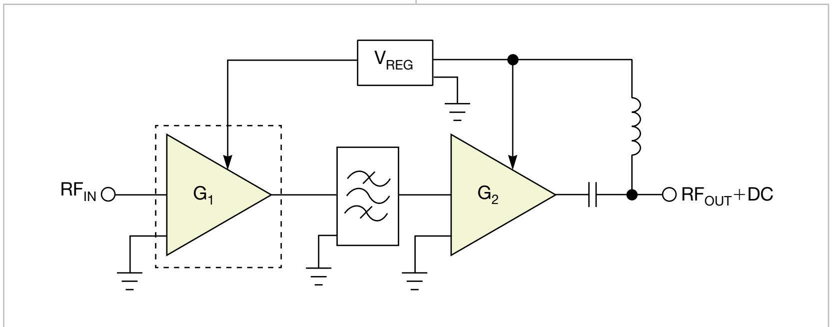

Figure 2 The bandpass filter between two amplifiers rejects out-of-band frequencies.

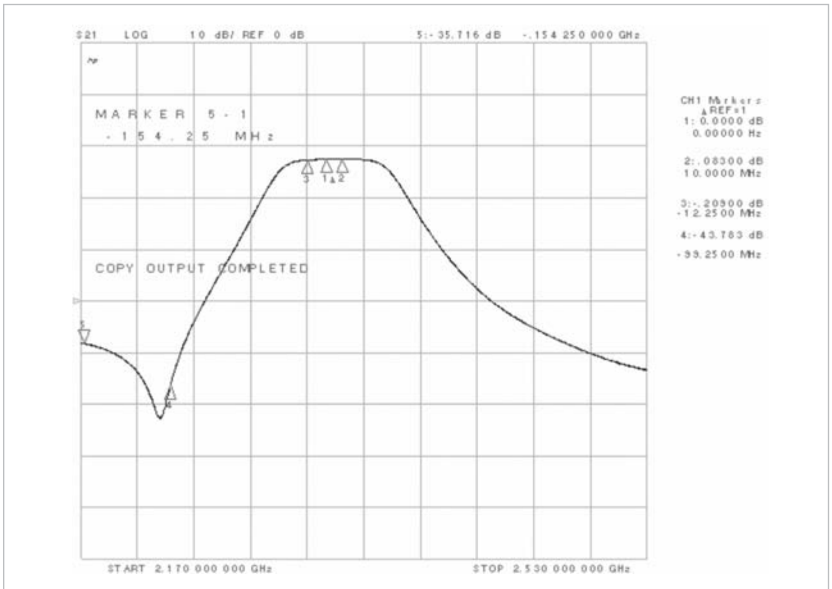

Figure 3 The measured amplifier response has a center frequency of 2.332 GHz.

Figure 3 shows measured gain performance at −40-dBm input power and −11.5-dBm output power relative to the 2.332-GHz center frequency. The circuit achieves out-of-band rejection with the help of the bandpass filter between the amplifier stages. EDN

REFERENCES

1 Chen, Seng-Woon, "Linearity requirements for digital wireless communications," *Technical Digest of the IEEE 19th Annual Gallium Arsenide Integrated Circuit Symposium*, Oct 15 to 17, 1997, pg 29, http://bit.ly/IUr2Ok.

2 Lee, Thomas H, *Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits*, University of Cambridge, 2004, ISBN: 0-521-83526-7.

3 "NE3509M04 hetero junction field effect transistor," California Eastern Laboratories, http://bit.ly/JxjB2F.

Simple solenoid driver is adaptable and efficient

Richard Oliver, Lowell Observatory, Flagstaff, AZ

Solenoid loads generally exhibit large hysteresis. Application of the rated voltage actuates these loads. Once they are in position, however, you can use a significantly lower voltage to thereafter reliably hold them on. A lower sustaining voltage results in less heat production and higher efficiency.

The circuit in **Figure 1** operates solenoid-driven air valves in the 4.2m Discovery Channel Telescope. The 24V-dc solenoid coil has a resistance of 72Ω. Diodes D_1 and D_2 and capacitor C_1 act as a ladder-type voltage multiplier. When Q_1 is off, they charge C_2 to approximately 1.5 times the peak-to-peak voltage of the transformer's secondary. The circuit in the **figure** shows approximately 24V.

When Q_1 turns on, the 24V on C_2 fires the solenoid. The solenoid current

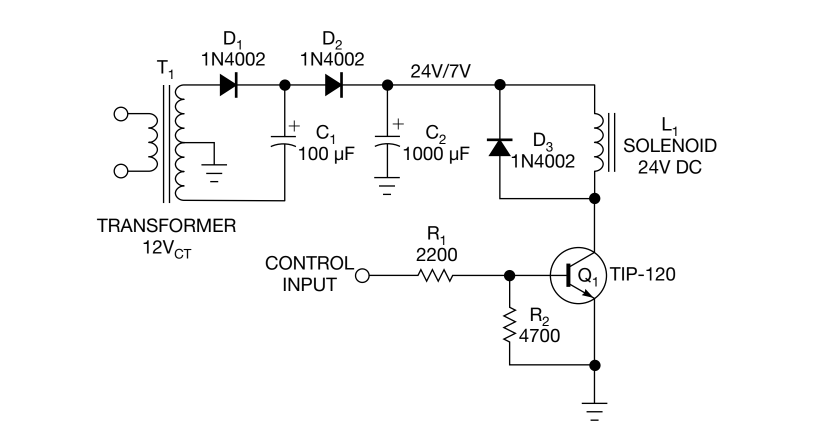

Figure 1 Capacitive-voltage division sets the precharge and sustaining voltages for efficient solenoid operation.

reduces the voltage on C_2 to a sustaining level of approximately 7 to 8V.

The selection of C_1 controls the sustaining voltage and the recharge time. Use an oscilloscope to confirm that, when the circuit is on, the voltage across C_1 remains positive throughout its cycle. If it is not, use a larger capacitor or substitute a nonpolarized unit. Once off, the circuit recharges rapidly, and the solenoid can fire again within 1 sec. Note that capacitor selection should be for ±20%-value tolerance or better.

The most attractive feature of this circuit is that C_1, a purely reactive component, accomplishes the voltage drop to the sustaining voltage; therefore, no power is dissipated. C_1 and C_2 should have voltages higher than the firing voltage; this circuit uses 35V capacitors. With appropriate tweaking, you can use this circuit for many solenoid-driver applications.

The 4.3m Discovery Channel Telescope incorporates this circuit in its guider and wavefront-sensor systems to insert alignment masks into the light path. Work on the telescope is nearing completion, and it will come online this summer, complete with its own TV special on the Discovery Channel. Find details at the Lowell Observatory Web site (www.lowell.edu). EDN

Automatic night-light feeds directly from the ac line

Abel Raynus, Armatron International Inc, Malden MA

There are many approaches to the problem of activating a light when it becomes dark, and a recent Design Idea covers this topic (**Reference 1**). Some approaches require a dc power supply and an electromechanical relay, but a better approach involves feeding the device directly from the ac line, minimizing the number of components (**Figure 1**).

The heart of the device is a light-sensitive cadmium-sulphide resistor, P_R, with a resistance of approximately 200 kΩ in the dark and decreasing to a few kilohms in the light. P_R and capacitor C_1 form an ac-voltage divider. In daylight, the voltage across P_R is too low to generate the required gate-trigger current to turn on bidirectional ac switch Q_1, thus keeping the load—usually a lamp—off. When it becomes dark, P_R's resistance rises, resulting in an increase in the TRIAC's gate current that triggers the TRIAC and lights the lamp.

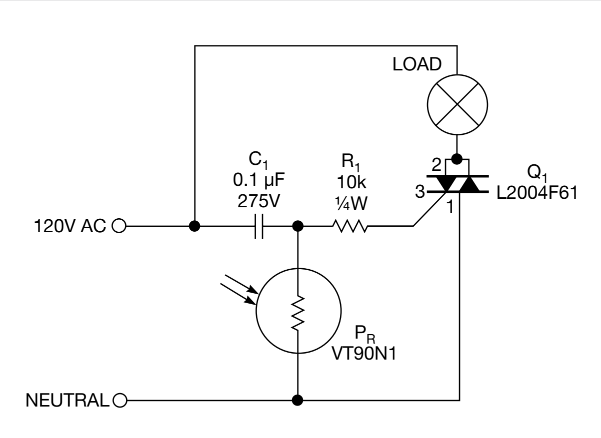

Figure 1 The photoresistor activates the TRIAC and the load when darkness falls.

The circuit uses inexpensive, off-the-shelf components, including the VT90N1 photoresistor; a 0.1-µF, 275V capacitor; and an L2004F61 TRIAC with a load current of 4A rms, a peak blocking voltage of 200V, and a gate-trigger current of 5 mA. The exact specifications of these components are not critical; you could use others instead.

Editor's note: Attributes worth mentioning include the fact that the capacitor introduces a phase shift, which places the peak of the gate voltage close to the zero crossing of the load's sine wave for optimum turn-on timing. Another benefit is thermal hysteresis, which occurs due to the reduction of the required triggering voltage and current as the TRIAC warms up after the initial turn-on. EDN

REFERENCE

1 Tran, Chau, "Simple night-light uses a photoresistor to detect dusk," *EDN*, Dec 15, 2011, pg 49, http://bit.ly/HPi1GG.

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Originally published in the August 6, 1992, issue of *EDN*

Dual op amp takes absolute difference

Lindo St Angel, Motorola General Systems Sector, Arlington Heights, IL

A traditional implementation of an absolute-difference function comprises a difference circuit followed by an absolute-value circuit; the entire circuit requires at least three op amps. The design problem is complicated in single-supply-only systems, which usually require an artificial ground, typically one-half of the supply. The circuit in **Figure 1** takes the absolute value of the difference of two voltages using only two single-supply, ground-referenced op amps. The circuit is designed for dc or low-speed operation.

For the case where $V_1>V_2$, IC_{1A} is disabled because diode D_1 is off. IC_{1B} and its associated resistors form a classic difference circuit where $V_{OUT}=(R_2/R_1)(V_1-V_2)$.

For the case where $V_2>V_1$, diode D_1 conducts, producing the composite amplifier system made up of both IC_{1A} and IC_{1B}, where $V_{OUT}=(R_2/R_1)(V_2-V_1)$. Using these two **equations**, the overall function of the circuit for V_1 and V_2 greater than zero is as follows: $V_{OUT}=(R_2/R_1)|(V_1-V_2)|$.

The circuit was built and tested with R_1=10 kΩ and R_2=220 kΩ. For $V_2>V_1$, the composite amplifier system has poor phase margin and is unstable. Thus, the circuit compensates the loop with the dominant pole formed by R_3 and C_1. At a gain of 22 and a desired response time of about 300 µsec (the 10 to 90% rise time when V_2 becomes 0.1V greater than V_1), values of R_3=56 kΩ and C_1=850 pF produced the best empirical results. R_3 and C_1 will vary, depending on the required speed of the response and the closed-loop gain.

Also, when $V_2>V_1$, the output of IC_{1A} becomes a function of the factor $2V_2-V_1$. Thus, IC_{1A} may saturate for large values of V_2. The factor's upper limit is as follows, where V_{SAT} is the saturation voltage for IC_{1A}: $(2V_2-V_1)<V_{SAT}(R_1+R_2)/R_2$. For the LM2902 operating from 5V, V_{SAT} is approximately 3.5V. This last **equation** also implicitly sets a common-mode voltage (V_{CM}) limitation. You can see this limitation by setting $V_1=V_2=V_{CM}$ and allowing the factor $(2V_2-V_1)$ to reduce to V_{CM}. EDN

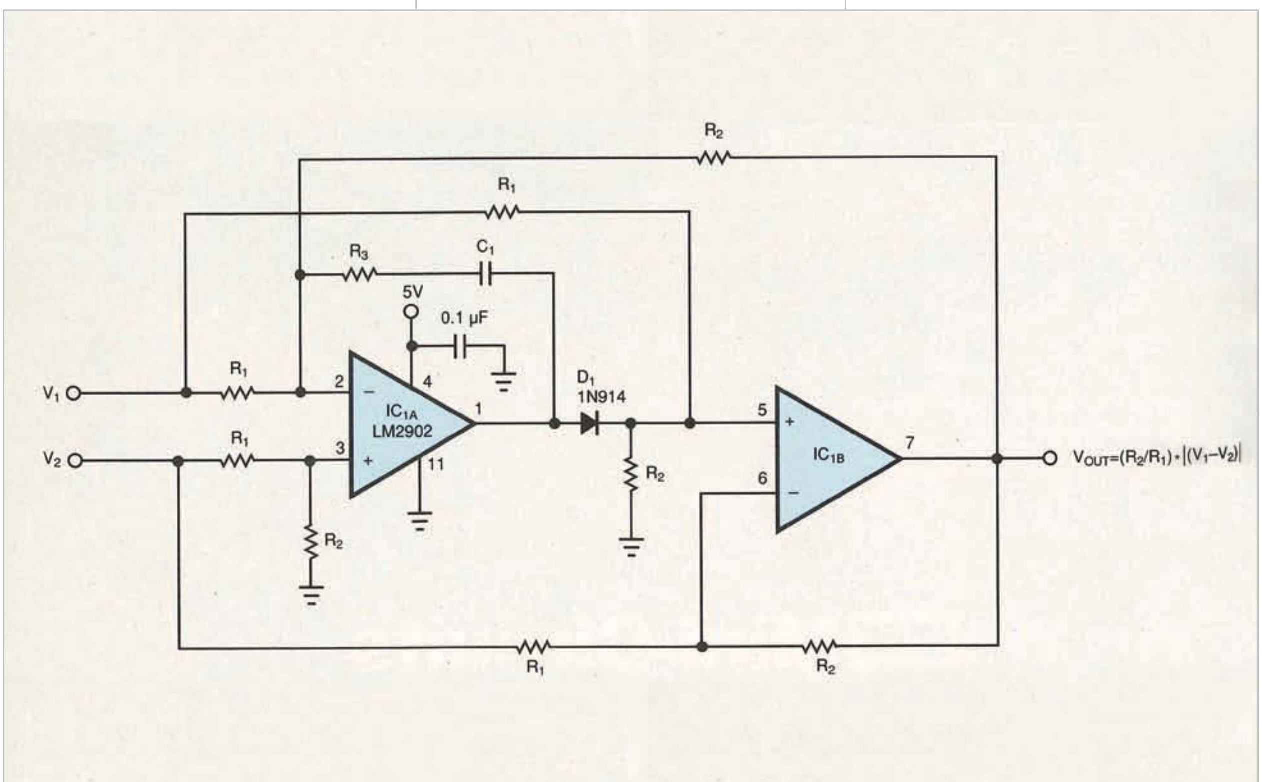
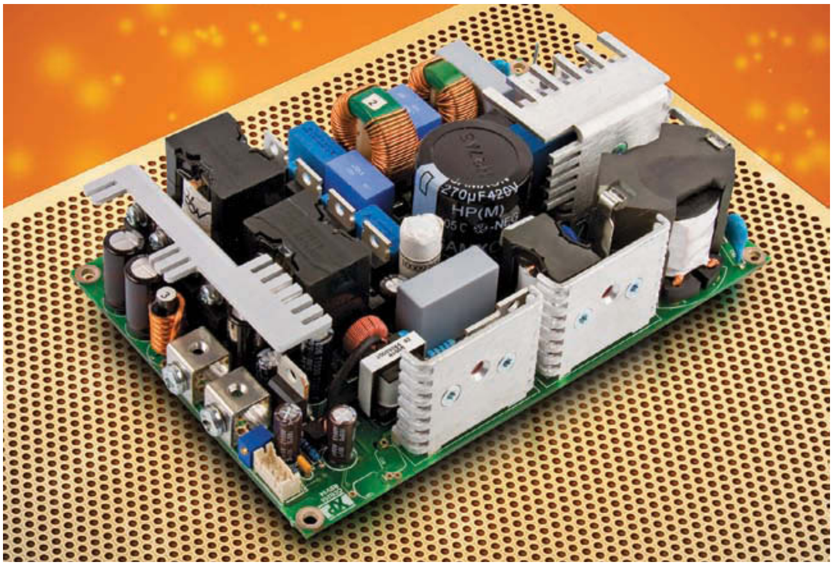


Figure 1 Using single-supply, ground-referenced op amps, this circuit accomplishes an absolute-difference function.

productroundup

POWER SOURCES



XP's CCB250 power supplies provide 95% efficiency

The CCB250 series of convection-cooled power supplies has an operating efficiency as high as 95%. The devices feature an input voltage of 80 to 275V ac in an ambient temperature of –20 to +70°C, with no derating until the temperature reaches 50°C. Maximum output power is 250W, and peak output power is 300W for as long as 500 msec. The six models in the series provide nominal outputs of 12, 15, 24, 28, 36, or 48V dc. A trim function allows the adjustment of the output by ±3% to accommodate line losses. An always-on 5V-dc, 0.5A output powers memory, logic, or control functions. The price is $175 (500).

XP Power, www.xppower.com

Fairchild FAN5904 increases mobile talk time

The FAN5904 synchronous buck converter supports GSM, GPRS, and EDGE protocols and 3, 3.5, and 4G power amplifiers. The device features a dynamically adjustable output voltage of 0.4 to 3.5V and an analog input voltage of 0.16 to 1.4V. Transition times are less than 10 μsec. The device operates in PWM mode with a 6-MHz switching frequency in low-power mode and a 3-MHz switching frequency in high-power mode, allowing its implementation with a 470-nH 2520 inductor and two 4.7-μF 1508 capacitors on the output to achieves less than 20.5 mm^2 of PCB area. Designers can also implement a 470-nH 2016 inductor, resulting in a footprint of less than 15 mm^2. The device comes in 16-lead WLCSP packages and sells for 95 cents (1000).

Fairchild Semiconductor, www.fairchildsemi.com

CUI's VGD series generates two voltages in one package

The VGD series of enclosed, dual-output internal switching power supplies comes in 30 and 60W configurations, targeting use in industrial-control, networking, automation, and test-and-measurement-equipment applications. The series offers a universal 85 to 264V-ac input and dual 5/12V- or 5/24V-dc output voltages. The devices feature short-circuit, overload, and overvoltage protection, a built-in EMI filter, and efficiency as high as 80%. Prices start at $19.80 each (100).

CUI Inc, www.cui.com

TI's LM3447 LED driver provides smooth dimming

The LM3447 ac/dc LED driver includes dimmer-detection, phase-decoder, and adjustable-hold-current circuits to provide smooth and flicker-free dimming in offline, isolated-LED-lighting applications, including A19, E26/27, and PAR30/38 bulbs, as well as can-light retrofits. The device operates with leading- and trailing-edge TRIACs and provides greater-than-0.9 PFC, thermal foldback, a fixed-frequency discontinuous-conduction-mode flyback topology with valley switching, LED open- and short-circuit protection, and driver-IC thermal shutdown. The LM3447 sells for $1.15 (1000).

Texas Instruments, www.ti.com

productroundup

Allegro Micro A8601 regulator targets automotive displays

The fixed-frequency, multiple-output A8601 regulator for LCD bias has a programmable or a synchronizable switching frequency with a 350-kHz to 2.25-MHz external-clock signal to minimize interference with AM- and FM-radio bands. The automotive-grade, AEC-qualified device has five independently adjustable output voltages from three linear regulators and two charge-pump regulators. It also features less-than-10-μA shutdown current; preprogrammed power-up and shutdown sequences; and overcurrent, overvoltage, and thermal-overload protection. Available in a 28-pin eTSSOP with an exposed thermal pad, the device sells for $2.95 (1000).

Allegro MicroSystems, www.allegromicro.com

On Semi's NCV890xxx series targets infotainment

The NCV890100, NCV890101, NCV890130, NCV890131, NCV890200, NCV890201, and NCV890231 switching buck regulators each incorporate an internal power switch and operate at 2 MHz. Designers can synchronize the 101, 131, 201, and 231 devices to an external-clock source. The devices convert an 18V input to outputs as low as 3.3V and a 16V input to outputs as low as 2.5V; they maintain a constant switching frequency of 2 MHz. The devices operate over 4.5 to 36V and can tolerate load-dump voltages as high as 40V and 45V for the 130, 131, and 231, suitable for start/stop and cold-crank conditions. The 100, 101, 130, and 131 deliver 1.2A of peak output current, and the 200, 201, and 231 deliver 2A. Available in DFN-8, DFN-10, and SOIC-8 packages, the devices sell for $1.13 to $1.50 (2500).

On Semiconductor, www.onsemi.com

ADI's ADP5041 and ADP5040 take up little PCB space

The ADP5041 and ADP5040 regulators combine a 3-MHz, 1.2A buck regulator and two 300-mA low-dropout regulators in a 20-lead LFCSP. They each use nine components and take up 50 mm^2 of PCB space. The 1.2A buck regulator has an output voltage of 0.8 to 3.8V, a current-mode topology, a 3-MHz operating frequency, a peak efficiency as high as 96%, and a regulator accuracy of ±3%. The low-dropout regulators feature an output voltage of 0.8 to 4.75V, an input supply voltage of 1.7 to 5.5V, a 60-dB PSRR to 10 kHz, 60-μV-rms typical output noise at 1.2V, and a dropout voltage of 150 mV at a 300-mA load. The ADP5041 has a circuit that detects a three-state condition when applied to the watchdog-refresh input at the WDI pin. A processor or a DSP port controls this pin. The processor can disable this watchdog-refresh timer when the port is in three-state mode, preventing a watchdog reset to the processor. The ADP5041 and ADP5040 sell for $1.79 and $1.39 (1000), respectively.

Analog Devices Inc, www.analog.com

Unipower's Sabre Lite hot-swap modules target 89% efficiency

The Sabre Lite series of sine-wave, hot-swap-inverter modules features a DSP-controlled architecture to produce a low-distortion, 50- or 60-Hz sine wave, efficiency levels better than 89%, and power density of 10.5W/in^3. The 1-kVA, 1200W, 1U-high modules produce 120 or 230V-ac nominal outputs from an input voltage of 40.5 to 58V dc. Two units in a 19-in. shelf can provide twice the capacity of one unit or operate automatically in an N+1 redundant mode. Operating temperature range without derating is −5 to +50°C. Prices start at $11.51 (medium to low volumes).

Unipower, www.unipowerco.com

GE's Barracuda bus converter targets IBAs

Targeting use in intermediate-bus architectures, the 300W, eighth-brick Barracuda bus converter comes in 25A digital and analog modules. Input voltage is 36 to 75V dc, with a 95% energy-efficiency rating. The device has a 58.4×22.8×11.3-mm form factor and an operating temperature of −40 to +85°C. The digital version incorporates communication, synchronization, load sharing, differential remote sensing, and output voltage trim. The analog series is compatible with the DOSA-standard five-pin bus-converter pinout. Prices start at $41 (OEM quantities).

GE Energy, www.ge-energy.com

TDK's HFE2500 targets hot-swap systems

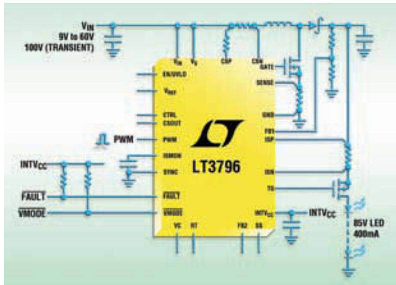
The 2.5-kW HFE2500 series of front-end power supplies targets distributed-, hot-pluggable-, and redun-

dant-power systems. The 19-in., rack-mount enclosure allows designers to parallel as many as four supplies with automatic load sharing to provide as much as 9.5 kW of output power. An optional integral microcontroller in each supply allows for remote programming, monitoring, and status reporting using an isolated I^2C/PMBus interface, which allows designers to individually turn the supplies on or off as the system load varies. The HFE2500 supplies measure 1.61×4.21×12.8 in. and sell for $689 each (100).

TDK Corp, www.tdk.com

Linear LT3796 delivers 94% efficiency

The 100V LT3796 high-side current-sense dc/dc controller regulates a constant current or voltage to drive HB LEDs. A 6 to 100V input voltage supports automotive, architectural-lighting, and industrial applications. The device has an external N-channel MOSFET and can drive white LEDs with as much as 85V from a nominal 12V input, delivering more than 50W, or more than 94% in boost mode. A frequency-adjust pin enables users to program the frequency at 100 kHz to 1 MHz. The LT3796 comes in a thermally enhanced TSSOP-28, and prices start at $3.45 (1000). Prices for the extended-temperature LT3796IFE and the H-grade-option LT3796HFE start at $3.86 and $4.11, respectively.



Linear Technology Corp, www.linear.com

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Probing questions

DANIEL VASCONCELLOS

My first job after college was working for a major HVAC (heating/ventilation/air-conditioning) manufacturer. The company was developing a new home-heat-pump-controller design using a microcontroller, and a number of prototype units were already available for development when I came onboard. The company had hired a consultant, who taught microprocessor programming at a local college, to write just enough software to get the processor off the ground. I began by writing some preliminary software to exercise the digital I/O, which contained a number of output relays.

As I began testing the software on the prototype, I almost immediately smelled something burning; a resistor in the power-supply section of the prototype soon started to emit smoke and then began burning. I quickly shut off the power, but it was too late to save the resistor and the expensive microcontroller.

I took the charred board to the electronics lab to do some forensic work. I replaced the resistor, checked the power supply, and found everything in order. I then put in a preprogrammed microcontroller containing the consultant's code, and the prototype correctly executed the code upon power-up. After returning to my office to continue testing, I downloaded my code; as soon as the prototype powered up, the same resistor started to smoke again. Following two more trips to the lab for repairs, I found that the prototype would consistently run with the consultant's code but overheat and fail while running mine.

The smoking resistor connected between the input and the output of the regulator, according to the application note, to boost output power. I connected an oscilloscope at a convenient spot—the output of the regulator and ground—and single-stepped through the code to see what event had triggered the overheating. I patiently single-stepped through my code several times, but the system didn't fail. On the scope, I observed an occasional—and somewhat expected—spike in the 5V-dc rail when one of the relays cycled. I eventually decided to run the board at normal speed; it continuously executed my code without any problems.

The next time I powered up the board, the resistor immediately started to smoke again. At this point, I realized I had not reconnected the scope to the prototype after my inspection. Could the scope probe somehow have been making the difference? I reconnected the scope using an FET probe instead of the X1 probe I had previously been using and again began stepping through the code. This time, the scope showed a substantial ringing on the power-supply rail each time a relay cycled.

The ringing on the supply rail made me ponder the effects of a seemingly benign software change I had recently made. The consultant had written to the relay outputs using byte writes. I had changed to a BSET and BCLR instructions to independently control relays. As a result, my code would cycle the relays in rapid succession upon initialization or at the end of a cycle. The cycling was enough to cause the regulator to latch up, causing the resistor to overheat.

I discovered that the decoupling capacitor had been "combined" with another capacitor closer to the processor; the intent was to decouple the processor and regulator using one part to save costs. The capacitor's higher value, remote location, and vias in the path to it allowed the regulator to become unstable with sudden changes in load. The X1 probe had provided just enough "decoupling" to maintain the regulator's stability.

I soldered a 0.01-μF capacitor between the ground and the output terminal of the regulator, and the stability problems immediately disappeared. I quickly learned about the subtleties of using application notes and paying close attention to decoupling techniques. **EDN**

Jan D Clarke is a professional engineer in York, PA.


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