UBM Electronics

EDN®

SEPT 2012
www.edn.com
Issue 15

Headless ATE system increases production reliability and efficiency
Page 25

PCB-layout considerations for nonisolated switching power supplies
Page 41

30 YEARS OF DSP

Page 30

IT'S NO ACCIDENT...

DIGIKEY.COM

THE BUSIEST WEBSITE IN THE INDUSTRY!

80% MORE UNIQUE VISITORS
— THAN THE NEXT —
CLOSEST DISTRIBUTOR

Source: *Unique Visitors, March 2012, Compete.com*

Digi-Key® CORPORATION

World's Largest Selection of Electronic Components Available for Immediate Shipment

2 MILLION PARTS ONLINE | 500+ INDUSTRY-LEADING SUPPLIERS | NEW PRODUCTS ADDED DAILY

1.800.344.4539

Anritsu

Smart now.
Smart later.

VectorStar® Network Analyzers are technologically and economically smart.

Anritsu's industry-leading technology delivers performance where it really matters. The VectorStar 70 kHz to 125 GHz flagship broadband system provides industry-best performance in all three critical performance areas: broadband frequency coverage, dynamic range, and measurement stability. Whatever your starting requirement, feel safe in the knowledge that Anritsu VectorStar offers the expandability you need in the future. As your needs grow, so can your VectorStar, with:

- 20, 40, 50, and 70 GHz models and the flagship 70 kHz to 125 GHz broadband system
- Industry-leading combination of frequency coverage, dynamic range, and stability
- Two-port, four-port, and multiport (4-12) variants
- Nonlinear measurement systems

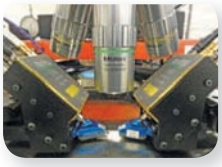
For applications ranging from microwave component testing to on-wafer device characterization, when you want best-in-class performance and industry-leading technology, you know the answer—Anritsu.

To learn more and download an application note from our library, visit us at:

www.anritsu-offer.com/vna-edn/

Scan code for library:

Microwave Bench Portfolio



40 kHz to 125 GHz VNA
- On-wafer and bench top
- Extensions to 750 GHz

Two-Port and Multiport VNA Solutions
- 20, 40, 50, and 70 GHz

Signal Generators
- 0.1 Hz to 70 GHz
- Extensions to 325 GHz
- Low phase noise

Power Meters
- 10 MHz to 50 GHz

USB Power Sensors
- 10 MHz to 26 GHz

"Superinductors"

That's what engineers are calling our new ultra-low DCR power inductors

Super*con*ductors pass current with virtually no resistance.

Our new XAL/XFL inductors do much the same. Their DCR is incredibly low: often half that of similar size parts.

And their current handling is equally impressive. Coilcraft's proprietary core material has a soft saturation characteristic that prevents drastic inductance drops during current spikes.

Competitors' 4.7uH inductors have much higher DCR per mm³ than Coilcraft's XAL5030.

Unlike competitive parts, these inductors don't suffer from thermal aging. And we give you far more footprint options to maximize PCB density.

To see what else makes our new XAL/XFL inductors so super, visit **coilcraft.com/xal.**

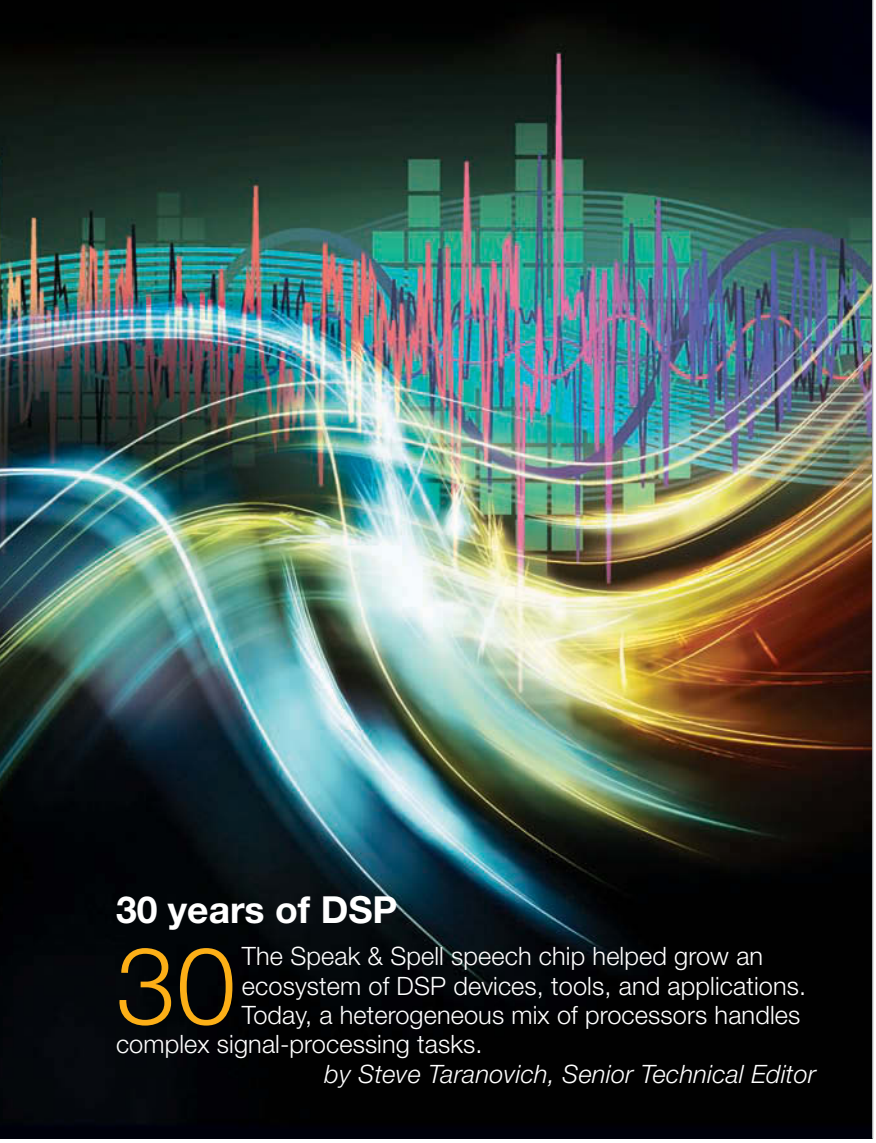
Coilcraft®

coilcraftdirect.com
No min order. Next day delivery.

WWW.COILCRAFT.COM

EDN contents

September 2012



30 years of DSP

Headless ATE system increases production reliability and efficiency

PCB-layout considerations for nonisolated switching power supplies

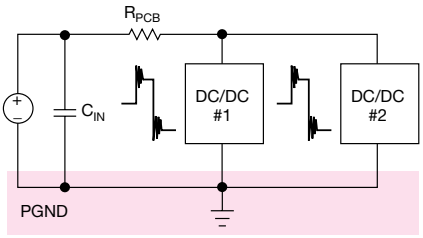
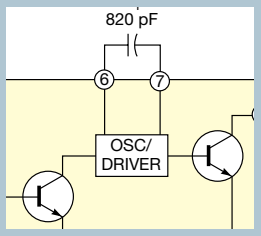


IMAGE: SHUTTERSTOCK & THINKSTOCK

DESIGNIDEAS

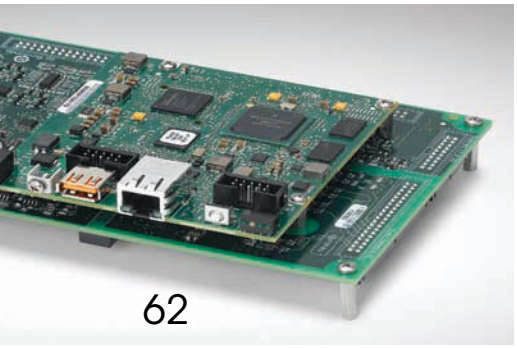


▶ Submit your own Design Idea to edndesignideas@ubm.com.

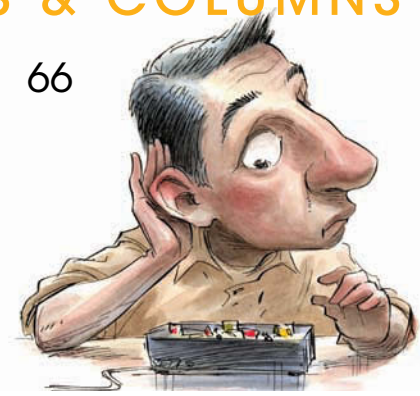
contents September 2012

pulse

DEPARTMENTS & COLUMNS



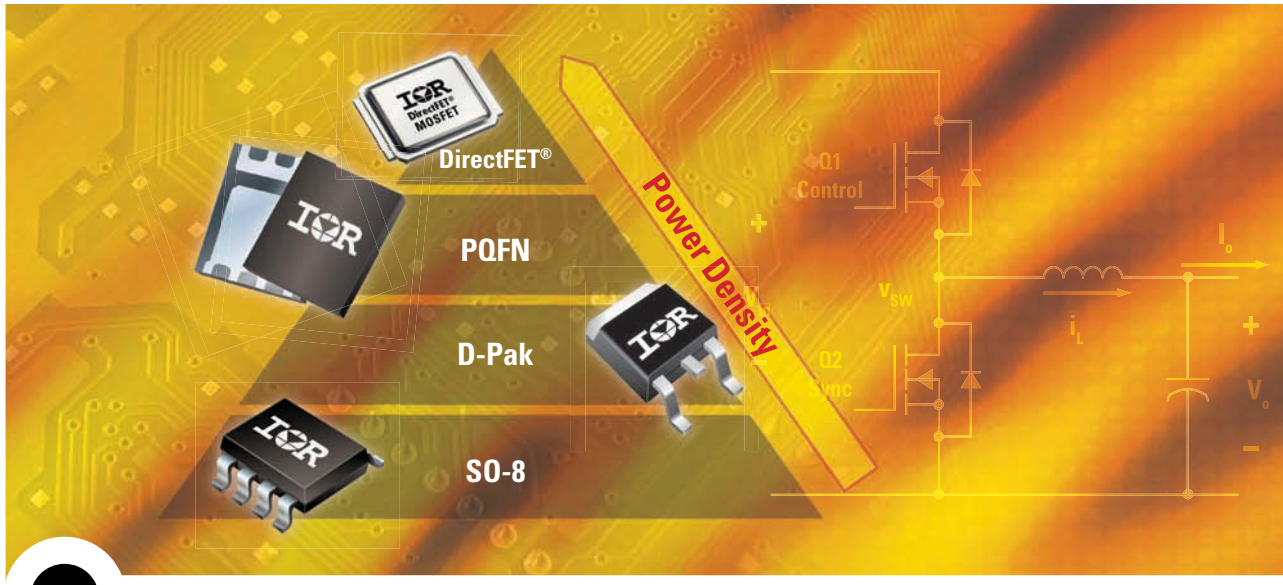
62



66

EDN® (ISSN# 0012-7515) is published semimonthly (January–June) and monthly (July–December) by UBM Electronics, 600 Community Drive, Manhasset, NY 11030-3825. Periodicals postage paid at Manhasset, NY, and at additional mailing offices. SUBSCRIPTIONS—Free to qualified subscribers as defined on the subscription card. Rates for nonqualified subscriptions, including all issues: US, $150 one year; $250 two years; $300 three years. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. For telephone inquiries regarding subscriptions, call 847-559-7597. E-mail: edn@omeda.com. CHANGE OF ADDRESS—Notices should be sent promptly to EDN, PO Box 3609, Northbrook, IL 60065-3257. Please provide old mailing label as well as new address. Allow two months for change. NOTICE—Every precaution is taken to ensure accuracy of content; however, the publishers cannot accept responsibility for the correctness of the information supplied or advertised or for any opinion expressed herein. POSTMASTER—Send address changes to EDN, PO Box 3609, Northbrook, IL 60065-3257. CANADA POST: Publications Mail Agreement 40612608. Return undeliverable Canadian addresses to APC, PO Box 503, RPO West BVR CRE, Rich Hill. ON L4B 4R6. *Volume 57, Number 15 (Printed in USA).*

[www.edn.com]



Select The Best MOSFET Pair to Meet Your Power Density Needs

Scalable Solutions for DC-DC Buck Converters

Part Number	BV_{DSS} (V)	Function	Package	$R_{DS(on)}$ Max. V_{GS}=10V (mΩ)	Q_G V_{GS}=4.5V (nC)
IRFH5306	30	Control	High Current PQFN 5 x 6	8.1	7.8
IRFH5302	30	Sync	High Current PQFN 5 x 6	2.1	29
IRFHM831	30	Control	PQFN 3x3	7.8	7.3
IRFHM830	30	Sync	PQFN 3x3	3.8	15
IRFHM830D	30	Sync	PQFN 3x3	4.3	13
IRFH7911	30	Control	Half-Bridge Asymmetric PQFN 5x6	8.6	8.3
		Sync		3.0	34
IRLR8729	30	Control	D-Pak	8.9	10
IRLR8726	30	Sync	D-Pak	5.8	15
IRF8714	30	Control	SO-8	8.7	8.1
IRF8734	30	Sync	SO-8	3.5	20
IRF8513	30	Control	Half-Bridge Asymmetric SO-8	15.5	5.7
		Sync		12.7	7.6

The IR Advantage

- Optimized Sync and Control MOSFETs for high system efficiency
- High light-load efficiency
- Improved thermal performance with DirectFET® top-side cooling
- Scalable solutions for different power density requirements
- Benchmark performance
- Wide range of packages

Your FIRST CHOICE for Performance

for more information call 1.800.981.8699 or visit us at www.irf.com

Distributors : ALLIED ELECTRONICS | Digi-Key CORPORATION | AVNET electronics marketing | FUTURE ELECTRONICS | ARROW ELECTRONICS | Newark | MOUSER ELECTRONICS a tti company

International IOR Rectifier
THE POWER MANAGEMENT LEADER

EDN online

JOIN THE CONVERSATION

Comments, thoughts, and opinions shared by *EDN*'s community

In response to "Neil Armstrong, 1930 to 2012: gone but never to be forgotten," a blog post by Patrick Mannion at www.edn.com/4394788, RichQ commented:

"I was 16 when [Apollo 11 landed on the moon], already a nerd and immensely proud of what my future profession had accomplished. This got my father (a USAF doctor) to talk about his time helping study the probable effects of space on humans, years before the first Mercury went up. It was a personal connection to the moon event that I had not known about before and made me doubly proud.

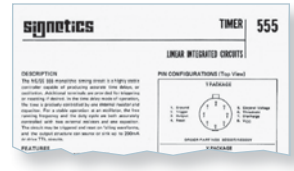
"Full moon coming up this weekend [Aug 31]. Will gaze at it and reflect. Well done, Neil. Well done."

In response to "Faraday discovers electromagnetic induction, August 29, 1831," a post in the *EDN* Moments blog at www.edn.com/4394972, Bill Groves (@billgroveseng) commented via Twitter:

"That wasn't just a fair-uh-day; it was a most excellent day! ;-) Sorry, couldn't resist (badda boom)."

In response to "How to read a data sheet," an article by Doug Grant at www.edn.com/4394484, Battar commented:

"Here's a bit of advice I got from an expert: If a chip fails on you, get to the list of 'absolute maximums' in the data sheet. The chip failed because you overstepped one of those lines. Just check which one."



EDN *invites all of its readers to constructively and creatively comment on our content. You'll find the opportunity to do so at the bottom of each article and blog post.*

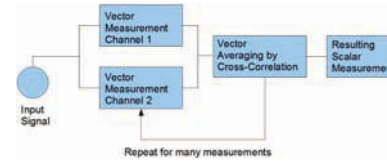
CONTENT

Can't-miss content on EDN.com

CIRCUIT PROTECTION CAN'T BE AN AFTERTHOUGHT

Design functionality suffers when circuit protection is deferred. Engineers whose professional lives revolve around overcurrent protection and shock immunity share their expert recommendations.

www.edn.com/4394365



MEASURING SMALL SIGNALS ACCURATELY: A PRACTICAL GUIDE

Measurement of very small signals close to or even below our instrument's noise floor can be made more accurate by using noise de-embedding or by applying a multichannel cross-correlation technique.

www.edn.com/4394635

ENGINEERING COMMUNITY

Opportunities to get involved and show your smarts

Focused on the ARM ecosystem, this Santa Clara, CA, event kicks off on Tuesday, Oct 30, with an intensive day specifically geared toward chip-design teams working with ARM intellectual property and tools. Wednesday and Thursday will feature programs for system designers and software developers interested in building ARM-technology-based modules, boards, and systems. Don't miss this opportunity for design debate, learning, and discovery.
www.armtechcon.com

BY PATRICK MANNION, BRAND DIRECTOR

Apple won, so what now for designers?

The verdict in the Apple v. Samsung patent-infringement case, which Apple won to the tune of $1.049 billion, was remarkable for the size of the award as well as for the post-verdict opining. To put together some practical guidance for designers and innovators wanting to know what to do now, I spoke with Mike McLean, senior vice president of IP rights at TechInsights, a UBM company that specializes in this area.

I would also guide you to our Design Cycle blog post, "Patents: Where's yours (and how do you get them)?" (www.edn.com/4311963), which polls the *EDN* community on the topic of patents in general and includes a link to Apple's patent portfolio. Both the community's comments and the portfolio are worth a look, given what I'm about to share.

Almost immediately, the Apple verdict drew rants against the ineptitude of the US patent office and the innovation-stifling nature of the patent process; accusations from outside the United States of jury and even judicial bias toward US-based companies; condemnation of those evil patent trolls who add nothing yet take everything; and, of course, disdain for the big, bad lawyers who get an "unfair" share of the spoils. It seemed no one was happy, aside from Apple and its attorneys.

McLean, for his part, is direct in his assessment of the claims that the US patent environment stifles innovation. It's "an emotional argument," he says. "There are examples on both sides and lots of data to show it can encourage innovation, too. The pace of technology hasn't slowed down."

Of course, that doesn't mean the system can't be improved, but right now, it's the best we've got. As for whether the system is skewed in favor of US corporations, I'm sure that has sometimes appeared to be the case; in the wake of the Apple-versus-Samsung verdict, many South Korean and European pundits intimated as much. McLean, however, says he doesn't "see that skewing," noting that "international companies use the US patent system. They take advantage of the strong patent-protection system in the US."

At least one *EDN* reader from outside the United States agrees, noting in a comment to our aforementioned blog: "I have a few patents which were used in manufacture, too, but in my country—I live in the Ukraine—it [a patent] is similar to toilet paper."

Designers should take away a few keys points from the Apple verdict, according to McLean. The first is that you either need to get out ahead of Apple or choose a different area of focus. "Apple has shown they are willing to defend their patents," McLean says.

Second, mobile handsets are a heavily patented category and one in which numerous battles continue to be fought. "You can't go into a mobile-device design without knowing [what you're up against]," McLean says.

We know this to be true—indeed, a main reason that Google bought Motorola's Mobility Group was the latter's patent portfolio—but what's the point at which you become the target for a patent-infringement suit, or what I like to call the tripping point? According to McLean, two main circumstances can push an innovator to that point, and both boil down to dollars.

The first is sizable revenue for your product. "This will draw the attention of people who have patent portfolios in that space," McLean says. The second, related factor is market share; if you start taking it from the big guys, watch out.

So, how does a little-guy inventor or operation navigate this legal minefield? Talk with the right people, check out the space, and get a good patent attorney, McLean says. Put yourself in a position to defend yourself. "Starting out, it's not really an issue," says McLean; "it's when [your innovation] starts making money" that you need to beware. Defending means having a patent portfolio to help with cross-licensing deals; this fosters design freedom and can provide supplementary income.

Two circumstances put an innovator at risk of becoming a patent-suit target, and both boil down to dollars.

The biggest mistake you can make, beyond ignoring the issue altogether, is focusing only on the innovation itself. You will always need access to other people's patents, McLean notes, so don't just patent your specific solution to a problem, as others can design their own work-arounds. Instead, try and think of all other possible work-arounds and patent those, too. "This gives you more trading chips to get licenses," he says.

For more on how *EDN* community members really feel about patents and the patent process, and whether they're worth the trouble, go to www.edn.com/4311963. While you're there, add your voice to the debate. EDN

Contact me at patrick.mannion@ubm.com.

EDN

BRAND DIRECTOR
Patrick Mannion
1-631-543-0445;
patrick.mannion@ubm.com

EXECUTIVE EDITOR
Rich Pell
Consumer
1-516-474-9568;
rich.pell@ubm.com

MANAGING EDITOR
Amy Norcross
Contributed technical articles
1-781-734-8970;
amy.norcross@ubm.com

MANAGING EDITOR, ONLINE
Suzanne Deffree
DIY, STEM, Industry Watch
1-631-266-3433;
suzanne.deffree@ubm.com

SENIOR TECHNICAL EDITOR
Steve Taranovich
Analog, Power, Design Ideas
1-631-413-1834;
steve.taranovich@ubm.com

CONTRIBUTING EDITOR
Carolyn Mathas
LEDs, Communications
1-530-873-3755;
cmathas@earthlink.net

CONTRIBUTING EDITOR
Stephen Evanczuk
Systems Design
1-802-549-4644;
sevanczuk@gmail.com

DESIGN IDEAS CONTRIBUTING EDITOR
Glen Chenier
edndesignideas@ubm.com

ASSOCIATE EDITOR
Diana Scheben
1-631-983-7693;
diana.scheben@ubm.com

ASSOCIATE EDITOR
Jessica MacNeil
1-212-600-3243;
jessica.macneil@ubm.com

COLUMNISTS
Howard Johnson, PhD, Signal Consulting
Bonnie Baker, Texas Instruments
Pallab Chatterjee, SiliconMap
Kevin C Craig, PhD, Marquette University

CONTRIBUTING TECHNICAL EDITORS
Dan Strassberg, strassbergedn@att.net
Brian Bailey, brian_bailey@acm.org
Robert Cravotta
robert.cravotta@embeddedinsights.com

VICE PRESIDENT/DESIGN DIRECTOR
Gene Fedele

CREATIVE DIRECTOR
David Nicastro

ART DIRECTOR
Giulia Fini-Gulotta

PRODUCTION
Adeline Cannone, Production Manager
Laura Alvino, Production Artist
Yoshihide Hohokabe, Production Artist
Diane Malone, Production Artist

EDN EUROPE
Graham Prophet,
Editor, Reed Publishing
gprophet@reedbusiness.fr

EDN ASIA
Huang Hua,
Operations General Manager
huang.hua@ednasia.com
Grace Wu,
Associate Publisher
grace.wu@ednasia.com
Vivek Nanda, Executive Editor
vnanda@globalsources.com

EDN CHINA
Huang Hua,
Operations General Manager
huang.hua@ednchina.com
Grace Wu,
Associate Publisher
grace.wu@ednasia.com
Jeff Lu, Executive Editor
jeff.lu@ednchina.com

EDN JAPAN
Masaya Ishida, Publisher
mishida@mx.itmedia.co.jp
Makoto Nishisaka, Editor
mnishisa@mx.itmedia.co.jp

UBM ELECTRONICS MANAGEMENT TEAM
Paul Miller,
Chief Executive Officer, UBM Technology
Kathy Astromoff,
Chief Executive Officer, UBM Electronics
Brent Pearson,
Chief Information Officer
David Blaza,
Senior Vice President
Karen Field,
Senior Vice President, Content
Jean-Marie Enjuto,
Vice President, Finance
Barbara Couchois,
Vice President,
Partner Services and Operations
Felicia Hamerman,
Vice President, Marketing
Amandeep Sandhu,
Director of Audience Engagement and Analytics

UBM Electronics

For a complete list of editorial contacts, see http://ubmelectronics.com/editorial-contacts

pulse

INNOVATIONS & INNOVATORS

Morse code on Mars

The engineers at NASA's Jet Propulsion Laboratory had a bit of fun with the design of the Curiosity Mars rover: If you look carefully at the treads on the wheels of the vehicle, you'll notice the predominant, zigzag pattern, but you'll also see a section of tread on each wheel that's patterned with dots and dashes. As the rover has begun its explorations of the Red Planet, its wheels have left snippets of Morse code imprinted in the surface dust.

The official word is that the dots and dashes serve as "visual odometry markers" that tell the mission controllers how far Curiosity has roved and let them verify that the rover's wheels are indeed turning when the rover's telemetry says it is moving. But I think they're a cool hack that some ham on the development team at the Jet Propulsion Lab couldn't resist; after all, the dots and dashes spell out "JPL."

A while back, I had lunch with a professor and some of his grad students. The prof knew I was a ham and told his students that I could decode Morse code signals in my head. The students were astonished, partly because they didn't know Morse code was still being used anywhere, and partly because a human could copy it without a computer.

It turns out that Mars isn't the only place you'll find Morse code these days. The next time you watch a baseball game being played at Fenway Park in Boston, look carefully at the white lines in the scoreboard on the left-field wall. You'll spot some dots and dashes hiding in plain sight in two of the vertical stripes. They spell out "TAY" and "JRY," for Thomas A Yawkey and his wife, Jean R Yawkey; the Yawkeys were co-owners of the Red Sox for many years.

There is also a "Morse Code" wine brand in the shops; the specific varietal is spelled out in dots and dashes on the label. The next time you're shopping for wine, bring along a ham to tell you what it is. **—by Doug Grant**

▷**NASA JPL**, www.jpl.nasa.gov.

The tread pattern on the Mars Science Laboratory Curiosity rover leaves an impression on the Martian surface spelling "JPL" in Morse code: ·--- ·-·· ·-·· (courtesy NASA/JPL).

TALKBACK

"Jack Kilby: He invented the integrated circuit and enabled the electronics revolution."

—Commenter fgibbard, in response to a 5 Engineers blog post that asks, "Who are the greatest engineers of all time?" Weigh in at www.edn.com/4394683.

Name
Dr. Dennis Hong

Job Title
Associate Professor of Mechanical Engineering, Virginia Tech

Area of Expertise
Robotics

LabVIEW Helped Me
Convey and respond to vast amounts of data in real time

Latest Project
Design and prototype a car that can be driven by the blind in just 4 months

NI LabVIEW

LabVIEW makes me better because

CODE REUSE

saves time and effort

>> Find out how LabVIEW can make you better at **ni.com/labview/better** **800 453 6202**

NATIONAL INSTRUMENTS™

Dual-range dc power source furnishes up to 350W

B&K Precision Corp has expanded its line of dual-range power supplies with the Model 1747, which can deliver up to 350W in constant-voltage and constant-current operating modes. Suitable for a variety of uses in electronics manufacturing, service and repair, and engineering labs, the Model 1747 offers operational flexibility within voltage and current ranges to meet specific test needs.

The supply can output either higher voltage at a lower current (0 to 60V, 5A) or higher current at a lower voltage (0 to 35V, 10A). Providing nearly three times more power than the similar Model 1737, the Model 1747 offers a sufficient increase in current range yet still maintains the regulation and low-ripple characteristics available in the Model 1737.

Both voltage and current are adjustable with coarse- and fine-control knobs. Two bright, four-digit LED meters monitor voltage and current.

Other features include automatic recall of the supply's last settings on power-up, overload and reverse-polarity protection, and the addition of an output on/off button. An RS-232 port on the rear panel allows remote control of the instrument from a PC using software or remote commands.

The price of the unit is $879.

—by Susan Nordyk

The Model 1747 offers an increased current range but maintains the regulation and low ripple of its predecessor.

▷**B&K Precision Corp**, www.bkprecision.com.

Octal ultrasound receiver embeds digital demod, cuts processor overhead

Analog Devices Inc says its AD9670 ultrasound receiver, with embedded demodulation and decimation, can condition eight channels of data from RF to a baseband frequency, reducing the processing load on the system FPGA by at least 50% compared with comparable receivers.

The AD9670 integrates a low-noise amplifier; variable-gain amplifier; antialiasing filter; and 125M-sample/sec, 14-bit ADC with SNR performance of 75 dB for enhanced image quality. The part is the latest addition to Analog Devices' ultrasound-receiver portfolio and is designed for midrange to high-end portable and cart-based ultrasound systems.

The AD9670 embeds demodulation and decimation functionality to offload the system FPGA.

The integrated digital I/Q demodulator, programmable-oscillator, and 16-tap FIR (finite-impulse response) decimation filter reduce FPGAs' data-bandwidth requirements, letting designers use less expensive processors or reallocate processing bandwidth to other system functions. The receiver provides a CW (continuous wave) processing path with an analog I/Q demodulator that has harmonic rejection to the 13th order, allowing designers to reduce the number of filter components and thereby cut system cost, reduce design complexity, and improve signal sensitivity. The CW-mode output dynamic range is more than 160 dBc/$\sqrt{Hz}$ per channel.

According to Analog Devices, the octal receiver's 30-MHz antialiasing filter frequency and high A/D sampling rate yield 3-dB higher SNR performance than competing devices can provide. The ADC in the AD9670 offers a programmable clock, data alignment, and programmable digital test-pattern generation, providing built-in fixed and pseudorandom patterns and supporting custom, user-defined test patterns, entered via a serial port interface. Total power is 130 mW per channel; an eight-channel low-noise amplifier reduces input-referred noise to 0.78 nV/$\sqrt{Hz}$ typical at 5 MHz (gain equals 21.3 dB).

"By introducing the first octal ultrasound receiver with digital demodulation and decimation filtering, we are able to minimize the data I/O and throughput rates and place less stress on the system processor," says Pat O'Doherty, vice president of the health-care segment at Analog Devices.

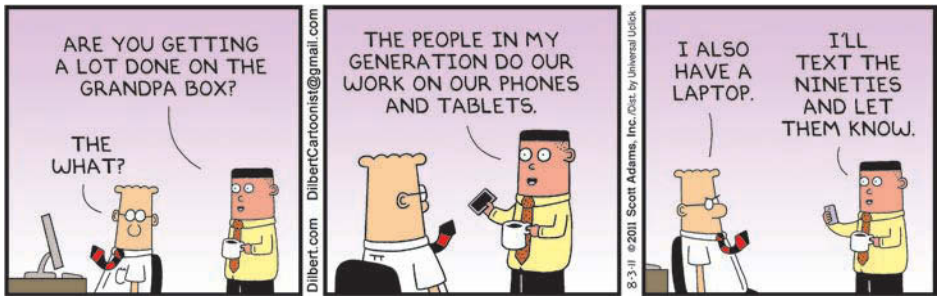
The AD9670 is pin-similar to ADI's AD9278 and AD9279 octal receivers, allowing designers to upgrade cart-based and portable ultrasound equipment designs using a common PCB layout.

The receiver is due in full production in October for a price of $69 (1000).

—by Nick Flaherty

▷**Analog Devices**, www.analog.com.

DILBERT By Scott Adams



Welcome to the mobile age of data monitoring and control.

The Agilent 34972A Data Acquisition Switch Unit takes our best-selling Agilent 34970A to the next level with built-in LAN and USB connectivity. You can even control everything remotely via mobile Web interface (phone or tablet). So you can collect and understand more data, more quickly.

34972A	34970A
BenchLink data logger software SCPI programming	
3-slot LXI unit with built-in 6½ digit DMM	
USB and LAN	GPIB and RS-232
Graphical web interface	N/A
$1,882*	$1,629*

* Prices are in USD and are subject to change

Scan the QR code or visit http://goo.gl/nELPY to see a 34972A product tour video

Agilent and our Distributor Network
Right Instrument.
Right Expertise.
Delivered Right Now.

TESTEQUITY
800-732-3457
www.testequity.com/agilent

FREE mobile app and wireless connectivity measurement tips
www.testequity.com/Agilent_DAQ

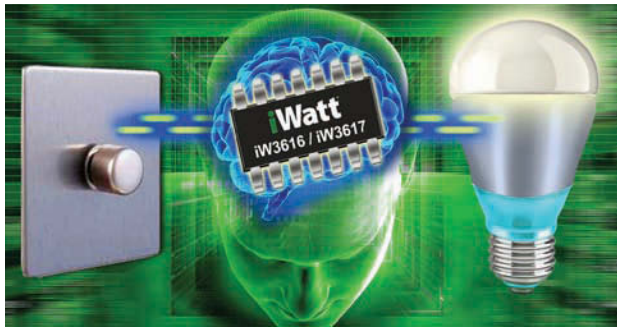
Anticipate ___Accelerate ___Achieve

Agilent Technologies

Flickerless LED drivers for SSL apps provide patented digital dimming control

Long known for its impressive market share in the mobile-device LED segment, iWatt Inc just announced a digital ac/dc SSL (solid-state lighting) LED-driver platform and the iW3616 and iW3617 drivers. *EDN* recently sat down with the iWatt folks for a demonstration of flicker, which according to the company is prevalent in LED designs.

With the LED-driver platform, iWatt takes its existing Flickerless LED drivers and increases output power to 25W or higher; lowers the bill-of-materials cost by 10% to 20%; and ensures compatibility with a wide range of installed dimmers, including residential triac-based types as well as sophisticated, digital models.



The iW3616 and iW3617 both build on the iWatt 15W iW3614 LED driver by expanding dimmer compatibility and by improving dimming and EMI performance.

The company's digital dimming algorithms—the heart of the iWatt technology—are protected by its "Adaptive dimmer detection and control for LED lamp" patent (US Patent 8,222,832). The iW3616 and iW3617 both build on iWatt's 15W iW3614 LED driver by expanding dimmer compatibility and by improving dimming and EMI performance. In space-constrained applications, they also provide a size advantage over the iW3614 by replacing the earlier driver's FETs with low-cost bipolar junction transistors; reducing circuit-protection component count and EMI filtering; and using a small, low-cost E-capacitor.

Both new drivers operate with 630- to 900-Hz dimming frequencies to allow for smooth and flicker-free dimming from 1% to 100% with tight, ±5% LED-current regulation. LED-safety features inherent in the drivers include open/short-circuit protection, input-overvoltage protection, overtemperature thermal shutdown, ac-line overvoltage/frequency protection, and LED-current derating at high temperatures.

Applications include retrofit bulbs and external drivers, ballasts, and luminaires. The digital dimmers can be used in commercial, residential, and emergency lighting.

The drivers are available in production quantities in standard, 14-lead small-outline packages. Samples are priced at 77 cents for the iW3616 and 91 cents for the iW3617, both in order quantities of 1000.

—by Carolyn Mathas

▷**iWatt**, www.iwatt.com.

Multicore platform brings integration to auto center console

Cost and space constraints have kept automakers from designing such features as connected radios, infotainment systems, and reconfigurable instrument clusters into subluxury-class cars. With backup cameras now slated to become mandatory in new US vehicles in 2015, however, integrated dashboard features are moving from the "options" side of the window sticker to the "standard" column.

Freescale Semiconductor, having surveyed the changing landscape of automotive capabilities, is extending its ARMv7-compatible Vybrid controller into the automotive market with silicon-enabled software for in-cabin features. To enable backup-camera integration, for example, the controller supports inputs from less expensive analog cameras as well as more sophisticated digital cameras, allowing the Vybrid platform to serve the whole range of automotive designs, from low-end to luxury models.

The platform's dual-core (Cortex-A5 plus Cortex-M4) architecture handles both MPU and MCU tasks on one chip, providing performance of more than 850 Dhrystone MIPS. An integrated video ADC supports direct connection of one or more analog cameras to minimize the system cost of conformance to the pending rear-view-camera mandates.

Freescale is taking its ARMv7-compatible Vybrid controller into the automotive market with silicon-enabled software for in-cabin features.

A 1.5-Mbyte on-chip SRAM and multiple package options provide scalability from low-cost, basic connected radios without external DRAM to infotainment systems with dual displays. The 2D-ACE (animation and composition engine) and OpenVG hardware acceleration reduce memory requirements and provide advanced user interfaces. Integrated CAN controllers, MLB, UART/LIN, and Ethernet with IEEE 1588 support provide standard vehicle connectivity.

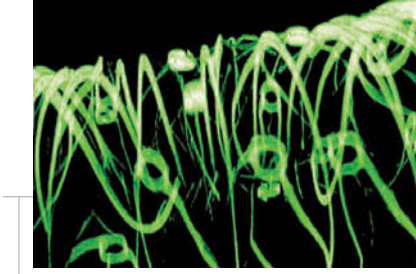
Dual USB 2.0 OTG (On-the-Go) controllers with integrated PHY, along with serial interfaces such as UART, SPI, and I^2S, provide connectivity to consumer electronic devices such as smartphones, tablets, and Bluetooth-enabled devices.

Vybrid VF series devices are included in Freescale's product-longevity program, which ensures supply for a minimum of 10 years.

—by Margery Conner

▷**Freescale Semiconductor**, www.freescale.com.

Team embeds nanowire sensors in 3-D "tissue scaffolds"



This 3-D reconstructed confocal fluorescence micrograph shows the tissue scaffold (courtesy Charles M Lieber and Daniel S Kohane).

Researchers from Boston Children's Hospital, Harvard University, and the Massachusetts Institute of Technology have added electronic sensors to engineered, 3-D "tissue scaffolds." The silicon nanowires could be used to monitor electrical activity in cells, control drug release, and test experimental drugs' effects on biological systems; ultimately, they could expedite development of tissue-engineered hearts, according to Robert Langer, David H Koch Institute professor at MIT and a senior author of the paper presenting the team's work.

Other cellular platforms have incorporated electronic sensors but comprise cells grown on planar metal electrodes or transistors. Three-dimensional scaffolds more accurately replicate natural tissues.

The researchers built their tissue scaffold using a nontoxic epoxy that yielded the required porous, 3-D structure. The embedded nanowires carry electrical signals to and from the structure's cells. The team chose silicon nanowires for the electronic sensors because the nanowires are small, stable, safe for use in human tissue, and more electrically sensitive than metal electrodes. The nanowires range in diameter from 30 to 80 nm and can detect less than 0.001W, or roughly the level of electricity in a cell.

The researchers reported growing cardiac, neural, and muscle tissue in the lab. Using the engineered cardiac tissue, they were able to monitor cells' response to the stimulant noradrenalin, according to the published paper (http://bit.ly/OpVNRK).

Columbia University biomedical engineering professor Gordana Vunjak-Novakovic, who was not on the research team, calls the work "a beautiful example of how nanoelectronics can be combined with tissue engineering to monitor the behavior of cells."

The team also embedded electronic sensors in blood vessels grown on the scaffolds and used the sensors to measure pH changes in and around the vessels. The researchers ultimately hope to engineer tissues that not only could sense an electrical or chemical event but also could respond to it appropriately, such as by releasing a drug.

"It could be a closed-feedback loop, much as [the human] autonomic nervous system is," says Daniel Kohane, director of the Laboratory for Biomaterials and Drug Delivery at Children's Hospital and a senior author of the paper.

The National Institutes of Health, the McKnight Foundation, and Boston Children's Hospital funded the research. The next steps are to perfect the technique and test the structures in animals.

—by Diana Scheben

▷**Massachusetts Institute of Technology**, web.MIT.edu.

BY BONNIE BAKER

Delta-sigma antialiasing filter with a mode-rejection circuit

The approach to the antialiasing-filter design for the delta-sigma data converter is significantly different from the approach you would use for a SAR (successive-approximation register) or pipeline (high-speed) converter. With SAR and pipeline converters, you have systems that evaluate one sample at a time. In both cases, the analog signal is "grabbed" and stored on the converter's input capacitor array. These converters evaluate the stored signal and provide a digital representation of that single sample. With both devices, the target frequency for the multiorder, antialiasing filter is the converter's Nyquist frequency.

The delta-sigma converter's input modulator samples the input analog signal numerous times at a high sample rate (F_S, **Reference 1**). The following sinc digital filter resamples and converts a group of these modulator samples to an output digital representation. The conversion process from the modulator's string of samples to a 24-bit digital code is significantly slower (F_D, **Reference 1**) than the sample rate of the delta sigma's input structure. Consequently, the delta-sigma converter has two sample rates (F_S, F_D). The first-order antialiasing filter's target frequency, however, is the output data rate, F_D. You can find the fundamental antialiasing-filter design concepts for a delta-sigma converter in **Reference 1**.

Once you establish the target antialiasing frequency of F_D, you can quickly define the theoretical design formulas, as **Reference 2** discusses. The calculation for this theoretical evaluation takes into account resistor noise and converter bits. To determine the theoretical filter resistance (**Figure 1**), use the following **equation**:

$$R_{FLT(MAX)} = \frac{10^{-(ER \times 0.602)}}{4 \times k \times T \times F_D},$$

where ER is the specified effective resolution from the ADC manufacturer's data sheet, k is Boltzmann's constant, and T is the temperature in Kelvin. To determine the theoretical filter capacitance, use the following **equation**:

$$C_{FLT} = \frac{1}{2 \times \pi \times R_{FLT} \times F_D}.$$

Note that the circuits and the discussions presented in **references 1** and **2** address only the reduction of differential noise, with no regard to the input impedance of the converter or common-mode noise.

In terms of the converter's input impedance, the capacitors of a switched-capacitor-input, delta-sigma converter are continuously charged and discharged while measuring a voltage between AIN_P and AIN_N (**Figure 2**, available online at www.edn.com/4395286). These internal capacitors (C_B, C_{A1}, and C_{A2}) are relatively small when compared with the external circuitry. Consequently, the average input impedance appears to be resistive. The converter's capacitor values and modulator switching rate set this resistive value.

To measure the common-mode input impedance of the structure in **Figure 2**, tie AIN_P and AIN_N together and measure the average current that each pin consumes during conversion. To measure the differential input impedance, apply a differential signal to AIN_P and AIN_N and measure the average current that flows through the pin to V_A. The common- and differential-mode resistance can range from hundreds of kilohms to hundreds of megohms. Those values depend on the circuitry following the input switching-capacitor structure inside the converter. The value of $R_{FLT}/2$ must be at least 10 times lower than the converter's input impedances.

The two common-mode capacitors, C_{CM_P} and C_{CM_N}, attenuate high-frequency common-mode noise. The differential capacitor should be at least an order of magnitude larger than the common-mode capacitors because mismatches in the common-mode capacitors cause differential noise.

If the input signal to any ADC contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, bandlimit the input signals containing noise and interference components. The digital filters in delta-sigma converters provide some high-frequency noise attenuation, but the digital sinc filter cannot completely replace an antialiasing filter. When designing an input filter circuit, factor in the interaction between the filter network and the input impedance of the converter. EDN

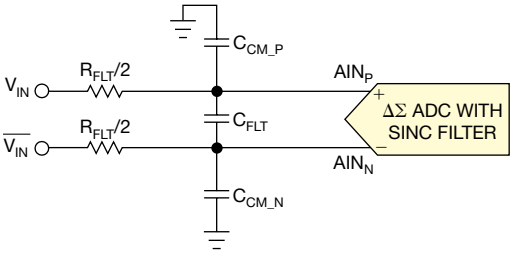


Figure 1 This complete filter attenuates differential noise with $R_{FLT}/2$ and C_{FLT}, and common-mode noise with C_{CM_P} and C_{CM_N}.

REFERENCES

1 Baker, Bonnie, "Using an analog filter to inject noise," *EDN*, July 23, 2009, http://bit.ly/RheNm9.
2 Baker, Bonnie, "Analog filter eases delta-sigma-converter design," *EDN*, June 12, 2008, http://bit.ly/NLG2Se.

Protecting IGBTs with Avago Optical Isolation Amplifiers

Introduction

Insulated-gate bipolar transistors (IGBTs) can fail when subjected to overloads and overvoltages. Isolation amplfiers (iso-amps) can respond quickly to over-current and overload conditions when used on the output phases and the DC bus.

A typical block diagram of a power converter in an AC motor drivet consists of an inverter that converts the DC bus voltage to AC power at a variable frequency to drive the motor. IGBTs are expensive power switches that form the heart of the inverter. These power devices must operate at a high frequency and must be able to withstand high voltages.

Iso-amps such as the ACPL-C79A work with shunt resistors to accurately measure power converter current even in the presence of high switching noise. When used with a resistive divider, iso-amps work as precision voltage sensors to monitor the DC bus voltage. The microcontroller monitors the current and voltage information from the iso-amps and uses the data to calculate the feedback values and output signals needed to for fault management in the IGBTs and power converters.

Fault Protection

However, the IGBT protection must be such that its cost doesn't affect that of the motor drive system. IGBT gate drivers such as the ACPL-332J and current sensors with protection features can detect faults economically in this regard. They eliminate the need for separate detection and feedback components.

Over-current conditions in an IGBT can arise from a phase-to-phase short, a ground short or a shoot through. The shunt + iso-amp devices on the output phases and DC bus can, besides measuring current, detect such faults.

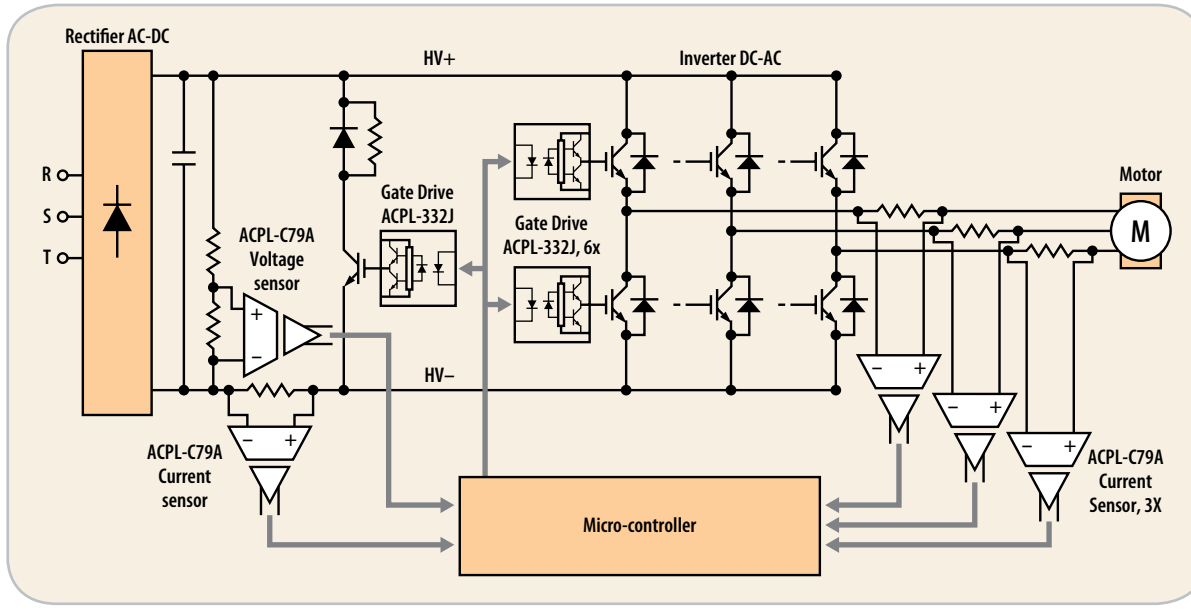
Typical IGBT short-circuit survival times are rated up to 10 µsec. So any protection must prevent this limit from being exceeded. Within 10 µsec, the circuit must detect the fault, notify the controller and complete the shutdown. Iso-amps use various methods to get these results.

For instance, the ACPL-C79A has a fast, 1.6 µsec response for a step input. That lets the iso-amp capture transients during short-circuits and overloads. The signal propagation delay from input to output at mid point is only 2 µsec, while it takes just 2.6 µsec for the output signal to catch up with input, reaching 90% of the final levels.

Another example is the HCPL-788J, which responds quickly to over-currents using a different approach. In addition to the signal output pin, it has a Fault pin that toggles quickly from High to Low level when over-current occurs. This iso-amp provides ±3% measurement accuracy.

In the fault feedback design, nuisance tripping can be an issue. This is a triggering of fault detection in the absence of any damaging fault condition. To avoid false triggering, the HCPL-788J employs a pulse discriminator that blanks out di/dt and dv/dt glitches. The advantage of this method is that

Figure 1: Block diagram of power converter in a motor drive



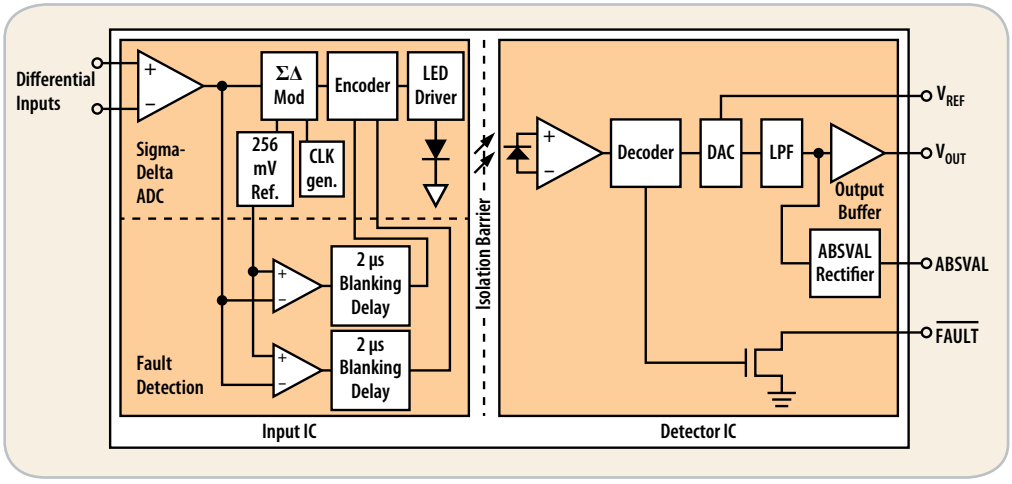


Figure 2: In the HCPL-788J iso-amp, the differential input voltage is digitally encoded by a sigma-delta A/D converter and then fed to the LED driver, which sends the data across the isolation barrier to a detector and D/A.

rejection is independent of amplitude, so the fault threshold can be set to low level without risking nuisance tripping.

The circuit that detects faults quickly contains two comparators in the Fault Detection block to detect the negative and positive fault thresholds. The switching threshold is equal to the sigma-delta modulator reference of 256 mV. The outputs of these comparators connect to blanking filters with a blanking period of 2 µsec and then go to the Encoder block.

To ensure speedy transmission of the fault status across the isolation boundary, two unique digital coding sequences represent the fault condition, one code for negative, the other for affirmative. Detection of a fault interrupts the normal data transfer through the optical channel and replaces the bit stream with the fault code. These two fault codes deviate significantly from the normal coding scheme, so the decoder on the detector side immediately recognizes the codes as a fault conditions.

The decoder needs about 1 µsec to detect and communicate the fault condition across the isolation boundary. The anti-aliasing filter adds a 400 nsec delay to give a propagation delay of 1.4 µsec. The delay between the fault event and the output fault signal is the sum of the propagation delay and the blanking period (2 µsec) for an overall 3.4 µsec fault detection time.

The Fault output pin allows fault signals from several devices to be wire-ORed together forming a single fault signal. This signal may then be used to directly disable the PWM inputs through the controller.

Overload Detection

An overload condition refers to a situation where the motor current exceeds the rated drive current, but without imminent danger of failure, as when the motor is mechanically overloaded or is stalling because of a bearing failure

Inverters usually have an overload rating. The time period of the allowable overload rating depends on the time it takes before overheating becomes an issue. A typical overload rating is 150% of nominal load for up to one minute.

The ACPL-C79A accepts full-scale input range of ±300 mV and the data sheet specifications are based on ±200 mV nominal input range. Designers can choose the overload threshold at or in between either of the two figures. Usually the measurement accuracy of the overload current is less stringent than that of the normal operating current. Here, setting the threshold near 300 mV is a good choice. This allows full use of the iso-amp's dynamic input range. However, a threshold set at 200 mV ensures accurate measurement of the overload current. Once the voltage levels are decided, the designer must choose appropriate sense-resistor value according to corresponding current level.

The HCPL-788J includes an additional feature, the ABSVAL output, which can be used to simplify the overload detection circuit. The ABSVAL circuit rectifies the output signal, providing an output proportional to the absolute level of the input signal. This output is also wire OR-able. When three sinusoidal motor phases are combined, the rectified output (ABSVAL) is essentially a DC signal representing the RMS motor current. This DC signal and a threshold comparator can indicate motor overloads before they can damage to the motor or drive.

Overvoltage Detection

The DC bus voltage must also be continuously controled. Under certain operating conditions, a motor can act as a generator, delivering a high voltage back into the DC bus through the inverter power devices and/or recovery diodes. This high voltage adds to the DC bus voltage and puts a very high surge on the IGBTs. That surge may exceed the maximum IGBT collect-emitter voltage and damage them.

The miniature iso-amp (ACPL-C79A) is often used as a voltage sensor in DC bus monitoring applications. A designer must scale down the DC bus voltage to fit the input range of the iso-amp by choosing R1 and R2 values to get an appropriate ratio.

BY PALLAB CHATTERJEE

Solid-state drives head for the enterprise

In recent months, SSD (solid-state drive) providers have begun touting products that allow multilevel-cell flash memories to be used in enterprise-class drives for data-center and enterprise applications. These drives are going into applications that for decades have been the domain of 7200- and 15,000-rpm hard drives, as well as LTO (linear tape-open) and other tape- and DRAM-based data-storage devices.

Enterprise storage applications differ from their consumer counterparts on several specification fronts: The enterprise drives operate at both higher and lower temperatures than consumer drives, have high-duty-cycle data throughput, are powered on 24/7, and must store data for a typical operating life of five to seven years (mean time between failures of 44,000 hours). The information stored on enterprise drives also varies in data size, ranging from transactional-data stores, which involve very large numbers of small files; to small queries on large databases; and on to very large video- and database-file stores that are accessed by a shared compute system.

The increase in the amount of data stored in data centers and the cloud has made the limits of traditional storage technology the bottleneck for data access, and as a result solid-state drives have risen to dominance as a new tier of storage subsystem. The first SSDs were made with DRAM, which offered high speed and throughput but required constant power to maintain the data stored. The resultant cost of high-capacity DRAM-based storage on a power, performance, and capacity basis limited its application range.

Newer SSDs use nonvolatile, NAND flash technology, which provides high storage capacity and long data retention without requiring power to maintain the data—only to access it. There are trade-offs, however: Whereas DRAM has symmetric read/write performance and can indefinitely be written to and read as long as it is powered, flash read and write access times are asymmetrical. Flash also has a finite operating life, based on how many times something is written and, under certain conditions, how many times it is read.

These fundamental process-based read and write characteristics cannot be handled at the operating-system level for an interface but, rather, require design-specific firmware and functionality-controlled programming that are unique to each drive manufacturer. Such variation and diversity ratchet up the cost and complexity of maintaining a drive bank on the order of tens of thousands of drives, which is common these days.

Flash technology is advancing in two directions: through process-geometry scaling, which enables a greater number of cells in the same chip area, and through architectural tweaks that increase the number of data bits each flash cell can store. The state-of-the-art process-node range for production memory cells is 22 to 19 nm; the next-generation node is 14 nm. Such processes allow the manufacture of very large chips, with more than 8 billion cells on a single die.

Meanwhile, to meet the ever-rising demand for storage at reduced memory cost, flash manufacturers have pushed the technology to allow a single cell to store multiple bits of data. Flash variants available or in development today include SLC (single-level cell), MLC (multilevel cell), TLC (triple-level cell), and QLC (quad-level cell) devices, respectively able to store 1, 2, 3, and 4 bits per cell.

SLC NAND flash with ECC (error-correcting code) offers 100,000 program/erase cycles and a data-retention lifetime of 10 years; MLC NAND, also with ECC, offers 3000 to 10,000 program/erase cycles. TLC NAND flash offers 250 to 500 program/erase cycles.

The increase in the amount of data stored in data centers and the cloud has made the limits of traditional storage technology the bottleneck for data access. SSDs now dominate.

QLC NAND flash emerged in 2011. Developers include Intel Corp, Micron Technology Inc, Samsung, SanDisk, and Toshiba.

What's clear is that non-SLC technologies in their native form do not meet the requirements for enterprise applications. New DSP, ECC, and programming-waveform methods, however, are emerging to make these high-density technologies viable for enterprise storage. Developers are working on these technologies independently, and largely at the firmware level, to support flash cores from multiple vendors, and solutions are beginning to enter the marketplace. EDN

Pallab Chatterjee has been an independent design consultant since 1985.

WANT MORE?

- Go to www.edn.com/learning/teardowns for more Teardowns.
- For data sheets on the devices discussed in this Teardown and thousands of other parts, go to www.datasheets.com.

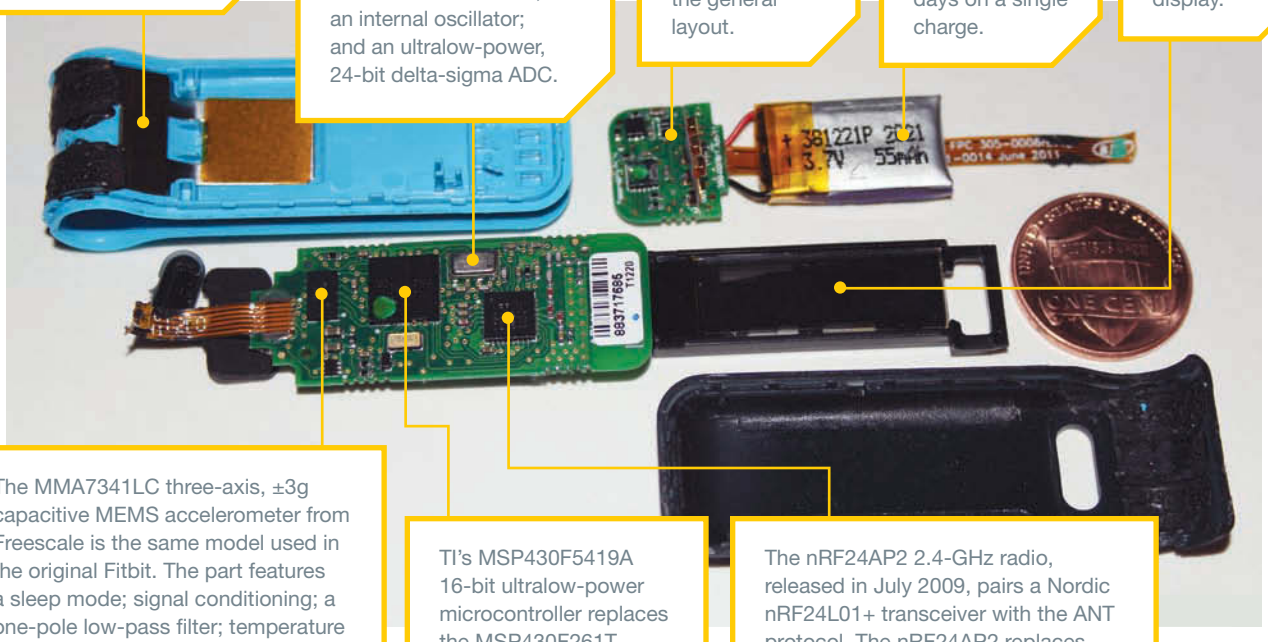
High-res pressure sensor brings stair-track capability to Fitbit Ultra

The Fitbit Ultra is the second generation of Fitbit Inc's popular personal health-monitoring device, which tracks your movements and downloads the data wirelessly to your PC. The first Fitbit distinguished itself from a crowded field by letting users upload their tracking data online, where it could be integrated into a personalized online health and fitness program. I tore down the original Fitbit shortly after its introduction in 2008 (www.edn.com/4394918). Though the development effort ultimately was successful, the team had spent many hours trying to roll its own wireless interface before finally giving up and contacting Nordic Semiconductor.

The first-generation Fitbit was easy to lose, and it didn't have solid stair-tracking capability. The Ultra—which, like the original, sells for $99—sports a more secure physical design and adds a high-resolution (20-cm) barometric pressure sensor from MEAS Switzerland SA for monitoring changes in step height.

The Ultra swaps Texas Instruments' MSP430F261T microcontroller for the lower-power F5419A, but it retains Freescale Semiconductor's MMA7341LC three-axis MEMS accelerometer. Freescale offers a full activity monitor reference design at http://bit.ly/OAAAB2.

Proprietary algorithms from Fitbit help keep the Ultra competitive in the low-power, high-performance arena.



The package base shows the spring on the left. Users of the first Fitbit complained that the unit was easy to lose (I lost mine), so the Ultra offers a stronger spring; a handy clip holder; and the ability to place the device in a pocket, rather than on a belt or the hip.

MEAS Switzerland's MS5607-02BA barometric pressure sensor module is the big addition in the Ultra. Combined with Freescale's MMA7341 and Fitbit's proprietary algorithms, the sensor lets the Ultra track stair steps. It provides 20-cm altitude resolution and has SPI and I^2C interfaces; an internal oscillator; and an ultralow-power, 24-bit delta-sigma ADC.

The external contacts on the main power board are lifted up to reveal the general layout.

The 3.7V, 55-mAhr, Li-ion polymer battery lasts between five and seven days on a single charge.

Users can personalize the 1×0.25-in. blue organic LED display.

The MMA7341LC three-axis, ±3g capacitive MEMS accelerometer from Freescale is the same model used in the original Fitbit. The part features a sleep mode; signal conditioning; a one-pole low-pass filter; temperature compensation; and g-Select, which lets one device gauge multiple levels of acceleration.

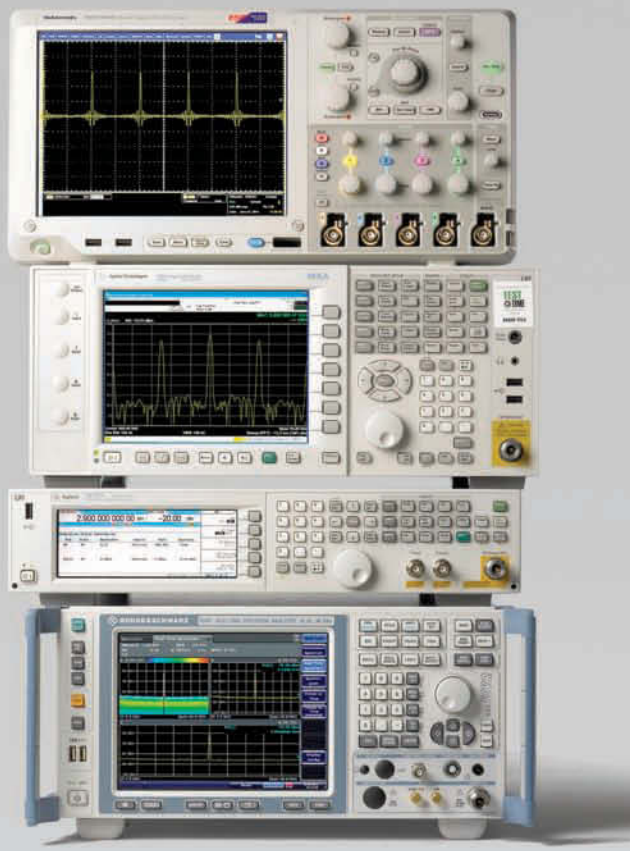
TI's MSP430F5419A 16-bit ultralow-power microcontroller replaces the MSP430F261T used in the original Fitbit and comes with 128 kbytes of flash, 16 kbytes of RAM, and a 12-bit ADC.

The nRF24AP2 2.4-GHz radio, released in July 2009, pairs a Nordic nRF24L01+ transceiver with the ANT protocol. The nRF24AP2 replaces the nRF24AP1 used in the first Fitbit. The newer radio reduces peak current to 17 mA and cuts average current by up to 75%, according to ANT Wireless and Nordic.

MathWorks®

Hardware Support includes
Agilent, Tektronix, LeCroy, Rohde & Schwarz, National Instruments, Anritsu, Keithley, Yokogawa, Tabor, Pickering, and more

Protocols and Standards supported include
GPIB, LXI, IVI, PXI, AXIe, TCP/IP, VISA, USB, UDP, and RS-232



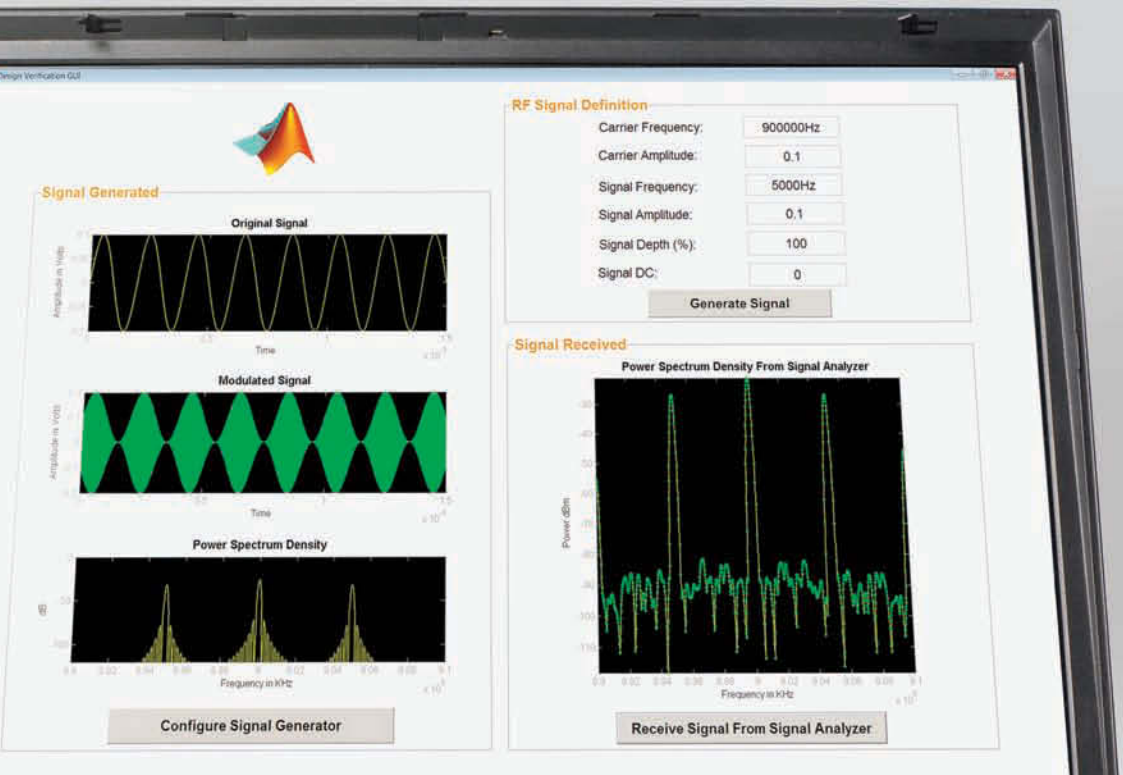
CONNECT MATLAB TO YOUR TEST HARDWARE

with INSTRUMENT CONTROL and DATA ACQUISITION TOOLBOXES

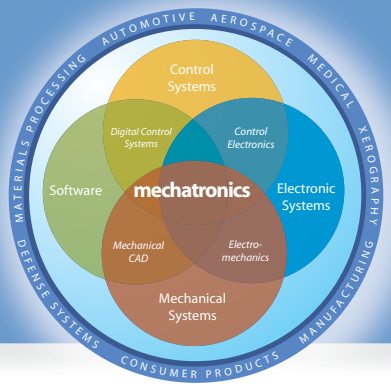
Connect your test equipment directly to MATLAB using standard communication protocols and instrument drivers that support thousands of instruments. You'll be able to analyze and visualize your results as you collect them, using the full power of MATLAB.

MATLAB® & SIMULINK®

Find it at
mathworks.com/connect
supported hardware list
trial request



UBM Electronics
DesignNews EDN
MECHATRONICS IN DESIGN
FRESH IDEAS ON INTEGRATING MECHANICAL SYSTEMS, ELECTRONICS, CONTROL SYSTEMS, AND SOFTWARE IN DESIGN



That fictitious force

The ubiquitous MEMS gyroscope uses it—but what is it?

By Kevin C Craig, PhD

Imagine you are on a merry-go-round that is turning at a constant rotational speed. You are standing near its center, and you start walking at a constant speed along a straight line painted radially on its floor from its center to its outer edge (**Figure 1**). What forces will you feel? The answer to that question will help explain how a MEMS gyroscope works.

Gyroscopes, invented in 1817, are used today in vehicle-control, aviation, aerospace, navigation, robotic, and military applications. MEMS gyroscopes have enabled applications in consumer electronics, such as camera stabilization and interactive video games. Numerous smartphone apps leverage the MEMS gyro's capabilities.

Engineers know that the forces of significance in everyday practice are physical-contact forces, such as friction, and those that act at a distance; that is, electromagnetic and gravitational forces. But what about inertial force, centrifugal force, and the mysterious Coriolis force—named for Gaspard-Gustave Coriolis? Aren't they real forces? No.

Inertial force, or mass times absolute acceleration, is equal to the physical force you must apply to a mass to cause it to accelerate. Centrifugal force, or mv^2/r, is equal to the physical force you need to apply perpendicular to the trajectory of the mass to cause it to move along a circular path of radius r at a constant speed. We have all experienced these forces. But what is the Coriolis force? **Figure 2** helps answer the question.

If we know our absolute acceleration during this motion—that is, with respect to the ground reference frame R—then we know the forces we will feel. The absolute acceleration is the difference between the absolute velocity at points 2' and 1 divided by Δt, in the limit as $\Delta t \to 0$. First, consider the Y-direction acceleration: Δv_Y=[component 2+component 4]−v. Divide this by Δt, and take the limit as $\Delta t \to 0$. The result is that $a_Y = -r\omega^2$. It is called the centripetal acceleration and is due solely to component 4. The velocity, v, has no effect on the centripetal acceleration; it depends only on position r and angular speed ω.

Next, consider the X-direction acceleration: Δv_X=[component 1+component 3]−rω. Divide this by Δt, and take the limit as $\Delta t \to 0$. The result is that $a_X = 2\omega v$. It is called the Coriolis acceleration and is independent of position r. It represents the sum of two identical contributions: The effect of ω changing the orientation of v is exactly the same as the effect of v carrying rω to a different radius, changing its magnitude. In vector notation, the expression for the absolute acceleration of point P, in terms of unit vectors of the body-fixed axes, is as follows:

$$\vec{a}^{P} = [\vec{\omega}^{B} \times (\vec{\omega}^{B} \times \vec{r}^{OP})] + 2(\vec{\omega}^{B} \times \vec{v}^{P}) = 2\omega v\hat{i} - r\omega^2\hat{j}$$

A gyroscope is a device that measures the angular velocity of a body about a certain axis of rotation. Classical gyroscopes are bulky, expensive, and unreliable. MEMS technology has the advantages of batch fabrication, small size, and low price. Almost all MEMS gyroscopes rely on vibrating mechanical elements that are driven to oscillate in the plane of the chip and to respond to rotation by another vibratory motion in the same plane. The main principle of MEMS gyroscopes is the transfer of energy between two modes of vibration, the drive and the sense modes, through the Coriolis acceleration. A fundamental understanding of the Coriolis force led to the development of this exciting technology. EDN

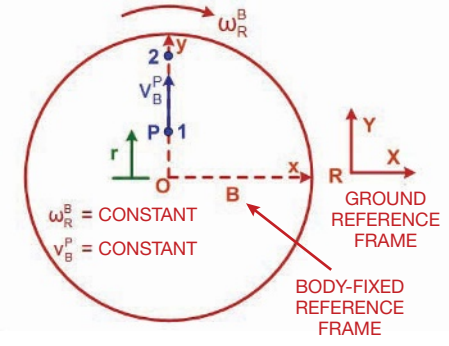


Figure 1 The physical situation: What forces will we feel?

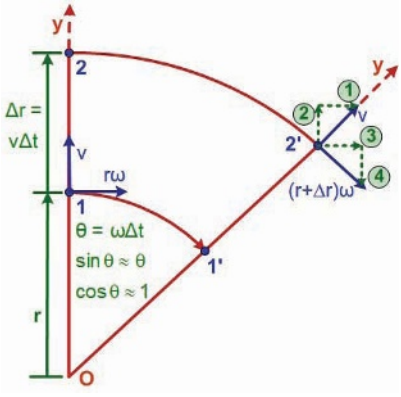
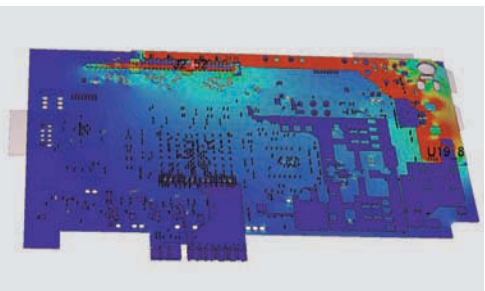


Figure 2 Changes in absolute velocity during the motion: If we know our absolute acceleration, then we know the forces we will feel.

CST STUDIO SUITE 2012

Discover what happens...

Making Sense of the Real World – System Level EM Simulation



IR-drop : surface current density distribution on multilayer PCB

Components don't exist in electromagnetic isolation. They influence their neighbors' performance. They are affected by the enclosure or structure around them. They are susceptible to outside influences. With System Assembly and Modeling, CST STUDIO SUITE 2012 helps optimize component as well as system performance.

Involved in signal or power integrity analysis? You can read about how CST technology was used to simulate and optimize a digital multilayer PCB's performance at www.cst.com/pcb.

If you're more interested in EMC/EMI or microwave components, we've a wide variety of worked application examples live on our website at www.cst.com/apps.

Get the big picture of what's really going on. Ensure your product and components perform in the toughest of environments.

Choose CST STUDIO SUITE 2012 – complete technology for 3D EM.

CST

CHANGING THE STANDARDS

Your question:

What does the R&S®RTO have to offer at 4 GHz bandwidth?

Our answer: The highest precision and fastest acquisition rate in its class. The new R&S®RTO oscilloscope is a powerful solution for developing digital, analog and RF designs. The extremely low-noise frontend offers the full measurement bandwidth of 4 GHz even at the smallest scaling (1 mV/div).

With an acquisition rate of 1 million waveforms per second, fast FFT analysis, high dynamic range, and a maximum bandwidth of 4GHz, the new R&S®RTO model is ideal for frequency domain measurement.

Come see what we've built.
rohde-schwarz-scopes.com

Attend our free technical sessions at DESIGN East 2012
Room 209 - Hynes Convention Center, Boston MA
Tuesday, September 18

- Near field communications technology and measurements
- Synchronous time and frequency domain analysis of embedded systems
- Wideband complex modulation analysis using a real-time digital demodulator
- Debugging and evaluating analog to digital converters

For a one-of-a-kind Tervis® Tumbler*, bring this ad to a technical session or Booth #700

* while supplies last

ROHDE&SCHWARZ

HEADLESS ATE SYSTEM INCREASES PRODUCTION RELIABILITY AND EFFICIENCY

A SYSTEMS INTEGRATOR DESIGNED AND DEPLOYED A RELIABLE AUTOMATED TEST-EQUIPMENT SYSTEM THAT'S SIMPLE TO OPERATE AND MAINTAIN, WITHOUT REQUIRING PCs ON THE PRODUCTION FLOOR.

BY ROB PUTALA • BLOOMY CONTROLS INC

Many manufacturers use manual test equipment that comprises stand-alone COTS (commercial off-the-shelf) test instruments, such as digital multimeters, oscilloscopes, and hipot testers. COTS test instruments often require configuration and programming using their front panels. The required sequences of button presses to program these instruments through multiple selection menus can be cumbersome and prone to errors, and can subject the test process to test inconsistency. Quality-control processes are driving manufacturers to automate test equipment in order to ensure consistent configuration control and data collection.

IMAGE: SHUTTERSTOCK

PC-based ATE (automatic test equipment) systems provide control of the testing process, manage instrument configurations, increase test throughput, and address the issues associated with manual test. Although PC-based ATE is widely accepted, many manufacturers still test manually, for a number of reasons.

The PC-based ATE systems deploy a PC with each test system, which requires a minimum level of operator skill and IT maintenance. For benchtop systems, the keyboard, monitor, and mouse occupy precious space on the production floor. Operator skill levels and language barriers may necessitate significant training for some manufacturers. In particular, setup and configuration during product changeover can be challenging. Also, the accessibility of Web browsing and other PC software can distract operators using PC-based ATE. Responsibility for IT administration of PCs on the production floor is a gray area at some organizations.

Such issues can lead to operator error, inefficiency, and inconsistency in the testing process. To avoid those problems, a simple, headless ATE system may be all you need in a facility with multiple manual test stations; operator usability concerns; or a low-volume, high-changeover product mix.

AT A GLANCE

- Production test systems often need very simple user interfaces that provide just enough control for the application.
- In the headless ATE system, an embedded controller board provides real-time processing, instrument control, and analog and digital I/O, plus LAN communications to a remote PC.
- A supervisory application running on a remote PC lets engineers and managers monitor production status and operator efficiency on the floor.

HEADLESS ATE SYSTEM

Engineers at Bloomy Controls developed a headless ATE system (www.bloomy.com/headless_ate) that is simple to operate and doesn't require PCs on the production floor. The system is headless because it doesn't need a keyboard, monitor, touchscreen, or mouse; instead, it contains a physical interface comprising a few mechanical buttons, LEDs, and an optional bar-code scanner. A supervisory application, located on any PC connected to the manufacturer's LAN (local-area network), can monitor and manage multiple headless ATE systems. The supervisory application lets managers control configurations sent to each headless ATE system and track the efficiency of each station, production line, and operator.

Bloomy Controls' headless ATE system uses a 3U (three-unit) rack-mount cabinet with a 1U shelf that contains a National Instruments Single-Board RIO (reconfigurable I/O) implementation running LabVIEW, a power supply, and an operating panel. In addition to the 1U shelf, the cabinet contains the requisite COTS test instruments for each test system.

Figure 1 shows the system, which in this application uses an ac power source. Most COTS test instruments come in 1U and 2U forms that will fit into a 3U enclosure. The headless ATE system in **Figure 1** contains a 2U COTS programmable ac power supply. A system clock time-stamps test activities that a supervisory application can record.

The headless system provides only the most basic operator controls, implemented by manipulating large mechanical buttons on the front panel, which can be configured and modified to meet the needs of the test process. In the headless ATE system in **Figure 1**, the LED-illuminated buttons are clearly labeled, in order, Test, Stop, and Retest. Green and red LED panel indicators, labeled Pass and Fail, inform the operator of the test result. The front-panel buttons and an optional bar-code reader are the only operator interface; consequently, the headless ATE system requires minimal operator training and eliminates the PC and associated maintenance.

The buttons and LEDs are monitored and controlled via a digital-I/O port in the NI Single-Board RIO (**Figure 2**), which contains a real-time processor, an FPGA, and analog and digital I/O. The board provides integrated communications via such protocols as Ethernet, USB, CAN, and RS-232 to control the COTS instruments, communicate to the UUT (unit under test), and connect to the supervisory PC.

SUPERVISORY APPLICATION

The supervisory application (www.bloomy.com/ate_supervisor) lets production managers monitor multiple headless ATE systems and provides cen-

Figure 1 The headless ATE system uses a 3U cabinet containing an NI Single-Board RIO, a power supply, and/or one or more COTS test instruments.

Figure 2 The NI Single-Board RIO contains a real-time processor, an FPGA, integrated communications, and analog and digital I/O.

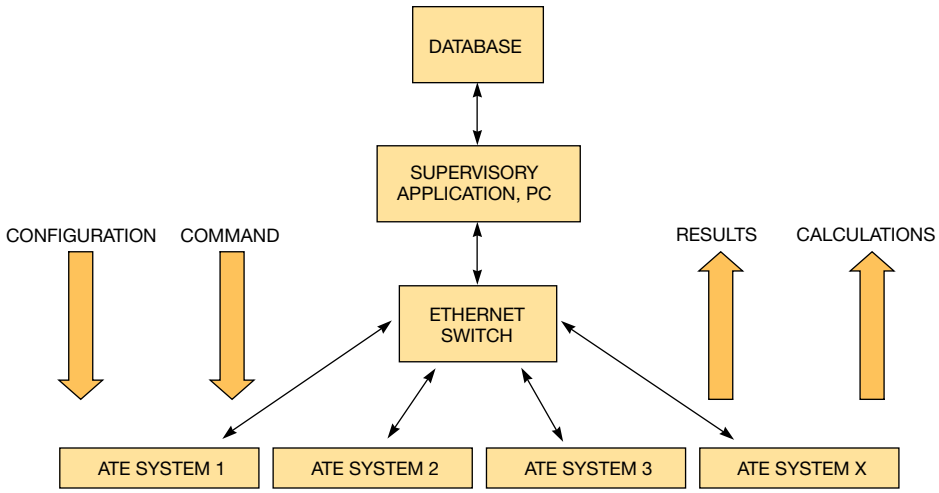


Figure 3 Multiple headless ATE systems can connect to a network through an Ethernet switch and to a remote PC running the supervisory application over the LAN.

tral control of the instrument configurations and data collection. Managers can install the supervisory application on a PC in their office or any PC in the production facility and immediately gain control over the test process.

Regardless of the number of headless ATE systems a manufacturer deploys, every test sequence and setting is displayed and controlled from the supervisory application.

Also, the headless ATE system and the supervisory application are readily scalable and easy to use for multiple production cells. The supervisory application can automatically detect and configure new headless ATE systems as soon as they are added to the LAN; likewise, if a headless ATE system is disconnected from the LAN, the supervisory application detects the disconnection and alerts managers via e-mail.

The ability to configure all of the headless ATE systems from the supervisory application eliminates operator error in setup or product-change procedures. Each headless ATE system sends test results, calculations, and any other desired data to the supervisory application, where it is displayed, analyzed, and stored in a database.

Figure 3 is a block diagram that illustrates how the supervisory application controls headless ATE systems. The

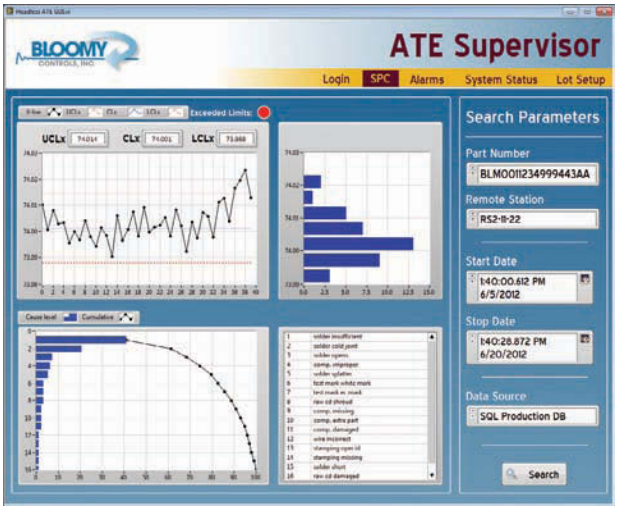


Figure 4 The supervisory display screen contains a Pareto chart (lower left), histogram (upper right), and SPC X-bar chart (upper left).

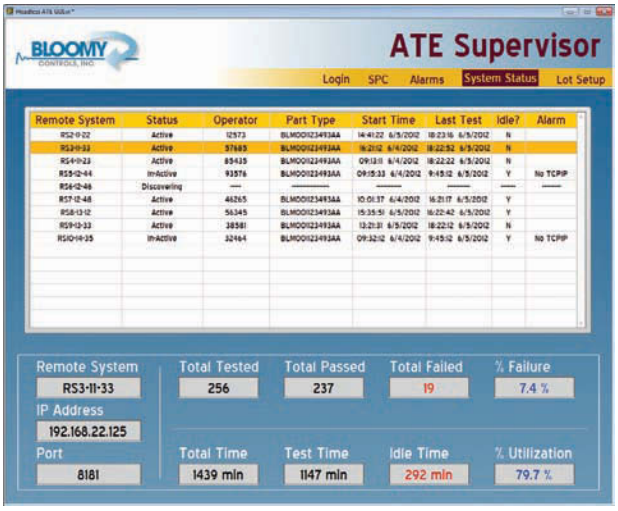


Figure 5 ATE Supervisor's system-status display screen shows each headless ATE system on the network, along with test statistics.

headless ATE system time-stamps and records all test activities to ensure accurate calculations of factors such as yield or test throughput. The time-stamped data lets the supervisory application track operator efficiency at each test station. Managers can view the test results, yields, SPC (statistical process control) analysis, and operator efficiency through the supervisory application, which connects to the production database.

Figure 4 shows the SPC display screen—the supervisory application that production managers frequently view. The screen displays a histogram,

Pareto chart, and X-bar and range SPC charts based on the data recording from the test process.

The supervisory application can generate alerts and alarms throughout the test process. The app can send e-mails to a list of supervisors to inform them that an event has occurred.

For example, an alarm might sound if three consecutive UUT failures occur on any one system, or an alarm can trigger an e-mail to production managers when yield drops below a specified value. The ATE supervisor's system-status screen displays the status, operator ID, and test times of each headless ATE system on the LAN (**Figure 5**).

The headless ATE system provides a simple operator panel that reduces the possibility of operator error and minimizes operator training. The supervisory application provides repeatable setup of the headless ATE systems and test sequences, as well as error-free data recording and analysis. Real-time SPC reporting and analysis allow production managers to view the data at any time from any designated PC on the LAN and to receive alerts when there are significant changes in the process or operator efficiency.

By simplifying the operator panel and centralizing the setup and configuration of multiple headless ATE systems, the overall system dramatically improves test-process reliability. EDN

ACKNOWLEDGMENT

This article originally appeared on EDN's *sister site,* Test & Measurement World, *at www.tmworld.com/4389754.*

AUTHOR'S BIOGRAPHY

Rob Putala is a senior systems engineer at Bloomy Controls Inc. Putala holds a bachelor of science degree in electrical engineering from Michigan Technological University (Houghton, MI) and a master's degree in business administration from the University of Notre Dame (Notre Dame, IN). He has more than 30 years of test-engineering experience.

JOIN THE CONVERSATION

To comment on this article, go to www.edn.com/4395308.

30 YEARS OF DSP

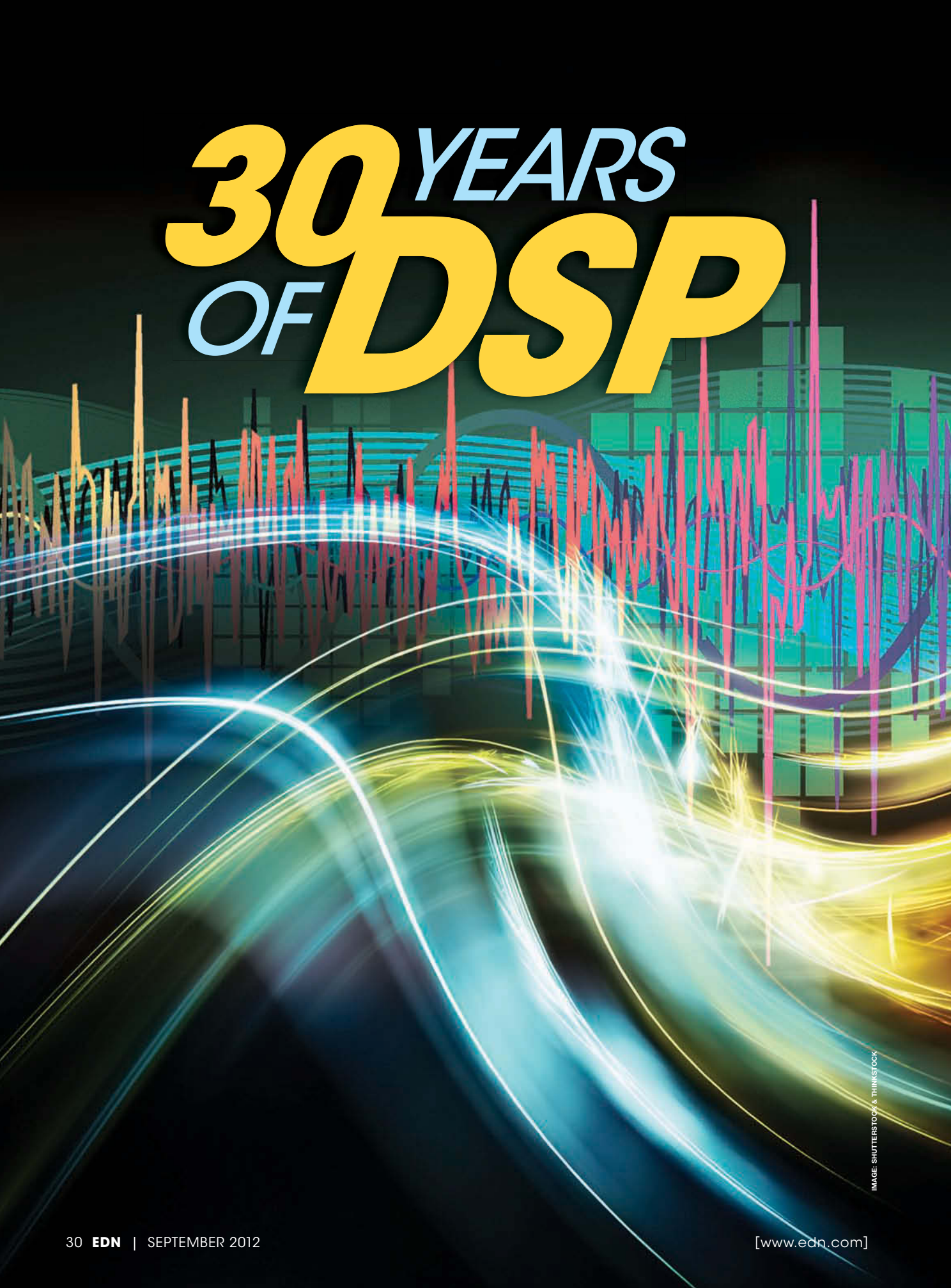
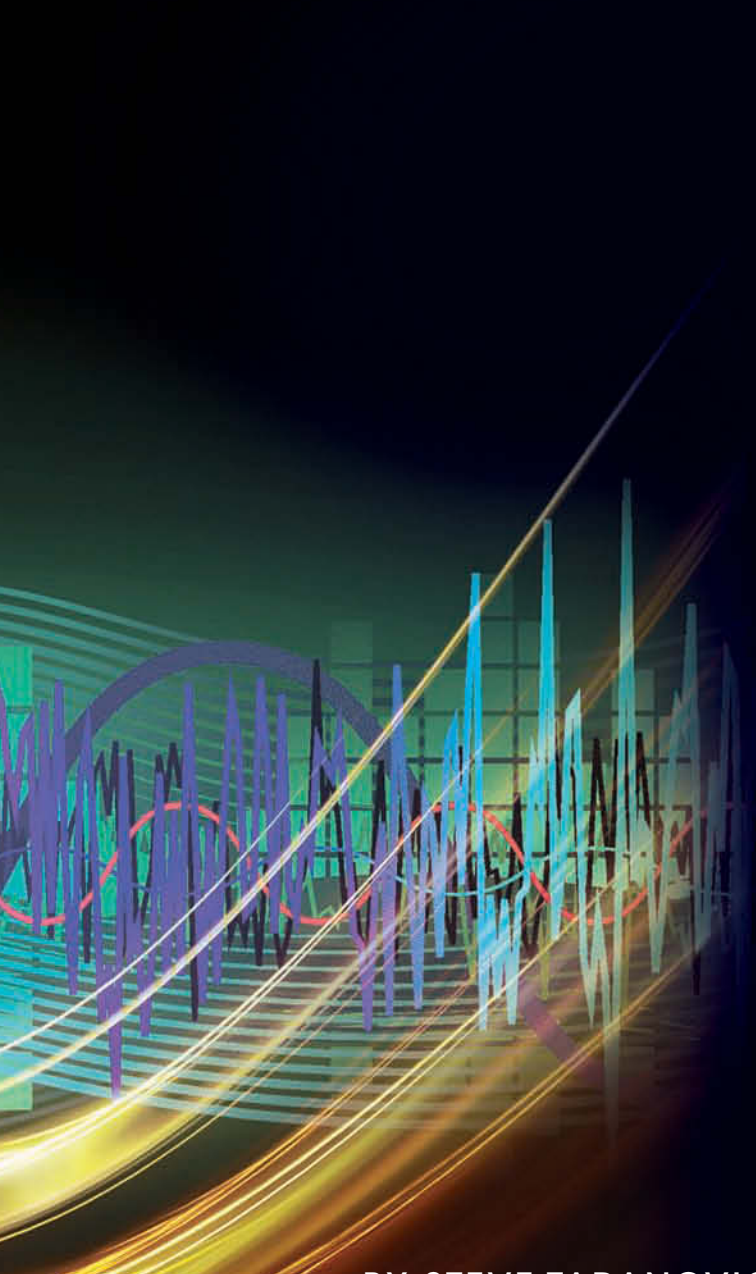


IMAGE: SHUTTERSTOCK & THINKSTOCK



THE SPEAK & SPELL SPEECH CHIP HELPED GROW AN ECOSYSTEM OF DSP DEVICES, TOOLS, AND APPLICATIONS. TODAY, A HETEROGENEOUS MIX OF PROCESSORS HANDLES COMPLEX SIGNAL-PROCESSING TASKS.

BY STEVE TARANOVICH • SENIOR TECHNICAL EDITOR

As Texas Instruments principal fellow Gene Frantz tells it, the aha moment for the company's DSP pioneers came in the late 1970s, shortly after TI's seminal Speak & Spell learning toy hit retailers' shelves. Frantz recalls that a customer asked, "If you can [use DSP to] add speech synthesis to a toy, what else can you use it for?"

This year, as TI celebrates its 30th year in the DSP market, that long-ago question has been answered many times over. Without DSP and the advances it has enabled in audio, graphics, and multimedia processing, there would be no "infotainment" content, no smartphones or tablets, no Internet or ecosystem of apps.

TI's "toy" technology not only moved the company into a new business but also set the stage for developments by TI, its competitors, and tool vendors that have pushed DSP technology into diverse applications and markets. At the same time, traditional DSP devices have seen competition from an array of alternative signal-processing platforms, including CPUs with DSP-oriented features; digital signal controllers, which pair a DSP core with a microcontroller; FPGAs that are used to design custom data paths for digital signal processing or even to create custom programmable processors; and, most recently, massively parallel processing graphics processors that can tackle data-parallel problems.

The roots of DSP technology predate the Speak & Spell by several years. In the early 1970s, scientists began using off-the-shelf TTL discrete logic chips to implement specialized signal-processing "engines." The early systems were relatively slow and consumed a lot of space. TRW shipped the first practical parallel multiplier design in 1973 and added bit-slice ALUs two years later. But at several hundred dollars just for the multiplier chip, the only customers that could afford such a product were research laboratories, medical-scanning equipment makers, and the military.

In 1978, American Microsystems Inc announced the first single-chip IC designed specifically for DSP: the 12-bit S2811. AMI devised a truly innovative circuit design but implemented its chip in a radical "V groove" MOS technology that never yielded volume commercial products.

The following year, Intel Corp introduced the Intel 2920 16-bit "analog signal processor," so called because Intel had designed the chip as a drop-in analog-circuit replacement, complete with on-board A/D and D/A converters. The 2920 processed analog signals digitally, but it lacked a parallel multiplier; what's more, its 600-nsec cycle time made it too slow to perform useful work in the audio spectrum, where the first high-volume DSP chip market would eventually materialize.

The first "true" single-chip DSPs—which market-analysis firm Forward Concepts defines as having parallel MAC (multiplier-accumulator) circuits—emerged in early 1980 from Bell Labs and NEC. The Bell Labs chip, the DSP-1, was a captive device used in AT&T and Western Electric equipment. NEC's µPD7720 was the first true single-chip DSP shipped in volume to the merchant market. Although hampered by primitive development tools, the NEC chip offered sufficient speed—a 122-nsec cycle time with a two-cycle MAC—to perform useful work in the audio spectrum.

In the late 1980s, Hiromitsu Yagi of Ricoh redesigned the original AMI S2811 chip for a conventional NMOS process. Yagi's work resulted in the Ricoh RD28211 and the AMI S28211.

AT A GLANCE

- DSP designers look to optimize what TI calls the "three P's of value": performance, price, and power dissipation.
- ADI designers know the power envelopes for the applications its DSPs target.
- Microchip takes an alternative approach to digital signal processing: the digital signal controller.
- In the future, programmable ASSP devices that offer an alternative to devices such as TI's DaVinci will be the target for FPGAs in certain market segments.

TI GETS IN THE GAME

In 1980, TI's Ed Caudel designed the initial architecture for what would become the company's first digital signal processor. Surendar Magar was hired the same year to optimize the architecture around DSP algorithms. TI introduced the resulting design to the world in February 1982 in the classic International Solid-State Circuits Conference paper, "A Microcomputer with Digital Signal Processing Capability" (**Reference 1**). Caudel announced the final product, the TMS32010, in April 1982 in Paris at the International Conference on Acoustics, Speech, and Signal Processing.

After Speak & Spell launched (**Figure 1**), TI went on to develop DSP devices for a host of industries, but the key to the business, and ultimately to the growth of the market at large, was the ecosystem that emerged around the processors. "TI became the first company with a sophisticated signal-processing chip and also understood that the device [itself] was not the product; the product was the device plus support plus the development environment plus a device hotline," says Frantz, one of the industry's foremost DSP engineers. "We created a product for customers to use in their product."

In the early years, TI's DSP hotline was a great source of design help to customers, especially because in many cases the person who answered the phone was

Figure 1 TI's Speak & Spell team—from left, Gene Frantz, Richard Wiggins, Paul Breedlove, and Larry Brantingham, showing off the product at its introduction—went on to push DSP technology into diverse applications and markets.

the architect of the device in question. "TI had some pretty large customers, and we were getting calls from six or seven different area codes from each of these big customers in different locations," Frantz says. "We realized that we knew more about what each company was doing than they did. We did all we could to help them grow."

There were also calls from many small start-ups asking the same questions, so TI began to see markets forming even before the players themselves picked up on the trends. The company spent the coming years inventing the next generation of signal processors to do the "crazy" things their customers wanted to do, as Frantz puts it.

Along the way, TI remained mindful of the "three P's of value": performance, price, and power dissipation. "Most people did not realize that power dissipation was that important," says Frantz, "but we had been working on low-power device technology since the mid-'60s, when the calculator was invented."

Early on, TI began its third-party program, marshaling small companies with DSP expertise to "fill in the holes" that TI could not address. Frantz describes the program as a "value Web," through which all participants would make money while expanding the available customer-support network.

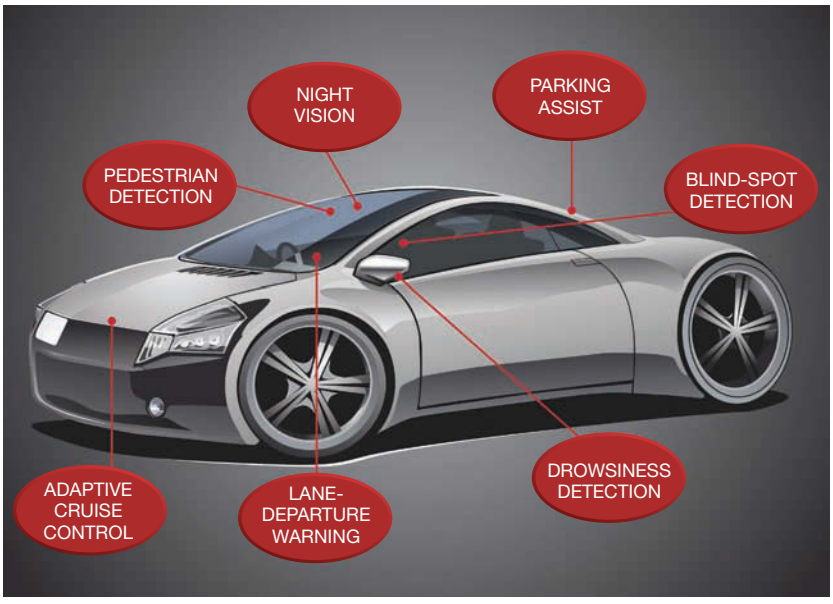


Figure 2 Future embedded automotive analytics will create autonomous vehicles.

Fernando Mujica, director of TI's System Architectures Lab and an expert

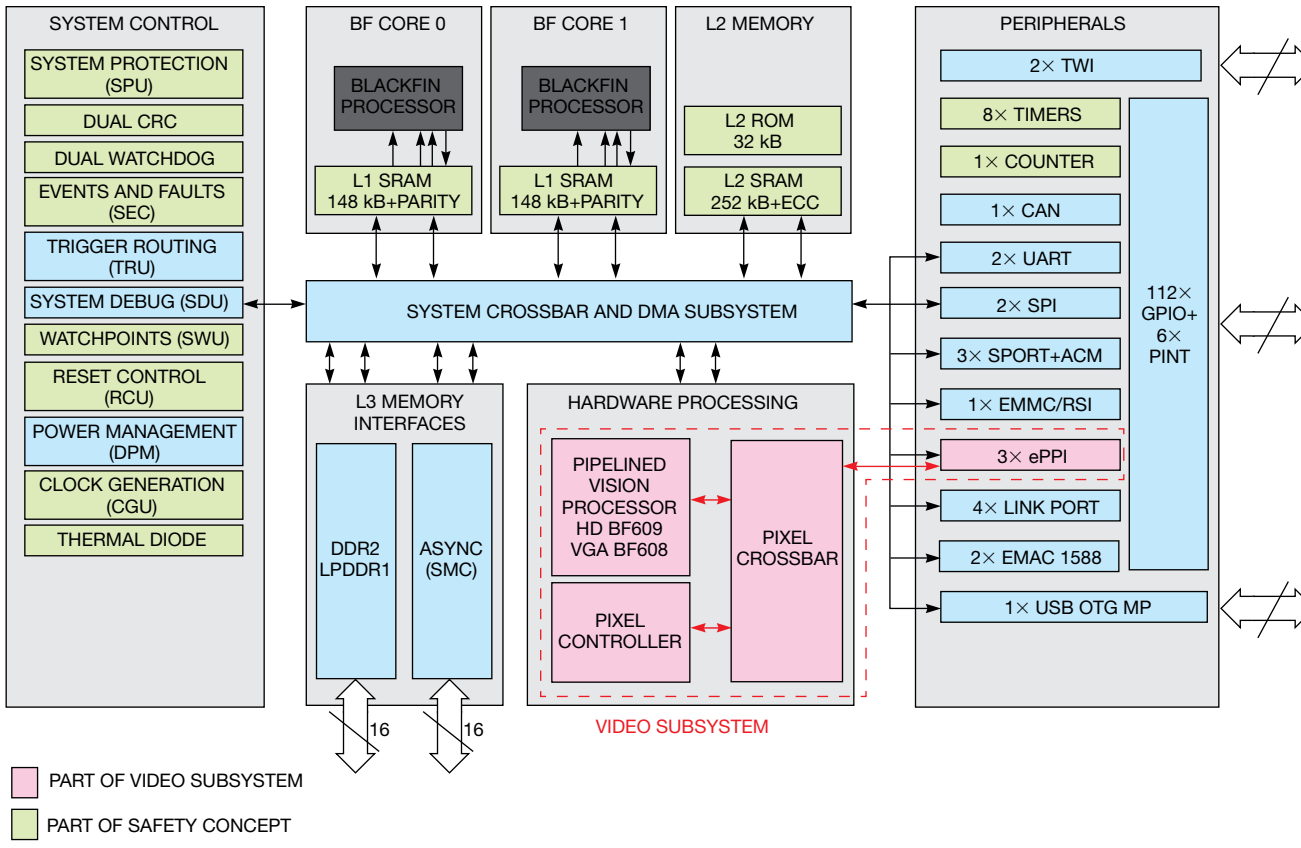


Figure 3 Dynamic power management in devices such as this ADSP-BF609/8 lets developers match processor power consumption to processing requirements during program execution.

in analytical embedded processing, is a member of the generation of engineers to whom DSP pioneers such as Frantz are passing the baton at TI. "Over the last 30 years, virtually every aspect of our lives has been influenced by DSP," Mujica says. "Now, we are seeing the DSP take on embedded analytics tasks, a growing and evolving area demanding the highest degree of programmability. Signal-conditioning and -compression technologies are now implemented as hard-coded accelerators and integrated with DSPs in modern embedded processors."

Current DSPs and other embedded processors tackle tasks that previously required human interaction. A case in point is the expanding range of automotive-safety features, including lane-departure warning and active cruise control, available in high-end vehicles. Such systems go beyond convenience features to warn the driver and even apply the brakes or steer the vehicle in an emergency.

"In the near future, embedded analytics solutions will make autonomous vehicles a reality," Mujica says (**Figure 2**). "Robotics is another area that is about to be revolutionized by the increasing capabilities of embedded processors to take on complex analytics tasks."

To see how digital signal processing is integrated into many of TI's offerings, take a look at the company's high-performance, KeyStone-based multicore processors, single-core processors, and OMAP processors (**references 2, 3,** and **4**).

LOW-POWER INNOVATOR

TI is not the only company to have driven DSP technology on the three P's of value. Analog Devices Inc has consistently improved the power/performance ratios of both its fixed-point Blackfin processors, developed in 2001, and its floating-point Sharc processors, which emerged in the mid-'90s.

Designers are continually challenged to reconcile power-budget requirements with the need for greater processing precision. In response, ADI has focused on the efficient utilization of available power and has turned out progressively more compact designs, ensuring greater system portability, minimal real-estate consumption, and overall lower operating costs, according to Colin Duggan, ADI director of marketing for processors, and Richard Murphy, Blackfin product manager. The pair note that low power draw typically yields low heat dissipation, which can help ensure greater system reliability and minimize the need for both system- and room-level cooling—with associated power, space, and cost savings.

JOIN THE CONVERSATION

To comment on this article, go to www.edn.com/4394792.

For battery-powered devices, low-power processors extend system battery life and time between charges, and help minimize system size and weight to ensure ease of portability. Reductions in processor power consumption also let designers use smaller batteries, maximizing power and space savings.

DPM (dynamic power management) in the just-announced BF60x high-performance family and previous Blackfin generations lets developers match the processor's power consumption to processing requirements during program execution (**Figure 3**). ADI pioneered the application of DPM with the release of the first Blackfin processors in October 2001.

LOW-POWER PROCESSORS EXTEND SYSTEM BATTERY LIFE, AND HELP MINIMIZE SYSTEM SIZE AND WEIGHT.

Other design techniques used in the Blackfin processors include programmable voltage and frequency scaling; clock-cycle-resolution dynamic clock gating; multiple power domains, to support deep-sleep and hibernate modes; high code density, to minimize bus-activation energy; mixed threshold-voltage transistor utilization, for optimal performance and power efficiency; a full-custom processor core, for maximum energy efficiency; judicious use of hardware accelerators; and support for metastable SDRAM, to minimize board-level power consumption.

On the floating-point side, ADI designed the recent Sharc 2147x with low power consumption in mind. The processor's 5-Mbit onboard memory lets designers conserve power that might otherwise be expended moving data across external memory, other processors, or both. The series' integrated memory and parallel-processing features enable performance gains that contribute to net power savings by ensuring that algorithms and programs execute faster.

Side-by-side comparisons, all showing typical power consumption at 25°C, help ADI make its case. In the Sharc family, the ADSP-21261, dissipating 900 mW at 150 MHz and 1.2W at 200 MHz, compares with the more recent ADSP-2147x family, dissipating 180 mW at 150 MHz and 363 mW at 266 MHz. In the Blackfin family, the BF527 draws 205 mW of core power at 600 MHz, with standby power in the neighborhood of 10 mW and hibernate-mode power dissipation of approximately 40 µA; the more recent BF592 offers active power draw of 88 mW at 300 MHz, standby power of less than 1 mW, and hibernate-mode power dissipation at 20 µA. The company's highest performance Blackfin BF609, with two 500-MHz cores, draws 400 mW at 1 GHz.

Duggan and Murphy note that ADI's power-down features provide flexible user control and that newer process geometries are more efficient in power. They add that the company's designers know the power envelopes for the applications its DSPs will need to meet.

ADI's goal is to enable the highest performance possible within a specific power envelope for the application. User-programmable PLLs, peripherals that can turn down their own system clocks, and the ability to turn off any clock domain in the absence of certain peripherals all save power. Other power-saving approaches include using efficient busing architectures, maximizing the percentage of transistors in the design that are high-threshold-voltage transistors (93% is typical), and using the PVP (Pipeline Vision Processor) as an accelerator.

MICROCHIP DSCs

Microchip Technology Inc takes an alternative approach to digital signal processing: the DSC (digital signal controller). The first step was to pair an 8-bit microcontroller with a DSP. Microchip engineers then integrated a DSP core with a PIC microcontroller to yield the 16-bit dsPIC in 2002 (**Reference 5**).

The scalable dsPIC solution offers patented microcontroller-like interrupt handling for real-time control, which otherwise is challenging to perform with a DSP, according to Microchip (**Figure 4**). The DSC core has a modified Harvard bus architecture, with a 16-bit-wide data path and 24-bit-wide instruction path; extensive addressing modes; a 16×16-bit general-purpose register set; a flexible software stack; single-cycle 16×16 multiply functionality; DMAC (direct memory-access control) with dual-port SRAM; and eight channels for peripherals.

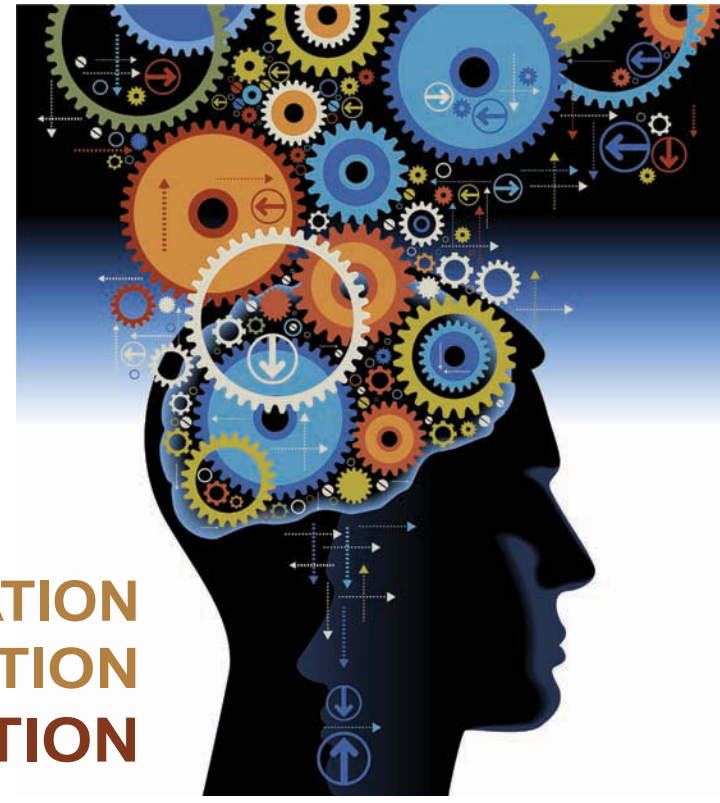
The DSCs run at speeds from 30 to 70 MIPS and serve markets such as digital power, lighting, motor control, speech, biometrics, sensor processing, and simple filters. The chips contain DACs for speech processing, motor-control PWMs, fast ADCs, and specialized ADCs for SMPS (switched-mode power supply) applications. Microchip says the parts lever-

ecia
Electronic Components Industry Association

2012 Executive Conference

October 28 - 30

InterContinental Chicago O'Hare Hotel



INFORMATION + APPLICATION = INNOVATION

a powerful formula for business growth and success

Identifying the right information for your business is crucial. The 2012 Executive Conference delivers on its legacy as the industry's premiere educational and networking conference.

Rick Hamada, Avnet - Frank Lange, Menlo Worldwide Logistics
Glenn Bassett, IHS - Gordon Hunter, Littelfuse - Guy Blissett, IBM
Frank Cutitta, The Center for Global Branding - Terry Jones, Kayak.com
Jim Forbes, Pricewaterhouse Coopers - Jon Dudas, *FIRST*

Conference Sponsors:

Honeywell, element14, ON, VISHAY, Advantage, BOURNS, Kruvand, molex, Model N, CDE Cornell Dubilier, DOVE Electronic Components, muRata, NORRIS & Associates, Penton, OneBeacon Technology Insurance, SHARP Microelectronics of the Americas, UBM Electronics, Digi-Key, IHS, NetCOMPONENTS, TE connectivity, Assurance, KEMET, PHOENIX CONTACT Inspiring Innovations, SOURCING, CARLTON-BATES, 75 Years MARSH Electronics, Inc., OMRON Electronic Components, Texas Instruments, HEARST business media, Littelfuse

Visit www. eciaonline.org or scan ⇨ for complete program & registration details.

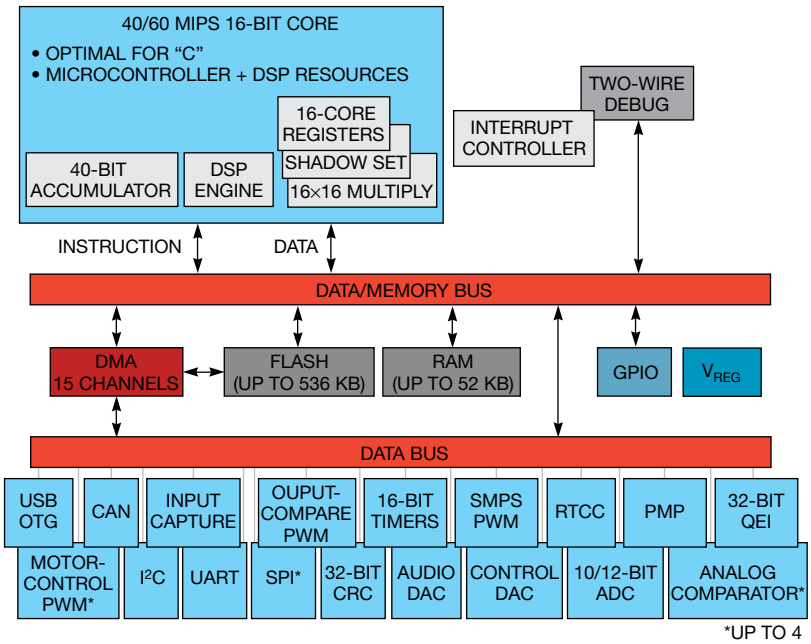


Figure 4 The scalable dsPIC solution offers patented microcontroller-like interrupt handling for real-time control, which otherwise is challenging to perform with a DSP.

age high op-amp integration and offer the "look and feel" of microcontrollers; designers do not have to learn DSP design or software to use them.

Microchip touts seamless migration from the dsPIC to the PIC24 microcontroller; the two are code- and pin-compatible. The same free MPLAB X integrated development environment is used for Microchip's 8-, 16-, and 32-bit microcontrollers and its DSCs. The company says its strategy is to offer engineers simple solutions so that developers of applications such as digital power will be comfortable using the analog-friendly, highly integrated dsPICs.

ENTER FPGAs

The transition to FPGA-based DSP hardware from conventional DSPs can involve a new set of design skills and a new understanding of hardware. For developers new to FPGAs or DSP, the shift can be a significant undertaking that adds risk to design schedules. A Xilinx white paper by senior manager Tom Hill, "Xilinx DSP design platforms: Simplifying the adoption of FPGAs for DSP" (**Reference 6**), shows how Xilinx's DSP development kits are designed to ease FPGA adoption and let algorithm and hardware developers ramp up quickly when developing DSP applications on Xilinx devices.

In the 1990s, according to Hill, Xilinx designed the 4000 series FPGAs for DSP processing. Customers soon found they could build digital filters with FPGAs. Circa 1999, Bruce Newgard, at the time a field applications engineer at Xilinx, saw a great opportunity for the company, but management needed a bit of convincing before signing off on the formation of a DSP division within Xilinx.

By 2005, Xilinx had forged a DSP strategy that involved collaboration with TI and MathWorks to bring out FPGA/DSP coprocessing platforms and tightly integrated tool flows for algorithmic development and design implementation. The same year, Forward Concepts estimated that $2 billion of the high-performance DSP market could be addressed by the performance and flexibility of FPGA-based DSP solutions. Xilinx initially targeted high-growth digital communications,

DSP DATA SHEETS

For a collection of data sheets on the latest DSPs and other processors, go to www.datasheets.com.

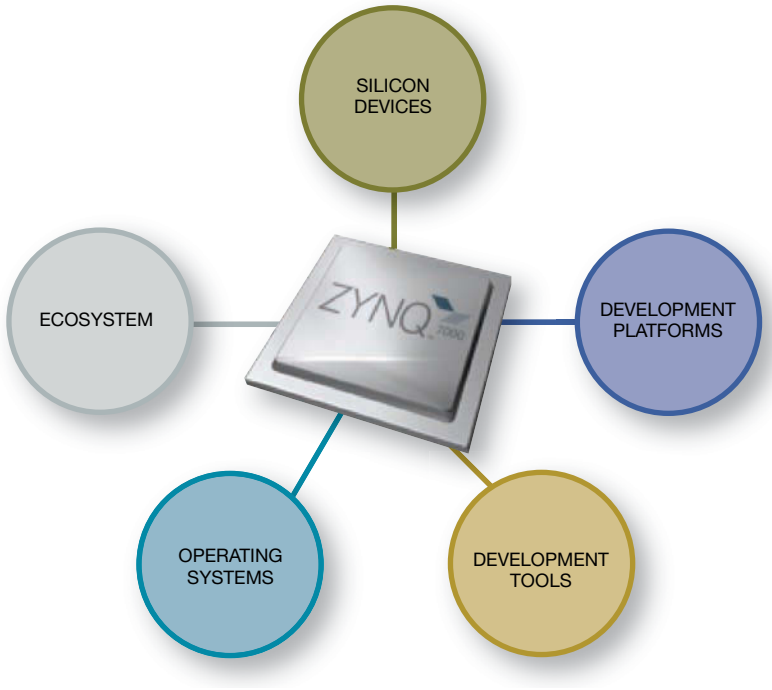


Figure 5 The Zynq-7000 family from Xilinx includes hardware and software development tools, operating systems, and other elements.

MVI (multimedia, video, and imaging), and defense systems. Combined, those areas account for more than 80% of the high-performance DSP market.

Xilinx teamed with MathWorks to develop System Generator, the industry's first DSP plug-in for Xilinx FPGAs. Today, System Generator for DSP is a leading high-level tool for designing high-performance DSP systems using FPGAs.

With System Generator, according to Xilinx, developers with little FPGA design experience can quickly create production-quality FPGA implementations of DSP algorithms in a fraction of traditional RTL development times. The tool provides system modeling and automatic code generation from MathWorks' Simulink and integrates the RTL, embedded, IP, Matlab, and hardware components of a DSP system. System Generator for DSP is a key component of the Xilinx DSP Targeted Design Platform.

Xilinx changed its business model from horizontally based FPGA supplier to vertical applications enabler and now operates specific market-segment groups. The next phase is algorithm-oriented platforms comprising tools, IP, silicon, and kits.

Xilinx FPGA-based DSP platforms now interface with real-world signals and have interfaces to high-speed data converters. Data is sampled at very high rates and then downconverted to simplify DSP hardware implementations. Hill notes that FPGAs had often been used in systems to handle interfaces and downconversion, but 40% of the time they were used with a DSP device.

Doubts about the technique's ease of use and questions about the design flow have been stumbling blocks to adoption of FPGA-based DSP, so in January 2011, Xilinx bought AutoESL. The pairing yielded Xilinx AutoESL 2012.1, which made it easier for designers to get up to speed when implementing DSP systems with FPGAs and provided a smooth transition to the next generation of AutoESL technology: Vivado High-Level Synthesis 2012.2 (**Reference 7**). With the introduction of the Vivado Design Suite, Vivado High-Level Synthesis accelerates design implementation by letting developers target C, C++, and System C specifications directly into FPGAs without manually creating RTL.

Today, Hill notes, if you can do the design with a DSP, a customer will use a DSP; if the design calls for two or three DSPs, then FPGAs compete well. For heavy-duty filtering, FPGAs win. FPGAs perform up/downconversion and digital predistortion in wireless and radar and sonar countermeasures for the military.

LIKE THIS?

For more articles like this one, go to www.edn.com/design/systems-design.

Medical imaging is another key area, with some CT scanning and ultrasound equipment having 256 or more sensors.

In March, Xilinx launched the Zynq-7000, touting "all programmable" SOC integration in a device that offers ASIC-like performance and power consumption, the flexibility of an FPGA, and the ease of programming of a microprocessor (**Figure 5**). The Zynq-7000 ecosystem includes hardware and software development tools and operating systems.

In the future, Hill predicts, FPGAs will be the foundation for programmable ASSPs that offer an alternative to devices such as TI's DaVinci digital media processors in select market segments.

The history of DSP could not be written without acknowledging the tool vendors that support DSP algorithm and architecture development. To read about the role of companies such as MathWorks and Synopsys Inc in the technology's evolution, and to get a DSP analyst's take on the industry's past, present, and future, see the full article online at www.edn.com/4394792.EDN

REFERENCES

1 Magar, Surendar, et al., "A microcomputer with digital signal processing capability," International Solid-State Circuits Conference, 1982, http://bit.ly/TZdN5O.
2 KeyStone-based multicore processors, Texas Instruments, http://www.ti.com/multicore.
3 C6000 high-performance DSPs, Texas Instruments, http://www.ti.com/c6000.
4 OMAP mobile processors, Texas Instruments, http://www.ti.com/omap.
5 16-bit PIC24 MCUs and dsPIC DSCs, Microchip, http://bit.ly/T6iWXv.
6 Hill, Tom, "Xilinx DSP design platforms: Simplifying the adoption of FPGAs for DSP," white paper, Dec 8, 2009, http://bit.ly/PGEB8n.
7 Vivado High Level Synthesis, Xilinx, http://bit.ly/OAM4q6.

You can reach Senior Technical Editor Steve Taranovich at 1-631-413-1834 and steve.taranovich@ubm.com.

Power your most demanding setups with ease.

No matter your application, accelerate with Agilent.

Whether it's automotive ECU, military communications, base station power amplifiers or general purpose test, maximize manufacturing throughput and R&D productivity. With seven new high-power modules from 300 to 500 W, Agilent helps you execute a wide range of high-power setups with the performance to measure milliamps accurately, too.

Agilent N6700 Modular Power System

- 4 mainframes–manufacturing or R&D
- 34 modules from 20 to 500 W
- 4 performance levels–basic to precision

To view application videos scan QR code

or visit http://goo.gl/sgwbK

Get a FREE 8 GB USB drive loaded with power product resources*
www.agilent.com/find/N6700Power

 *While supplies last. Terms and conditions apply.

u.s. 1-800-829-4444 canada: 1-877-894-4414

Anticipate Accelerate Achieve

Agilent Technologies

BY HENRY J ZHANG • LINEAR TECHNOLOGY CORP

PCB-layout considerations for nonisolated switching power supplies

A GOOD LAYOUT DESIGN OPTIMIZES EFFICIENCY, ALLEVIATES THERMAL STRESS, AND MINIMIZES THE NOISE AND INTERACTIONS AMONG TRACES AND COMPONENTS. IT ALL STARTS WITH THE DESIGNER'S UNDERSTANDING OF THE CURRENT-CONDUCTION PATHS AND SIGNAL FLOWS IN THE SUPPLY.

The best news when you power up a prototype supply board for the very first time is that it not only works, but also runs quiet and cool. Unfortunately, that is not always the case.

A common problem with switching power supplies is "unstable" switching waveforms. Sometimes, waveform jitter is so pronounced that the magnetic components generate audible noise. If the problem is related to the printed-circuit-board layout, identifying the cause can be difficult. That is why proper PCB layout at the early stage of a switching-power-supply design is critical.

The power-supply designer best understands the technical details and functional requirements of the supply in the final product. Thus, from the outset of the board-design project, the power-supply designer should work closely with the PCB layout designer on the critical supply layout.

A good layout design optimizes supply efficiency and alleviates thermal stress; most important, it minimizes the noise and interactions among traces and components. To achieve those goals, the designer must understand the current-conduction paths and signal flows in the switching power supply. Keep the following design considerations in mind to achieve a proper layout design for nonisolated switching power supplies.

THE LAYOUT PLAN

To achieve the best voltage regulation, load transient response, and system efficiency for an embedded dc/dc supply on a large board, locate the supply output near the load devices to minimize the interconnection impedance and the conduction voltage drop across the PCB traces. Ensure good airflow to limit the thermal stress; if forced-air cooling is available, locate the supply close to the cooling fan.

In addition, the large passive components, such as inductors and electrolytic capacitors, should not block the airflow to low-profile, surface-mount semiconductor components such as power MOSFETs or PWM controllers. To prevent the switching noise from upsetting other analog signals in the system, avoid routing sensitive signal traces underneath the supply if possible; otherwise, you will need an internal ground plane between the power-supply layer and the small-signal layer for shielding.

It's important to plan out your power-supply location and board real-estate requirements during the system's early design and planning phase. Designers sometimes ignore that advice and focus first on more "important" or "exciting" circuits on the big system board. Treating power management as an afterthought and relegating the supply to whatever space is left on the board are contrary to achieving an efficient and reliable power-supply design.

For multilayer boards, it is highly desirable to place the dc ground or dc input- or output-voltage layers between the high-current, power-component layer and the sensitive, small-signal trace layer. The ground or dc voltage layers provide ac grounds to shield the small-signal traces from noisy power traces and power components.

As a general rule, the ground or dc voltage planes of a multilayer PCB should not be segmented. If you find that such segmentation is unavoidable, minimize the number and

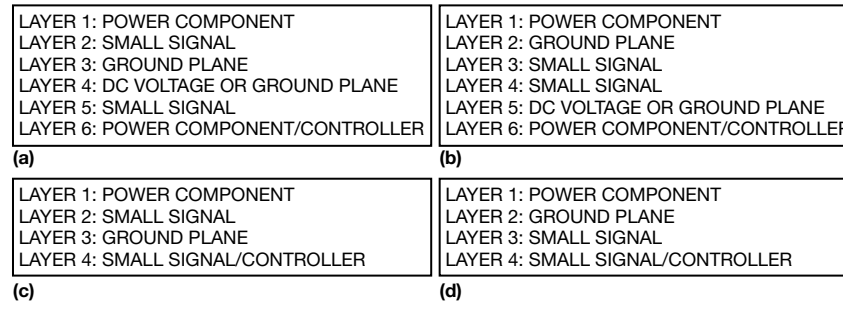


Figure 1 Undesirable layer arrangements for six- (a) and four-layer (c) switching-power-supply PCBs sandwich the small-signal layer between the high-current power layer and the ground layer. In desirable arrangements for six- (b) and four-layer (d) designs, the ground layers shield the small-signal layers.

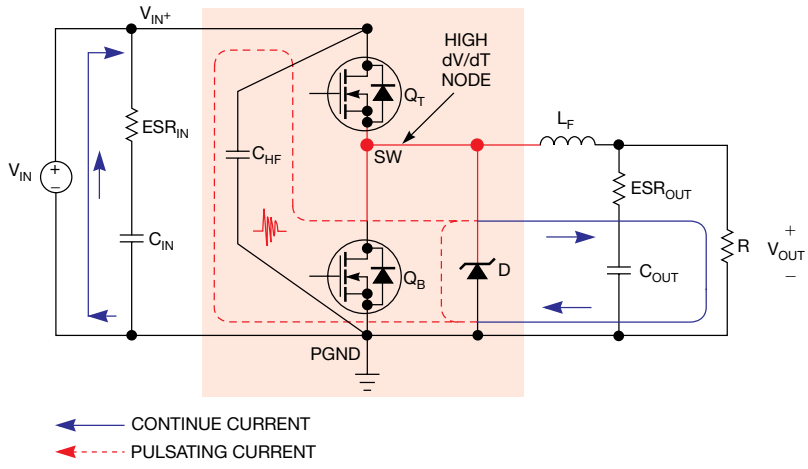


Figure 2 The solid line represents the continuous-current paths in a synchronous buck converter; the dashed line represents the pulsating (switching)-current paths.

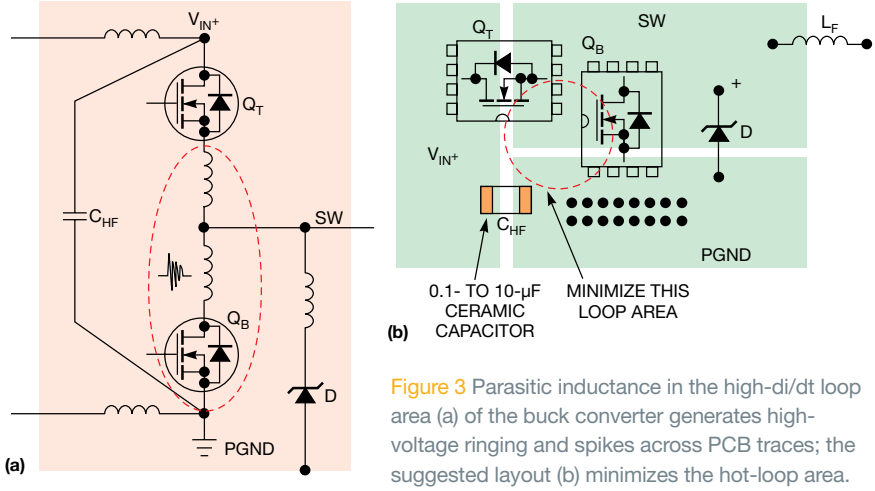


Figure 3 Parasitic inductance in the high-di/dt loop area (a) of the buck converter generates high-voltage ringing and spikes across PCB traces; the suggested layout (b) minimizes the hot-loop area.

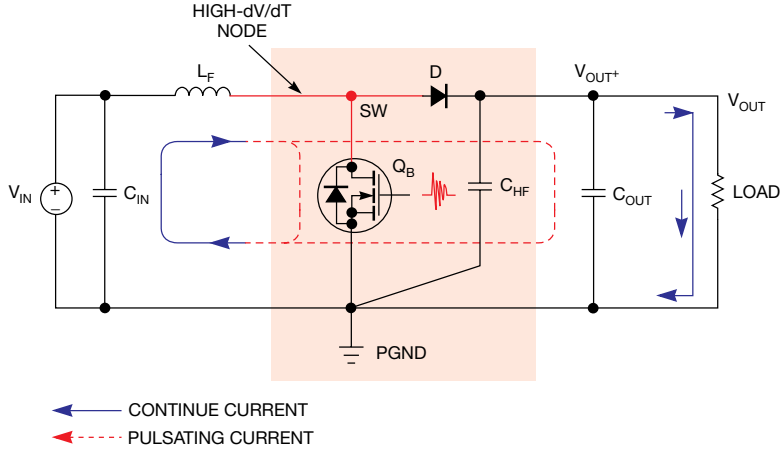


Figure 4 The continuous- and pulsating-current paths in the boost converter are shown. The high-frequency ceramic capacitor, C_{HF}, should be placed on the output side close to the MOSFET, Q_B, and boost diode, D.

length of traces in those planes, and route the traces in the same direction as the high-current-flow direction to minimize the impact.

Figures 1a and **1c** illustrate undesirable layer arrangements for six- and four-layer switching-power-supply PCBs, respectively. The configurations sandwich the small-signal layer between the high-current power layer and the ground layer, thereby increasing capacitive-noise coupling between the high-current/voltage power layer and the analog small-signal layer.

In **figures 1b** and **1d**, respectively illustrating desirable layer arrangements for minimizing noise coupling in six- and four-layer PCB designs, the ground layers shield the small-signal layers. It is important always to have a ground layer next to the outside power-stage layer, and it is desirable to use thick copper for the external high-current power layers to minimize PCB conduction loss and thermal impedance.

POWER-STAGE LAYOUT

A switching-power-supply circuit can be divided into the power-stage circuit and the small-signal control circuit. The power-stage circuit includes the components that conduct high current; in general, you would place those components first and then place the small-signal control circuitry in specific spots in the layout.

The large current traces should be short and wide to minimize PCB inductance, resistance, and voltage drop. This setup is especially critical for the traces with high-di/dt pulsating-current flow.

Figure 2 identifies the continuous- and pulsating-current paths in a synchronous buck converter; the solid line represents the continuous-current paths, and the dashed line represents the pulsating (switching)-current paths. The pulsating-current paths include the traces connected to the input decoupling ceramic capacitor, C_{HF}; the top control FET, Q_T; and the bottom synchronous FET, Q_B, with its optional, paralleled Schottky diode.

Figure 3a shows the parasitic PCB inductors in the high-di/dt current paths. Because of the parasitic inductance, the pulsating-current paths not only radiate magnetic fields but also generate high-voltage ringing and

spikes across the PCB traces and MOSFETs. To minimize PCB inductance, lay out the pulsating-current loop (hot loop) so that it has a minimum circumference and comprises traces that are short and wide.

The high-frequency decoupling capacitor, C_{HF}, should be a 0.1- to 10-µF, X5R- or X7R-dielectric ceramic capacitor with very low ESL (effective series inductance) and ESR (equivalent series resistance). Higher-capacitance dielectrics (such as Y5V) can allow a large reduction in capacitance over voltage and temperature and thus are not preferred materials for C_{HF} use.

HIGHER-CAPACITANCE DIELECTRICS CAN ALLOW A LARGE REDUCTION IN CAPACITANCE OVER VOLTAGE AND TEMPERATURE AND THUS ARE NOT PREFERRED MATERIALS FOR C_{HF} USE.

Figure 3b provides a layout example for the critical pulsating-current loop in the buck converter. To limit resistive voltage drops and the number of vias, place power components on the same side of the board, with power traces routed on the same layer. When it is necessary to route a power trace to another layer, choose a trace in the continuous-current paths. When using vias to connect PCB layers in the high-current loop, deploy multiple vias to minimize via impedance.

Figure 4 shows the continuous- and pulsating-current loops in the boost converter. In this case, you should place the high-frequency ceramic capacitor, C_{HF}, on the output side close to the MOSFET, Q_B, and boost diode, D.

Figure 5 provides a layout example for the pulsating-current loop in the boost converter. It is critical to minimize the loop formed by the switch, Q_B, rectifier diode, D, and high-frequency output capacitor, C_{HF}.

To emphasize the importance of the decoupling capacitor, **figures 6** and **7** provide an example of a synchronous buck circuit. **Figure 6a** shows the layout of a dual-phase, $12V_{IN}$ to $2.5V_{OUT}$/30A max, synchronous buck supply using the LTC3729 two-phase, single-V_{OUT} controller IC. The waveforms for switching nodes SW1 and SW2 and output inductor current I_{LF1} are stable at no load (**Figure 6b**). If the load current exceeds 13A, however, the SW1 node waveform starts missing cycles. The problem becomes even worse with higher load current (**Figure 6c**).

Adding two 1-µF high-frequency ceramic capacitors—one on each channel's input side—solves the problem by separating and minimizing the hot-loop area of each channel. The switching waveform is stable even with maximum load current up to 30A.

HIGH-DV/DT SWITCHING AREA

In **figures 2** and **4**, the SW voltage swings with a high dv/dt rate between V_{IN} (or V_{OUT}) and ground. This node is rich in high-frequency noise components and is a strong source of EMI noise. To minimize the coupling capacitance between

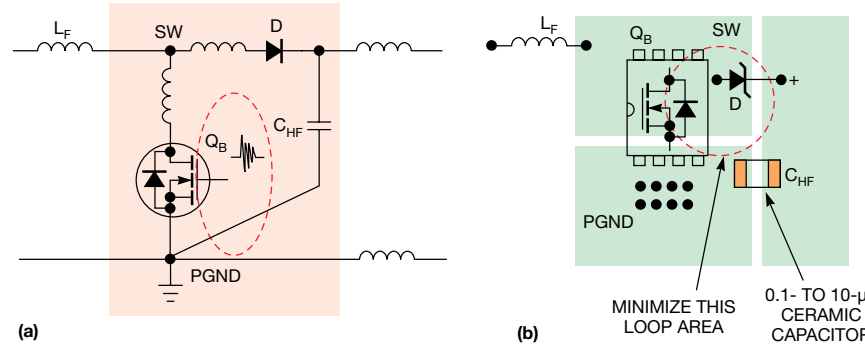
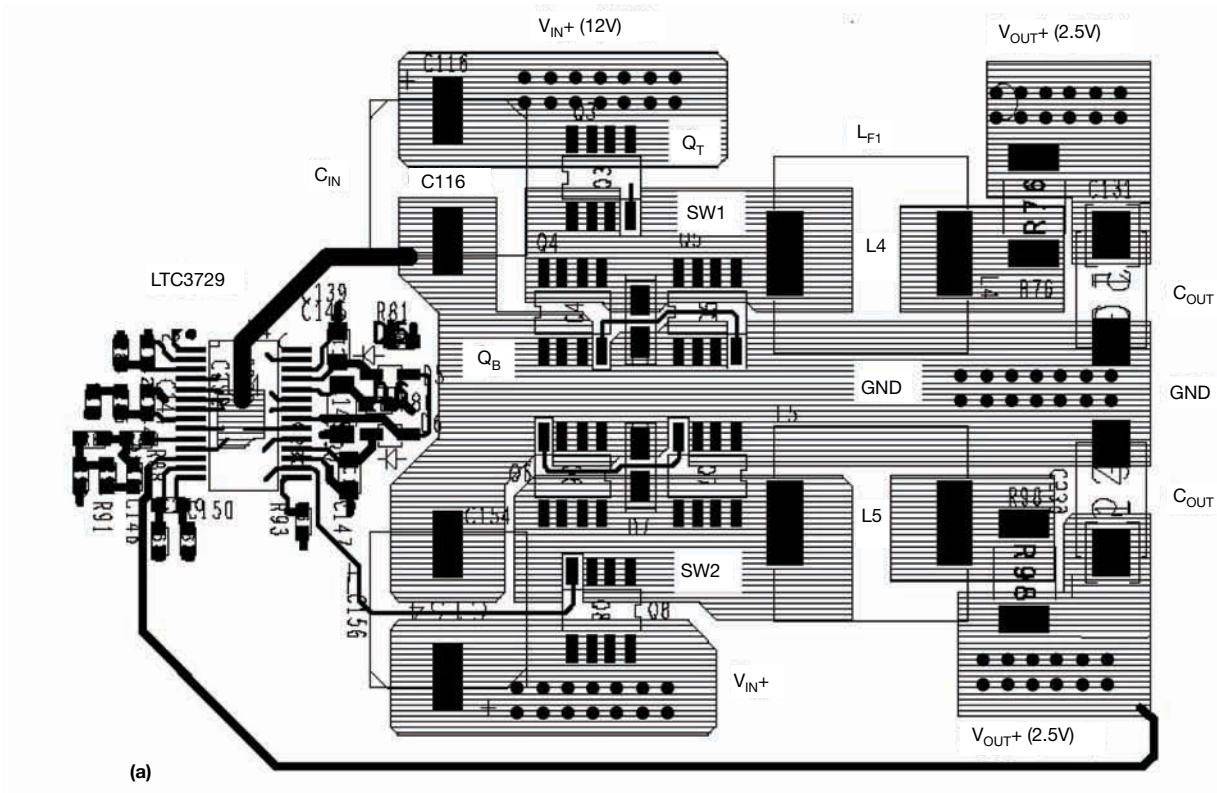
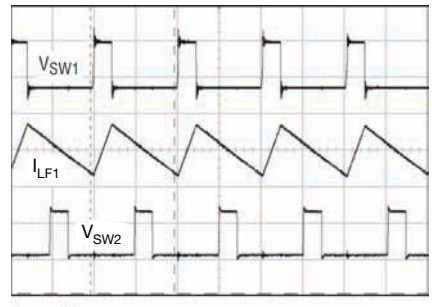


Figure 5 The hot-loop and parasitic PCB inductors in the boost converter are shown (a); the suggested layout (b) minimizes the hot-loop area.





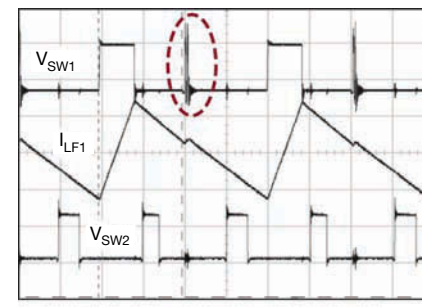
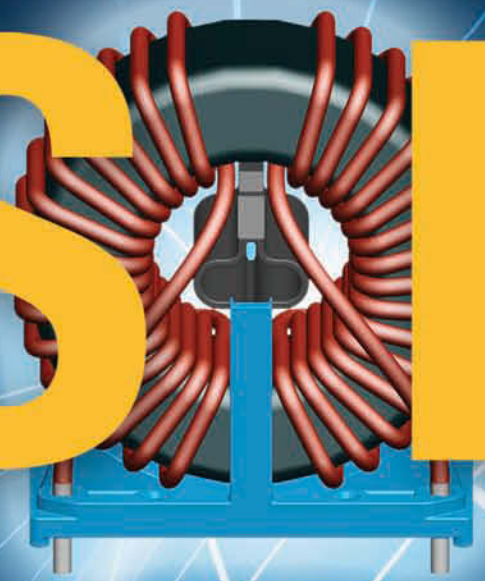


Figure 6 This two-phase, 2.5V/30A output buck converter (a) has a noise problem: Switching waveforms are stable at no load (b), but the SW1 waveform misses cycles when load current exceeds 13A (c).

TDK

The choice for SOLAR



Get something extra for your solar inverter: a perfect fit! Our broad line of EPCOS power line chokes and our ability to modify means you get the right choke for your design. EPCOS brand power line chokes cover inductance values from 0.2 to 100 mH and offer high current capability – up to 54 A with double power line chokes and up to 62 A with triple power line chokes!

We offer chokes for up to 1000 V and with resistance between 1.5 and 2800 mΩ. Rated voltage is 250 V AC for double and 690 V AC for triple variants. Designed for temperatures of 40 to 85 °C, they are available in vertical or horizontal versions.

Call 1-888-768-2673 or visit www.epcos.com/inductors

www.epcos.com

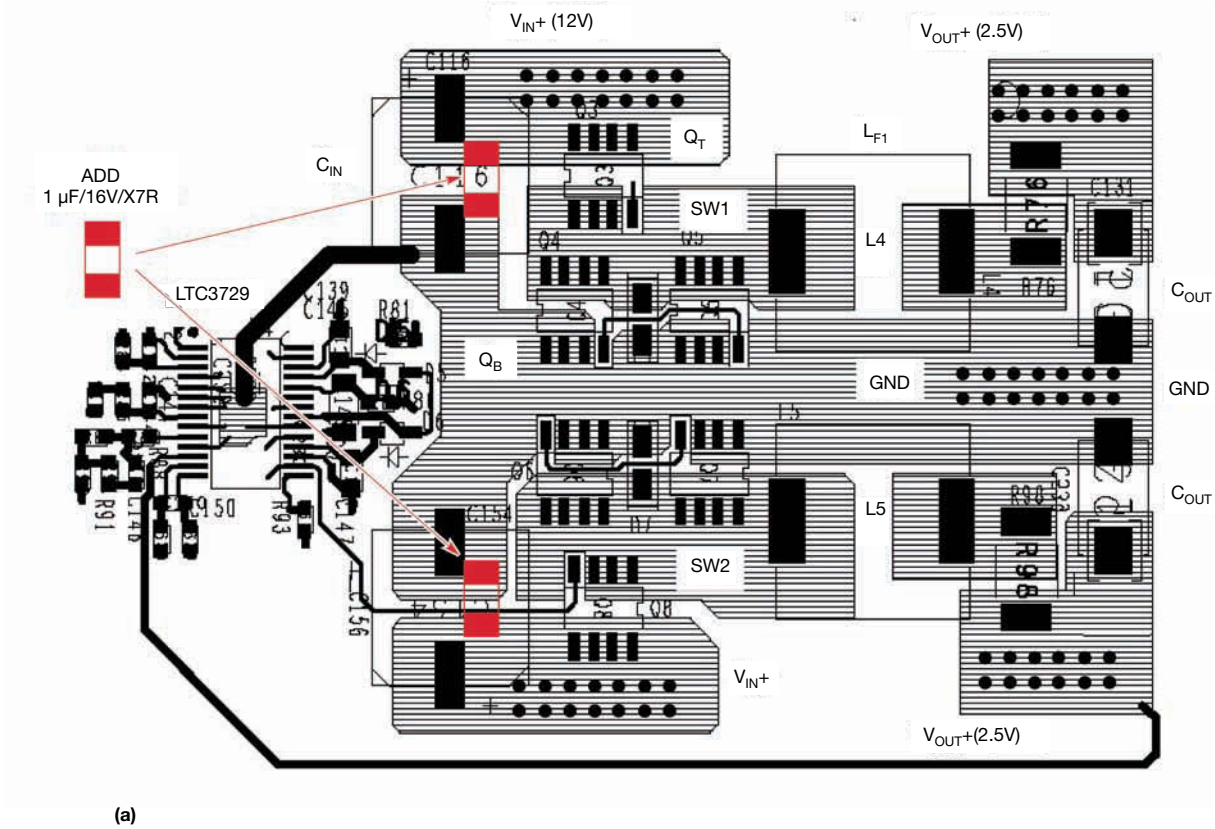


Figure 7 Adding two 1-µF, high-frequency input capacitors (a) solves the noise problem, as the switching waveforms at zero load (b) and 30A load (c) show.

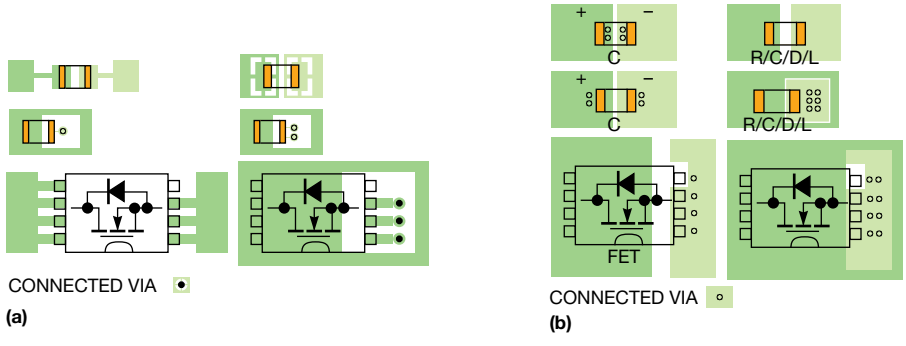
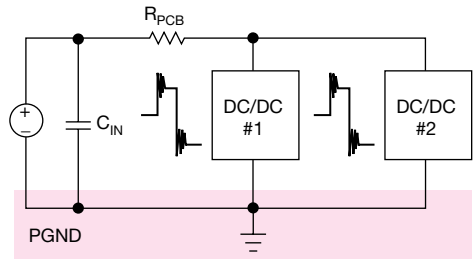
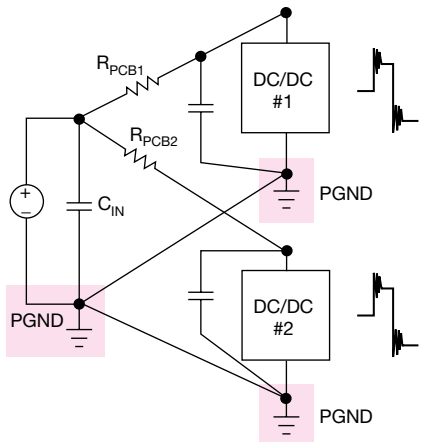


Figure 8 Unnecessary use of thermal-relief land patterns (a) increases the interconnection impedance of power components; in the recommended land pattern (b), the positive and negative vias are kept as close to each other as possible to minimize ESL.



(a)



(b)

Figure 9 When multiple onboard switching supplies share the same input-voltage rail (a), separate the input-current paths among the supplies for a more desirable setup (b).

the switching node and other noise-sensitive traces, you would minimize the SW copper; however, to conduct high inductor current and provide a heat sink to the power MOSFET, the SW-node PCB area cannot be made too small. It is usually preferable to place a ground copper area underneath the switching node to provide additional shielding.

In a design without external heat sinks for surface-mounted power MOSFETs and inductors, the copper area must be sufficient for heat sinking. For a dc voltage node, such as input/output voltage and power ground, it is desirable to make the copper area as large as possible.

Multiple vias are helpful in further reducing thermal stress. For high-dv/dt switching nodes, determining the proper size for the switching-node copper area involves a design trade-off between minimizing dv/dt-related noise and

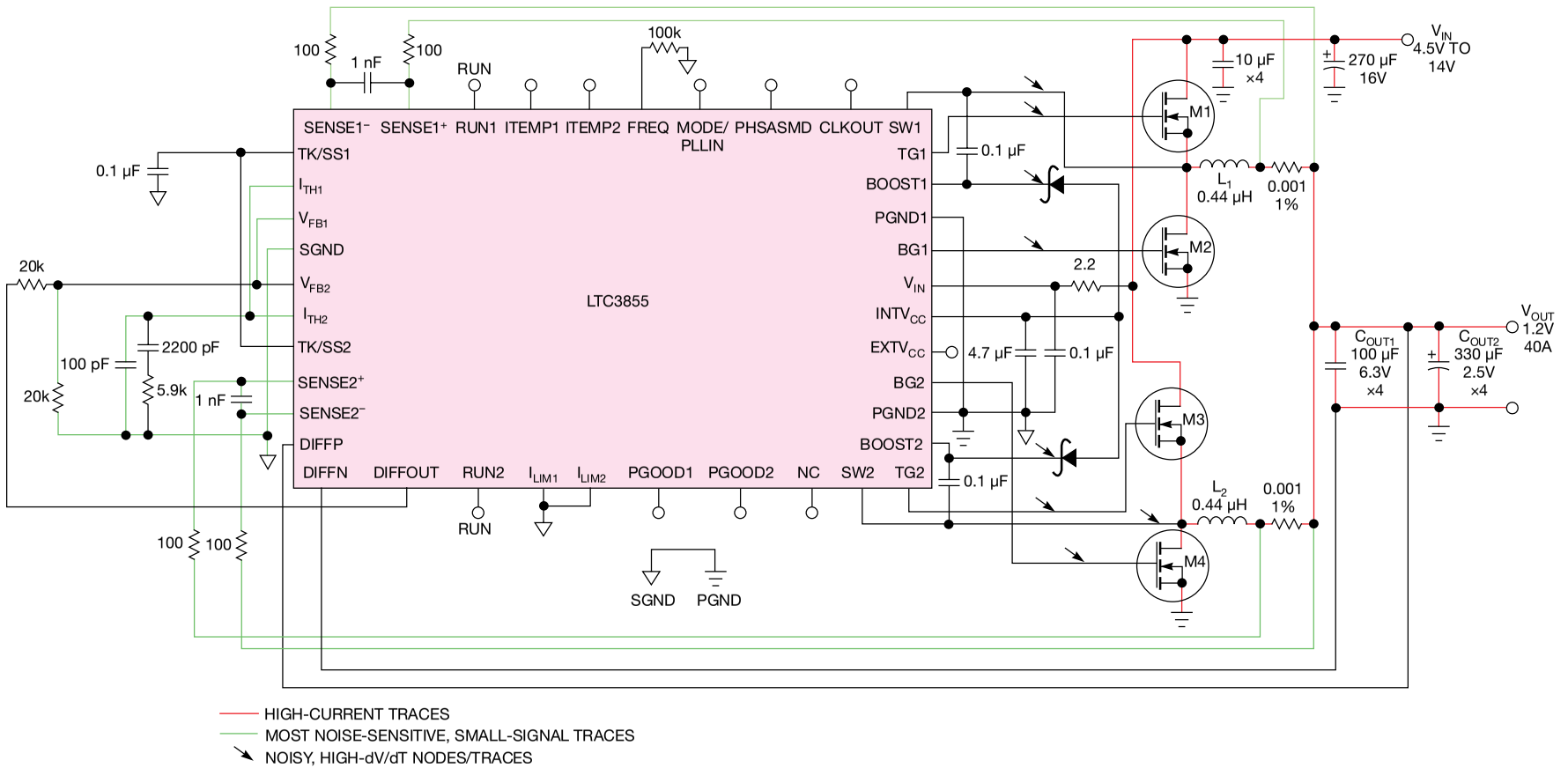


Figure 10 Using different colors in the schematic to indicate the different types of traces, as was done here for the LTC3855 buck converter, will help the PCB designer distinguish among them.

providing good heat-sinking capability for the MOSFETs.

POWER LAND PATTERNS

It is important to pay attention to the land (or pad) pattern of power components, such as low-ESR capacitors, MOSFETs, diodes, and inductors. **Figures 8a** and **8b** show examples of undesirable and desirable power-component land patterns, respectively.

For a decoupling capacitor, the positive and negative vias should be as close to each other as possible to minimize PCB ESL (**Figure 8b**). This is especially effective for capacitors with low ESL. Large-valued, low-ESR capacitors are usually more expensive; improper land patterning and poor routing can degrade their performance and thus increase overall cost. In general, the desired land patterns reduce PCB noise, reduce thermal impedance, and minimize trace impedance and voltage drops for the high-current components.

One common mistake in high-current power-component layout is the improper use of thermal-relief land patterns, as **Figure 8a** shows. Unnecessary use of thermal-relief land patterns increases the interconnection impedance of power components, resulting in higher power losses and decreasing the decoupling effect of low-ESR capacitors. If you use vias to conduct high current in your layout, be sure to use them in sufficient numbers to minimize via impedance. Further, do not use thermal relief for those vias.

Figure 9 shows an application with several onboard switching supplies sharing the same input-voltage rail. When those supplies are not synchronized to each other, it is necessary to separate the input current traces to avoid common-impedance noise coupling between different power supplies. It is less critical to have a local input-decoupling capacitor for each power supply.

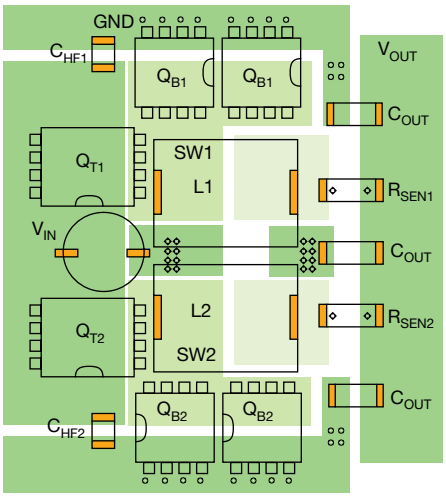


Figure 11 In this power-stage layout of a dual-phase, single-V_{OUT} buck converter, a solid power-ground-plane layer is placed just underneath the power-component layer.

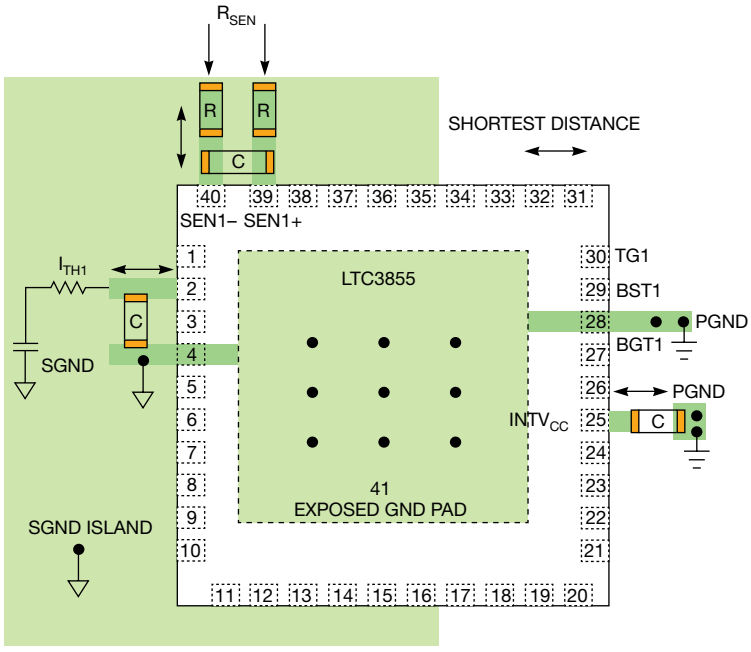


Figure 12 In the preferred ground-separation scheme for the LTC3855 supply, the IC has an exposed GND pad, which should be soldered down to the PCB to minimize electrical and thermal impedance. Several critical decoupling capacitors should be next to the IC pins.

components with ground planes or traces.

The control circuitry should have a separate signal (analog)-ground island from the power-stage ground. If there are separate SGND (signal ground) and PGND (power ground) pins on the controller IC, you should route them separately. For controller ICs that have integrated MOSFET drivers, the small-signal section of the IC pins should use the SGND (**Figure 12**).

Only one connection point is required between the signal and power grounds. It is desirable to return the signal ground to a clean point of the power-ground plane. Connecting both ground traces just under the controller IC can accomplish the two grounds. **Figure 12** shows the preferred ground separation of the LTC3855 supply. In this example, the IC has an exposed ground pad. It should be soldered down to the PCB to minimize electrical and thermal impedance. Multiple vias should be placed on the ground-pad area.

The decoupling capacitors for the controller IC should be physically close to their pins. To minimize connection impedance, it is preferable to connect the decoupling capacitors directly to the pins without using vias. As shown in **Figure 12**, the LTC3855 pins that should have their decoupling capacitors closely located are the current-sensing pins, $Sense^+/Sense^-$; compensation pin, I_{TH}; signal-ground pin, SGND; feedback-voltage divider pin, FB; IC V_{CC} voltage pin, $INTV_{CC}$; and power-ground pin, PGND.

For a PolyPhase single-output converter, having a symmetric layout for each phase helps to balance thermal stresses.

LAYOUT DESIGN EXAMPLE

Figure 10 provides a design example of a 4.5V to 14V_{IN} to 1.2V/40A max dual-phase synchronous buck converter using the LTC3855 PolyPhase current-mode step-down controller. Before starting your PCB layout, one good practice is to use different colors in the schematic to highlight the high-current traces; the noisy, high-dv/dt traces; and the sensitive, small-signal traces. Such delineation will help PCB designers distinguish among the traces.

Figure 11 shows a power-stage layout example for the power-component layer of this 1.2V/40A supply. In this figure, Q_T is the top-side control MOSFET and Q_B the bottom-side synchronous FET. An optional Q_B footprint is added for even more output current. A solid power-ground-plane layer is placed just underneath the power-component layer.

CONTROL-CIRCUITRY LAYOUT

Keep the control circuitry away from the noisy, switching copper areas. It is preferable to locate the control circuitry close to the V_{OUT}+ side for the buck converter and close to the V_{IN}+ side for the boost converter, where the power traces carry continuous current.

If space allows, locate the control IC a small distance (0.5 to 1 in.) from the power MOSFETs and inductors, which are noisy and hot. If space constraints force you to locate the controller close to power MOSFETs and inductors, take special care to isolate the control circuitry from the power

LOOP AREA AND CROSSTALK

Two or more adjacent conductors can be coupled capacitively. High dv/dt on one conductor will couple currents to another through the parasitic capacitor. To reduce the noise coupling from the power stage to the control circuitry, keep the noisy switching traces far from the sensitive small-signal traces. If possible, route the noisy traces and sensitive traces on different layers, using an internal ground layer for noise shielding.

IF SPACE ALLOWS, LOCATE THE CONTROL IC A SMALL DISTANCE (0.5 TO 1 IN.) FROM THE POWER MOSFETS AND INDUCTORS, WHICH ARE NOISY AND HOT.

The FET-driver TG, BG, SW, and BOOST pins on the LTC3855 controller have high-dv/dt switching voltages. The LTC3855 pins connected to the most sensitive small-signal nodes are $Sense^+/Sense^-$, FB, I_{TH}, and SGND. If the layout routes sensitive signal traces close to high-dv/dt nodes, you must insert ground traces or a ground layer between the signal traces and high-dv/dt traces to shield the noise.

Using short and wide traces to route gate-drive signals helps minimize impedance in gate-drive paths. In **Figure 13**,

DESIGN NOTES

1.5A Rail-to-Rail Output Synchronous Step-Down Regulator Adjusts with a Single Resistor

Design Note DN506

Jeff Zhang

Introduction

A new regulator architecture the LTC3600 (first introduced with the LT3080 linear regulator) has wider output range and better regulation than traditional regulators. Using a precision 50µA current source and a voltage follower, the output is adjustable from "0V" to close to V_{IN}. Normally, the lowest output voltage is limited to the reference voltage. However, this new regulator has a constant loop gain independent of the output voltage giving excellent regulation at any output and allowing multiple regulators to be paralleled for higher output currents.

Operation

The LTC3600 is a current mode monolithic step-down buck regulator with excellent line and load transient responses. The 200kHz to 4MHz operating frequency can be set by a resistor or synchronized to an external clock. The LTC3600 internally generates an accurate 50µA current source, allowing the use of a single external resistor to program the reference voltage from 0V to 0.5V below V_{IN}. As shown in Figure 1, the output feeds directly back to the error amplifier with unity gain. The output equals the reference voltage at the I_{SET} pin. A capacitor can be paralleled with R_{SET} for soft start or to improve noise while an external voltage applied to the I_{SET} pin is tracked by the output.

Internal loop compensation stabilizes the output voltage in most applications, though the design can be customized with external RC components. The device also features a power good output, adjustable soft-start or voltage tracking and selectable continuous/discontinuous mode operation. These features, combined with less than 1µA supply current in shutdown, V_{IN} overvoltage protection and output overcurrent protection, make this regulator suitable for a wide range of power applications.

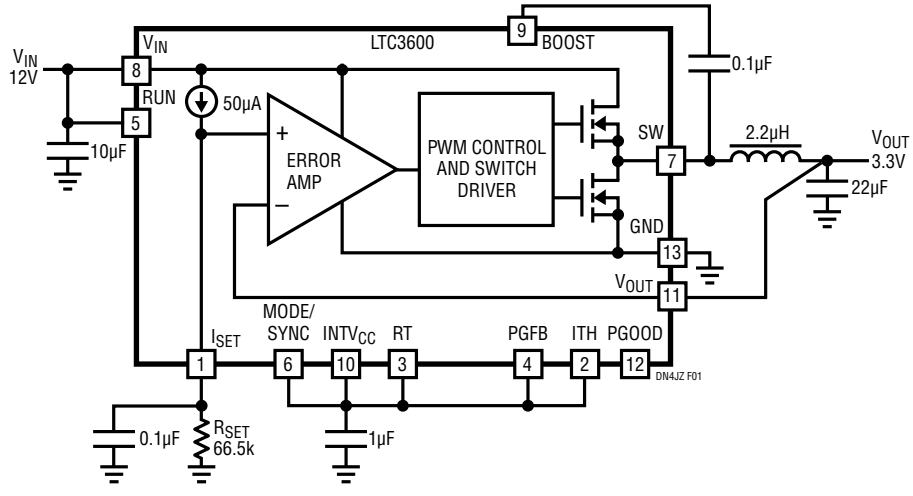
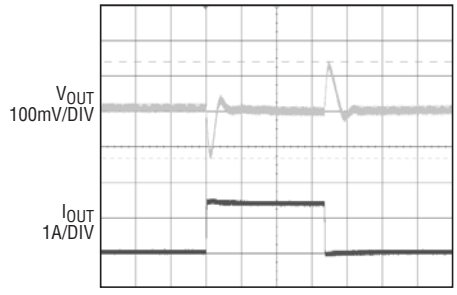


Figure 1. High Efficiency, 12V to 3.3V 1MHz Step-Down Regulator with Programmable Reference

Applications

Figure 1 shows the complete LTC3600 schematic in a typical application that generates a 3.3V output voltage from 12V input. Figure 2 shows the load step transient response using internal compensation and with external compensation. Figure 3 shows the efficiency in CCM and DCM modes. Furthermore, the LTC3600 can be easily configured to be a current source, as shown in Figure 4. By changing the R_{SET} resistance from 0Ω to 3kΩ, the output current can be programmed from 0A to 1.5A.



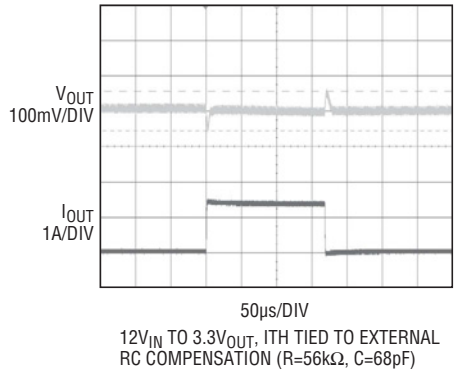


Figure 2. 0A to 1.5A Load Step Response of the Figure 1 Schematic

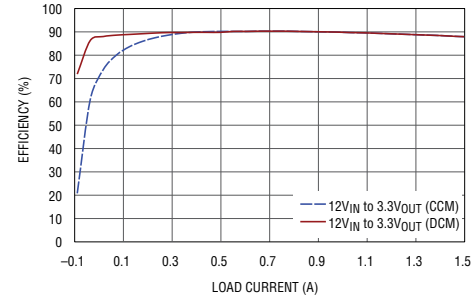


Figure 3. Efficiency of 12V Input to 3.3V Output Regulator in CCM and DCM Mode

Conclusion

The LTC3600 uses an accurate internal current source to generate a programmable reference, expanding the range of output voltages. This unique feature gives the LTC3600 great flexibility, making it possible to dynamically change the output voltage, generate current sources, and parallel regulators for applications that would be difficult to implement using a standard DC/DC regulator configuration.

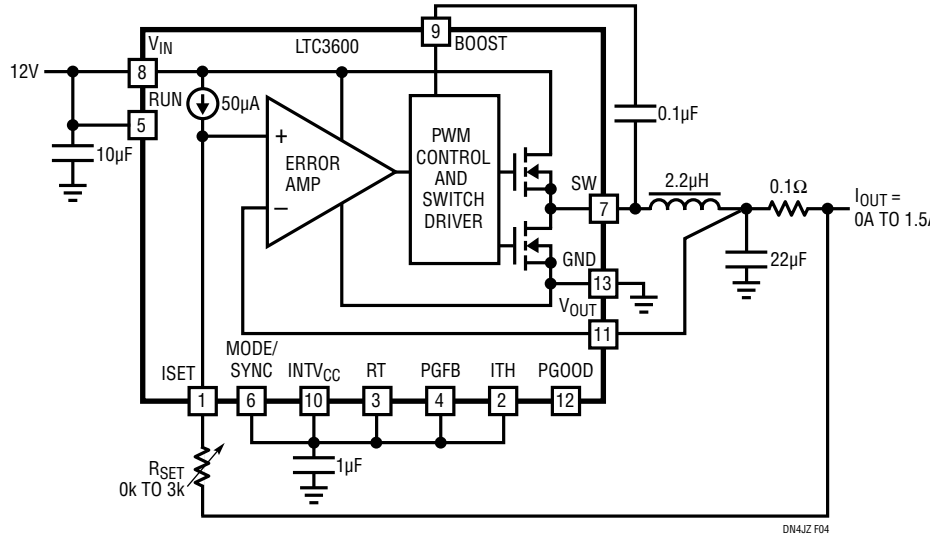


Figure 4. The LTC3600 as a Programmable 0A to 1.5A Current Source

Data Sheet Download

www.linear.com

For applications help,
call (408) 432-1900, Ext. 3845

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

dn506 AP/LT 0912 196k • PRINTED IN THE USA

DESIGN NOTES

36V, 3.5A Dual Monolithic Buck with Integrated Die Temperature Monitor and Standalone Comparator Block

Design Note 492

Edwin Li

INTRODUCTION

Multioutput monolithic regulators are easy to use and fit into spaces where multichip solutions cannot. Nevertheless, the popularity of multioutput regulators is tempered by a lack of options for input voltages above 30V and support of high output currents. The LT3692A fills this gap with a dual monolithic regulator that operates from inputs up to 36V. It also includes a number of channel optimization features that allow the LT3692A's per-channel performance to rival that of multichip solutions.

The LT3692A is available in two packages: a 5mm × 5mm QFN and a 38-lead plastic TSSOP. Although Both include the full feature set, the TSSOP package enhances the thermal performance of the dual buck.

HIGH INPUT VOLTAGE WITH HIGH TRANSIENT CAPABILITY

The LT3692A can operate up to an input voltage of 36V and can sustain a transient voltage up to 60V for 1 second, making it suitable for harsh operating environments such as those commonly found in automotive environments.

ON-DIE TEMPERATURE MONITORING

The LT3692A provides an on-die temperature monitoring function which facilitates the application circuit design, debugging and package thermal optimization. The voltage at T_J pin is directly proportional to the die temperature in Celsius (i.e., 250mV equals 25°C and 1.5V equals 150°C).

The measured temperature of the LT3692A TSSOP die tops out at 80°C* with the two outputs each supporting 3A loads at 5V and 3.3V from an input voltage of 18V,

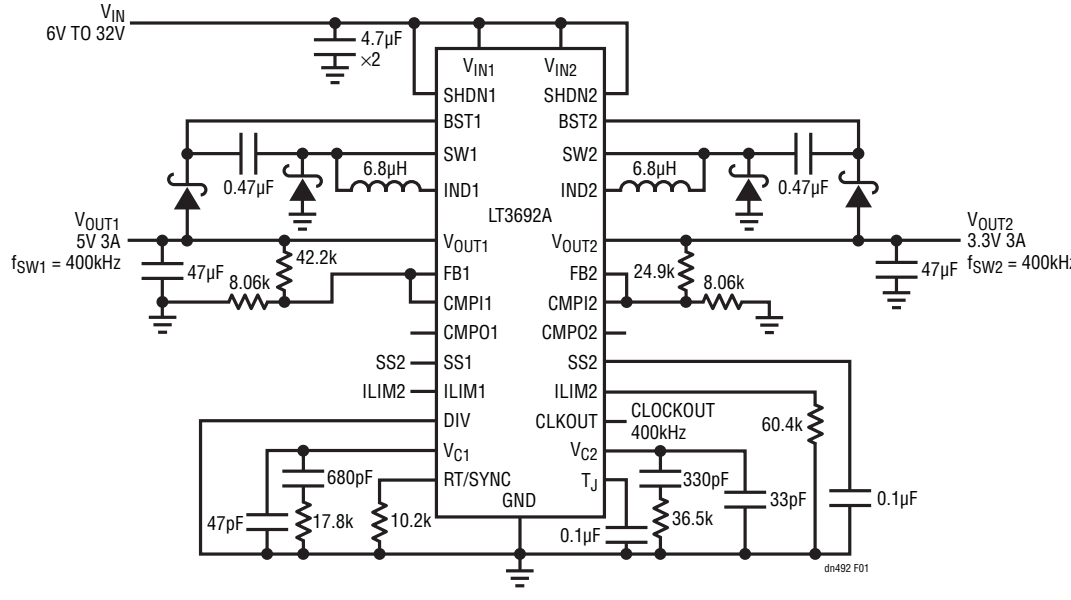


Figure 1. Dual 5V/3A/400kHz, 3.3V/3A/400kHz Application Keeps Temperature Rise Low at a V_{IN} of 18V

with a switching frequency of 400kHz. Figure 1 shows the schematic of the measured application circuit. The same setup, but with 2.5A loads, drops the max die temperature to 68°C.*

STANDALONE COMPARATOR BLOCK

The LT3692A also includes a standalone comparator block, which provides a 720mV threshold with hysteresis and outputs an open-collector signal. This comparator can be configured as a power good flag signal by connecting CMPI pin to FB pin to monitor the output voltage. It can also be configured as a temperature flag, which gives a warning signal when the die temperature rises to a preset point. This function is realized together with the on-die temperature monitor. Figure 2 shows how to configure a 100°C temperature flag.

OTHER FEATURES

Independent Adjustable Current Limit

The switch current limit on each output can be programmed from 2A to 4.8A. This expands the number of loading combinations that can be safely implemented without risking thermal overload of the package under extreme conditions, such as a short-circuit. Likewise, the current limit can be used to protect the part in compact designs where the saturation margin on inductors is lowered to meet size constraints.

Independent Synchronization

Independent synchronization allows any phase difference between the two outputs besides the standard 0° and 180°. The phase difference on the LT3692A is adjusted by controlling the duty cycle of the synchronization signal.

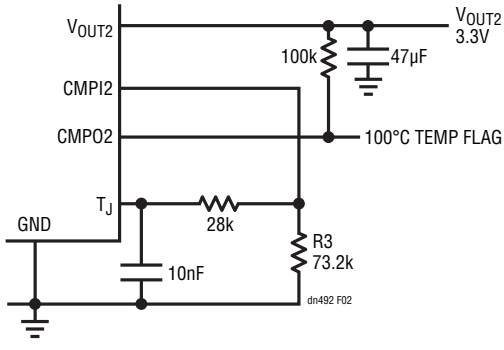


Figure 2. Temperature Flag Using Comparator Block and Temperature Monitor

*T_J pin reading on a standard demo board (DC1403A) running in a 25°C ambient temperature environment.

Frequency Division

Frequency division makes it possible to tune the operating frequency of each channel to optimize overall performance and size. The frequency of channel 1 can be programmed to run at 1, 1/2, 1/4 or 1/8 the frequency of channel 2. Figure 3 shows the layout of a 3.3V/2.5A/550kHz channel and a 1.2V/1A/2.2MHz channel application. The relatively low 550kHz frequency of V_{OUT1} maximizes channel 1's input voltage to 36V while meeting minimum on-time requirements and keeping the efficiency high. The high 2.2MHz frequency of V_{OUT2} allows the use of smaller components for channel 2 as shown in Figure 3. Despite the reduction in size, electrical and thermal performance is uncompromised.

CONCLUSION

The LT3692A is a dual output monolithic regulator that combines the ease-of-use and compact solution size of typical monolithic regulators with the flexibility of discrete, multichip solutions. Its high transient voltage capability, die temperature monitor, standalone comparator block, adjustable current limit, adjustable switching frequency and frequency division function and independent synchronization enable the LT3692A to work in many applications that other monolithic chips cannot.

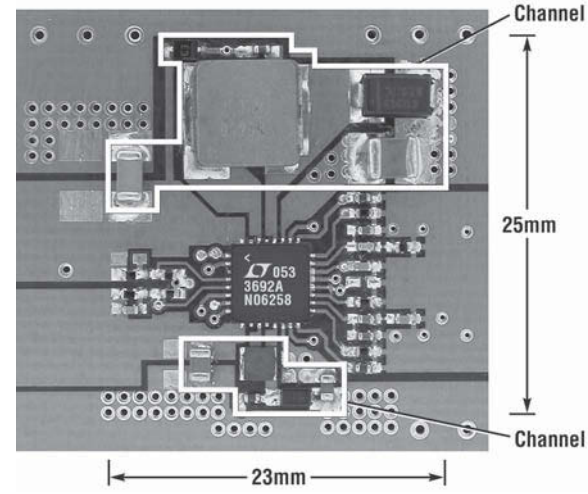


Figure 3. Dual 3.3V/2.5A/500kHz, 1.2V/1A/2.2MHz Layout. Channel 2 Requires Half of the Area of Channel 1

Data Sheet Download

www.linear.com

For applications help,
call (408) 432-1900, Ext. 3209

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

dn492f LT/TP 0711 226K • PRINTED IN THE USA

you should route top FET-driver traces TG and SW together with a minimum loop area to minimize inductance and high-dv/dt noise. Similarly, route bottom FET-driver trace BG close to a PGND trace.

If you place a PGND layer under the BG trace, the ac-ground return current of the bottom FET will automatically be coupled in a path close to the BG trace. Alternating current will flow to where it finds the minimum loop/impedance. In this case, a separate PGND return trace for the bottom gate driver is not required. It is best to minimize the number of layers on which the gate-driver traces are routed; doing so prevents gate noise from propagating to other layers.

Of all the small-signal traces, current-sensing traces are the most sensitive to noise. The current-sensing signal amplitude is usually less than 100 mV, which is comparable to the noise amplitude. In the LTC3855 example, the Sense$^+$/Sense$^-$ traces should be routed in parallel with minimum spacing (Kelvin sense) to minimize the chance of picking up di/dt-related noise, as **Figure 14** shows.

In addition, the filter resistors and capacitor for current-sensing traces should be placed as close to the IC pins as possible. This setup provides the most effective filtering in the event that noise is injected into the long sense lines. If inductor DCR current sensing is used with an R/C network, the DCR sensing resistor, R, should be close to the inductor, while the DCR sensing capacitor, C, should be close to the IC.

If you use a via in the return path of the trace to Sense$^-$, the via should not contact another internal V_{OUT}+ layer. Otherwise, the via may conduct large V_{OUT}+ current, and the resulting voltage drop may distort the current-sensing signal. Avoid routing the current-sensing traces near the noisy switching nodes (TG, BG, SW, and BOOST traces). If possible, place the ground layer between the current-sensing traces and the layer with power-stage traces.

If the controller IC has differential-voltage remote-sensing pins, use separated traces for the positive and negative remote-sensing traces, with Kelvin sense connection as well.

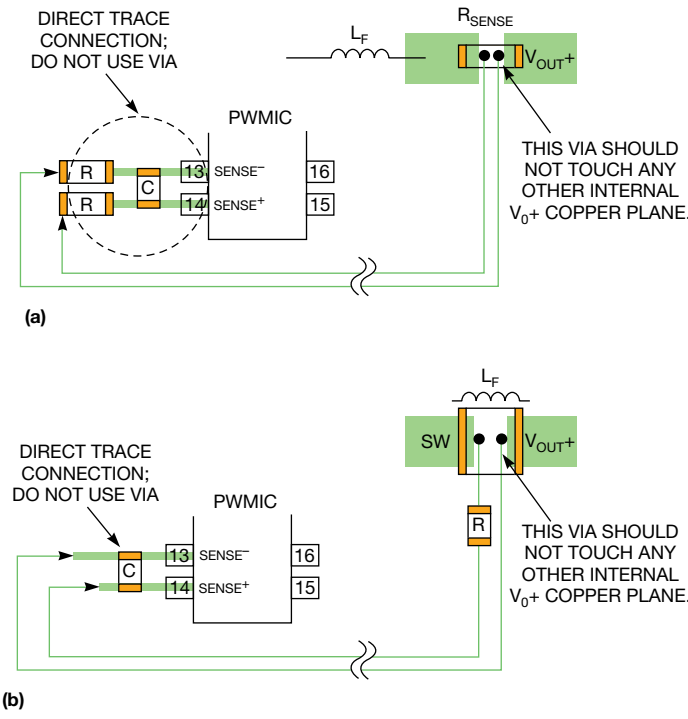


Figure 14 Kelvin sensing is shown for current sensing, R_{SENSE} (a) and inductor DCR sensing (b).

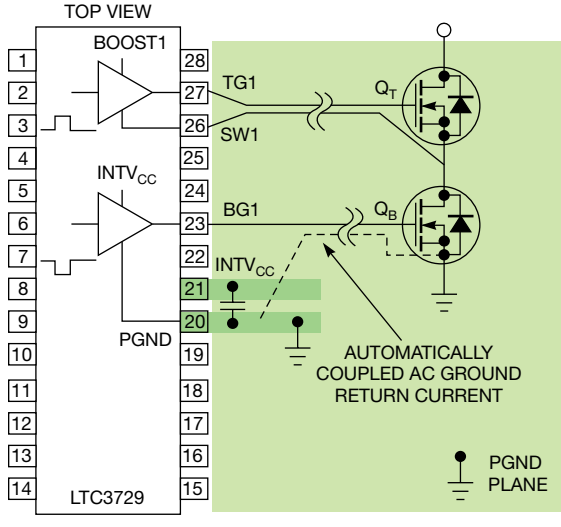


Figure 13 When routing MOSFET gate-driver traces, using short and wide traces helps minimize impedance in gate-drive paths. The gate-driver current paths should have minimum loop areas.

TRACE-WIDTH SELECTION

Current level and noise sensitivity are unique to specific controller pins; therefore, you must select specific trace widths for different signals. In general, the small-signal nets can be narrow and routed with 10- to 15-mil-wide traces. The high-current nets (gate driving, V_{CC}, and PGND) should be routed with short and wide traces. At least a 20-mil width is recommended for these nets.

LAYOUT CHECKLIST

Table 1, available online at http://bit.ly/Ruxanc, provides a sample checklist of the dual-phase LTC3855 supply shown in **Figure 10**. Using such a checklist will help ensure a well-laid-out power-supply design. EDN

AUTHOR'S BIOGRAPHY

Henry Zhang is an applications engineering manager for power products at Linear Technology Corp. He received his bachelor of science degree in electrical engineering from Zhejiang University in China in 1994 and his master's and doctoral degrees in electrical engineering from Virginia Polytechnic Institute and State University (Blacksburg, VA) in 1998 and 2001, respectively.

Distributed

Factorized

Power Management

Innovation

Integration

Performance

Speed

Efficiency

Density

More **Flexibility**

Support

Expertise

Productivity

Reliability

Qualified

Vicor gives power system architects the flexibility to choose from modular, plug-and-play components, ranging from bricks to semiconductor-centric solutions with seamless integration across all power distribution architectures.
From the wall plug to the point of load.

Don't let inflexible power products slow you down.
Choose from limitless power options to speed your competitive advantage.

Flexibility. Density. Efficiency.
Trust your product performance to Vicor

VICHIP
High Performance Power Modules

PICOR
Semiconductor Power Solutions

BRICK
Flexible Module Power

VICOR
The Power Behind Performance

vicorpower.com/rp/flexibility/edn

designideas

READERS SOLVE DESIGN PROBLEMS

Three-channel white-LED driver uses simple step-down dc/dc converter

Nora Jacalan Esteves, Technor Semiconductor LLC, Pleasanton, CA

With only a few additional components, you can use a highly efficient step-down dc/dc converter to create a constant-current, multiple-channel LED driver. It is relatively easy to drive a single-channel LED; however, it becomes more complicated when driving multiple-channel paralleled LEDs.

In normal dc/dc-converter applications, the control circuitry uses a power stage comprising an inductor and a capacitor, along with feedback through a resistor-divider network, to generate a regulated constant voltage and thus a constant current through the resistor divider. You can use an LED in place of the upper resistor of the feedback-divider network to allow the LED to be driven with a constant regulated current. The current flowing through the LED will be equal to the reference voltage of the dc/dc converter divided by the resistance of the grounded bottom resistor.

Although this method works well with one LED channel, it cannot be used to drive multiple parallel LED channels, because the mismatch in LED voltage drops would cause one LED channel to consume most of the current. As a result, only one LED channel would be lighted.

You can use the circuit in **Figure 1** to drive multiple paralleled LED channels

DIs Inside

▸To see and comment on all of *EDN*'s Design Ideas, visit www.edn.com/designideas.

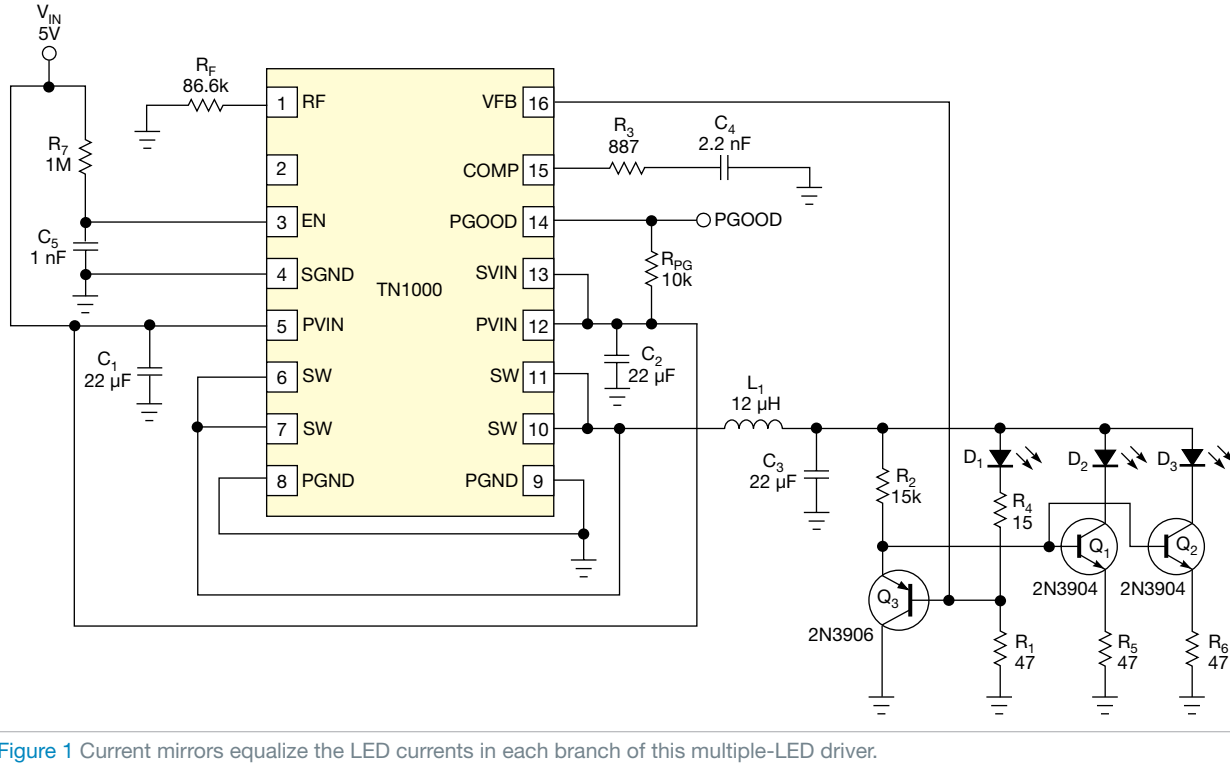


Figure 1 Current mirrors equalize the LED currents in each branch of this multiple-LED driver.

with only one dc/dc converter by adding a simple current-mirror scheme to generate the constant current required for each LED channel. The IC used in the **figure** is the TN1000, a 100-mA current-mode step-down dc/dc converter from Technor Semiconductor (**Reference 1**).

The voltage step-down stage consists of a 12-µH inductor and a 22-µF capacitor. The first LED channel for D_1 is driven by a regulated current of 17 mA, which is equal to the IC's 0.8V reference voltage divided by R_1. The voltage across C_3 will be regulated to whatever voltage is required to support the voltage across D_1 and R_4, as well as the 0.8V across R_1.

Emitter follower Q_3 drives the bases of Q_1 and Q_2, which mirror the 17 mA of D_1. The V_{BE} drops of emitter followers Q_1 and Q_2 are similar to and compensate for the V_{BE} drop of Q_3, so the voltage across R_5 and R_6 is also a constant 0.8V, and D_2 and D_3 are driven with a constant 17 mA.

R_4 is set so that the voltage across C_3 is high enough such that Q_1 and Q_2 do not saturate. R_4 should be set so that the voltage across C_3 can support the highest LED voltage plus approximately 255 mV to keep Q_1 and Q_2 from saturating. EDN

REFERENCE

1 "TN1000 100-mA Monolithic, Synchronous Step-Down DC-DC Converter," Technor Semiconductor, July 2011, http://bit.ly/MMw1WY.

Sense automobile high-side current with discrete components

Larry Beaty, Beatys Mills, Comer, Georgia

This Design Idea came about as a result of my not having access to those wonderful new ICs that sense current. I needed a discrete circuit that I could build easily but that would still be as accurate as the new ICs. This circuit seems to do the job.

Q_2 is the first current amplifier; it has a gain of 6.2 (**Figure 1**). Q_1 is the temperature-compensation amplifier controlled by IC_{1B}, which keeps the Q_1 collector voltage constant no matter what the temperature does to the circuit. The reference voltage for the circuit is the 5V system supply. The voltages noted on the schematic are as built.

IC_{1A} differentially amplifies the Q_1 and Q_2 collector voltages. The op amp has a gain of 4.9.

R_3 comprises two surface-mount power resistors, stacked one atop the other. The circuit has a range of 25A in for 5V out. This setup works nicely with an analog input to the microprocessor.

The two zener diodes protect the circuit from the automobile electrical system. Such systems have been known to spike to –90V.

If you want to get critical, match R_6 and R_7; more critical again, also match R_1 and R_4. I didn't do this step, and the mismatch did not seem to affect the operation. All resistors except R_3 are 1% 0805 SMT.

Observe sufficient copper weight and width on your PCB traces for maximum current-carrying capacity, and be sure to use Kelvin connections to R_3. This circuit ran slightly warm to the touch at 25A. EDN

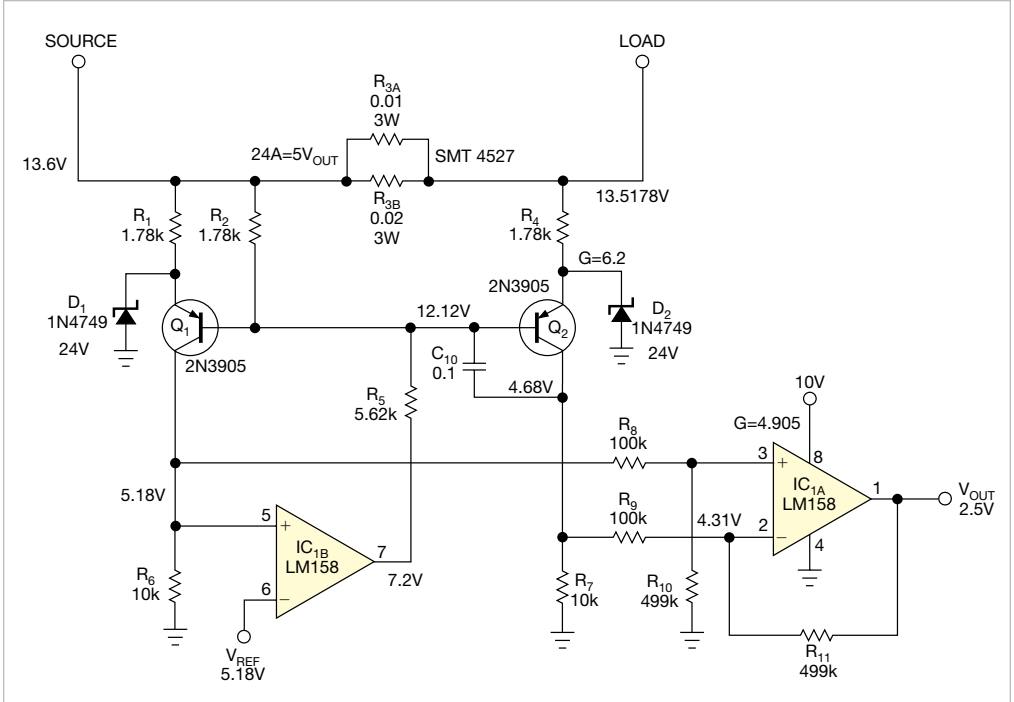


Figure 1 Q_1 and Q_2 convert the high-side voltage drop across current-sense resistor R_3 into a voltage that is within the common-mode range of IC_2.

THEY SAY:

"ANALOG INTEGRATION CAN'T BE DONE."

TRANSLATION:

"WE JUST DON'T REALLY WANT TO DO IT."

IT'S TIME TO BRING ANALOG *TOGETHER*.

www.maximintegrated.com

maxim integrated™

Dramatically increase the frequency range of RC-based voltage-controlled oscillators

Shawn Stafford, Pittsburgh, PA

A typical voltage-to-frequency converter—also known as a VCO (voltage-controlled oscillator)—IC has a simple linear tuning characteristic relating input voltage to output frequency. It is usually of the form F=kV/RC, where RC is the time constant of the associated timing resistor and capacitor. The output frequency range of these parts varies, but few, if any, tune over the entire range with one set of RC timing components. If you change the timing ratio as the input voltage changes, however, you can magnify the tuning range to take advantage of nearly the entire frequency range in one implementation.

HYPERABRUPT VARACTORS YIELD BIG CHANGES IN FREQUENCY FROM SMALL BIAS-VOLTAGE SHIFTS.

One way to achieve this goal is to replace the timing capacitor with a variable capacitor whose capacitance inversely changes with bias voltage: a varactor diode (**Reference 1**). For this design, the Analog Devices AD654 voltage-to-frequency converter was considered because of its simplicity and bandwidth of at least 1 MHz (**Reference 2**).

Figure 1 shows a typical implementation using a fixed resistor and capacitor. For the values shown, this setup gives a frequency range of approximately 10 Hz to 30 kHz over 0 to 10V on the input. After replacing the timing capacitor with an NTE618 hyperabrupt varactor, as shown in **Figure 2**, the same input voltage range of 0 to 10V produced a tuning range of approximately 10 Hz to more than 1 MHz (**Reference 3**).

The plot in **Figure 3** compares the tuning curves of each converter configuration. Note the dramatic increase in range, but at the expense of linearity. Temperature stability will also be affected. Overall, precision is traded for tuning range, which should be acceptable in basic applications that do not require the specified precision.

The hyperabrupt varactor allows large changes in frequency for small changes in bias voltage because of the large capacitance ratio. For some hyperabrupt varactors, the ratio can be as high as 15, as in the case of the NTE618, a

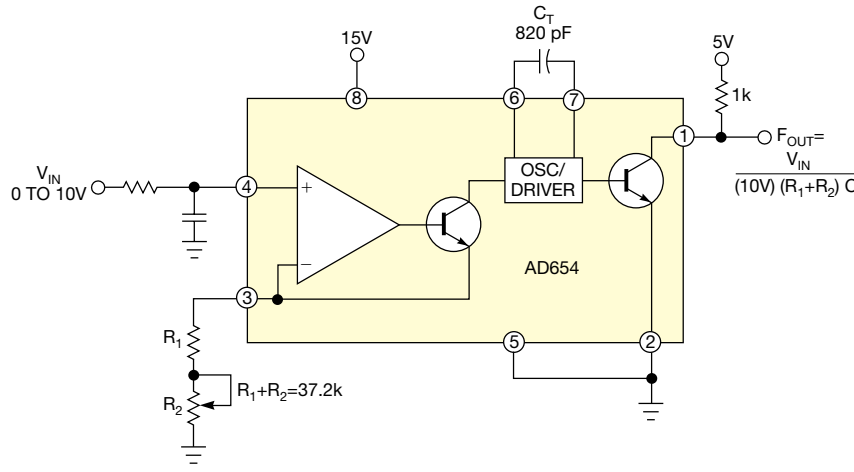


Figure 1 The usual usage of this VCO IC is with a fixed timing capacitor, C_T, at pins 6 and 7.

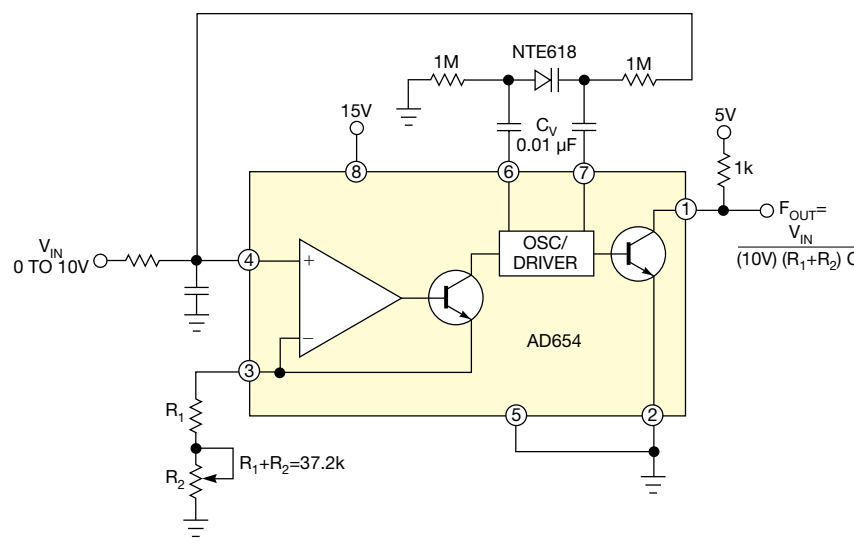


Figure 2 A voltage-variable capacitor (varactor) and an ac-coupled dc-bias network replace the fixed timing capacitor.

varactor that AM receivers use. As the frequency of the converter increases with higher voltage, the capacitance decreases, which in turn increases the frequency. This combination of responses generates the wide tuning range. The 0.01-µF coupling capacitors separate the varactor bias voltage from the operation of the converter core. Light varactor biasing with high-value, 1M resistors prevents additional loading of the oscillator.

This behavior is calculable and predictable to some degree, even from the data sheets. The tuning curve for the varactor diode can be generated in Microsoft Excel. This information then can be used in the voltage-to-frequency-conversion equation for the converter. For the NTE618, the approximate relationship of capacitance to voltage is expressed as $C=800E^{-10}\times e^{-0.46V}$.

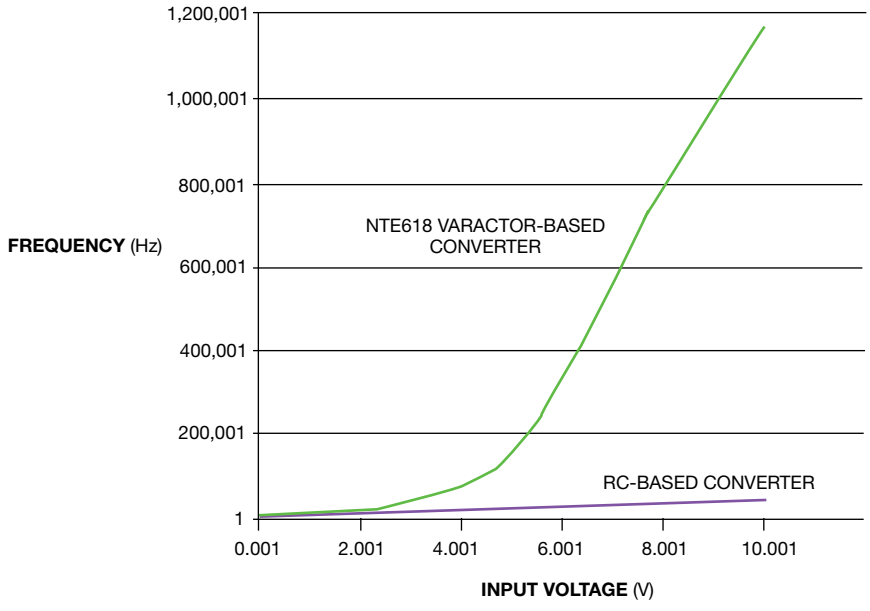


Figure 3 Replacing the fixed timing capacitor with a voltage-variable capacitor results in a much wider tuning range.

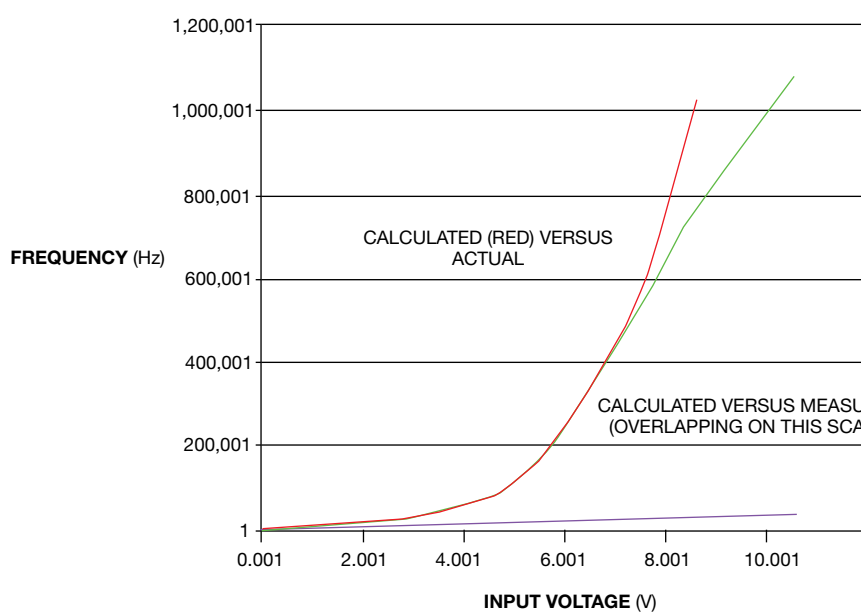


Figure 4 The calculated and measured responses are in close agreement.

Figure 4 shows the similarity between the calculated and measured results. The higher frequencies differ more as the varactor capacitance reduces to the order of the stray capacitance in the circuit and parts. Careful layout can minimize this issue and increase the range.

Note that at low input voltages, the varactor-based response and the fixed-capacitor converter response are nearly identical because of the varactor's inverse exponential relationship to the voltage. One useful result of achieving this range is eliminating the need to switch between converters to extend the tuning range. You can explore other useful and interesting applications using this approach with phase-locked loops, modulators, or function generators.

Editor's note: Figure 13 of the Analog Devices AD654 data sheet contains errors (**Reference 2**). The 74LS86 and LM360 cannot be subjected to 15V, and R_7 is most likely 8.2k, not 8.2Ω. EDN

REFERENCES

1 Williams, Jim, and David Beebe, "Switching-regulator supply provides low-noise biasing for varactor diodes," *EDN*, Nov 9, 2000, pg 117, www.edn.com/4359609.

2 "AD654: Low Cost Monolithic Voltage-to-Frequency Converter," Analog Devices, http://bit.ly/MMCdOE.

3 "NTE618 Varactor Silicon Tuning Diode for AM Radio," NTE Electronics, http://bit.ly/NLnZMQ.

Crystal-oscillator circuit is ultralow power

Thomas Mathews, Texas Instruments

For battery-powered circuits, it is easy to build an ultralow-current crystal oscillator designed around a 32.768-kHz crystal. This crystal is common for real-time-clock circuits. Because these circuits must operate at all times, achieving the lowest current draw possible is mandatory. Traditional gate-oscillator circuits—the 74HC04, for example—can draw several milliamps; the circuit shown in **Figure 1** normally draws only about 5 µA. This circuit uses the Texas Instruments LPV7215MF comparator, which is housed in a five-pin SOT-23 package. The operating current for this comparator is 580 nA; the entire circuit shown in **Figure 1** draws only 5 µA when running from a 3.3V supply.

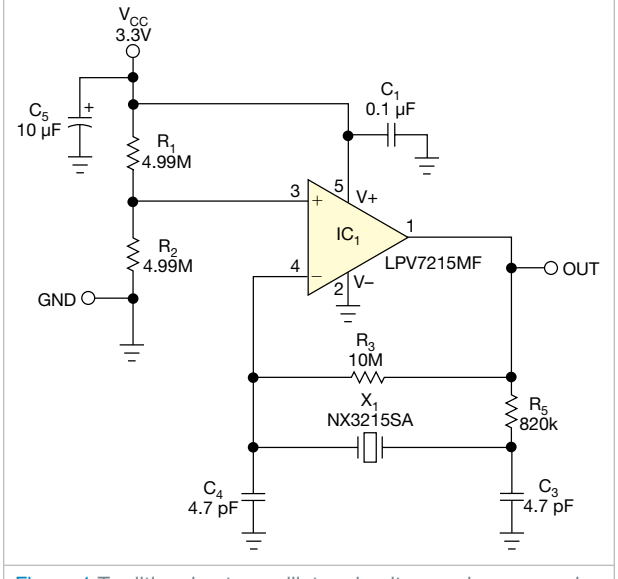


Figure 1 Traditional gate-oscillator circuits can draw several milliamps; the circuit shown normally draws only about 5 µA.

TABLE 1 LOADING ESTIMATES

Source	Supply current (µA)
LPV7215MF	0.58
R_1 and R_2 bias	0.33
R_3	0.083
Crystal network (estimated)	2
10-MΩ probe load	0.165
20-pF load capacitance	2.163
Estimated total	5.321
Actual total	5

Multiple copies of this circuit have been built and tested to confirm the 5-µA current draw. The largest portion of the 5 µA goes to the largely unavoidable operations of charging and discharging the output load capacitance. The circuit was tested using a standard 10-MΩ oscilloscope probe with about 10 pF of shunt capacitance; operating current into more capacitive loads will be higher. **Table 1** breaks down the power consumption piece by piece.

Capacitive loads must be charged by the upper transistor in the active output stage of the LPV7215. To charge a capacitor to 3.3V, note the capacitor **equation** Q=C×V. This charge is transferred into the capacitance during the first half of each cycle of the 32.768-kHz oscillation. During the second half, the charge is transferred to ground. As a result, the output-stage current, i, will be i=f×Q=f×C×V. For 20 pF (a 10-pF scope probe plus a PCB parasitic), i=(32.768 kHz)(20 pF)(3.3V)=2.163 µA.

From the **equation** above, it can be seen that additional output loading or higher operating frequencies will draw more output current. Anything that can be done to reduce the capacitive load will reduce the total current draw.

Figure 2 shows an example of the test boards used to create the crystal-oscillator circuit.

Typical LR44 alkaline button-cell batteries (**Figure 3**) have a capacity of 150 mAhr. With 5 µA of current draw, this clock circuit could run for about 30,000 hours, or 3.4 years. EDN

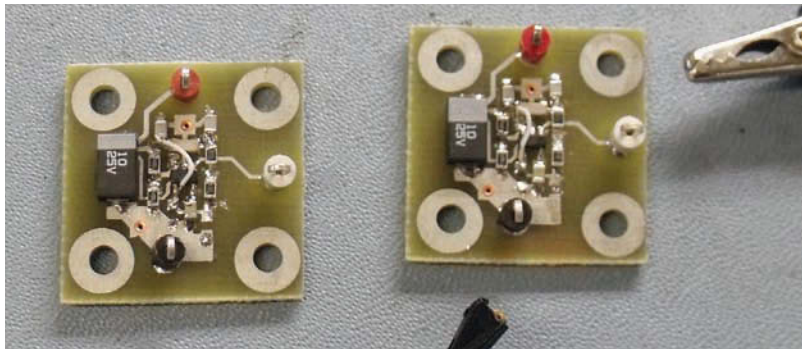


Figure 2 Test boards of a crystal-oscillator circuit are based on the Texas Instruments LPV7215MF comparator.

Figure 3 Typical LR44 alkaline button-cell batteries supply 150 mAhr of capacity.

designideas CLASSICS

Originally published in the Feb 4, 1991, issue of *EDN*

Buffers stabilize oscillator

Maxwell Strange, Goddard Space Flight Center, Greenbelt, MD

Adding a CMOS buffer to a classic op-amp oscillator dramatically improves its performance while preserving its low cost and low power consumption.

The overriding source of frequency drift in **Figure 1a** is the nonsymmetry and variability of the op amp's output-saturation voltages. These effects produce output-amplitude variations, which, when fed to the inputs via R_1 and R_2, produce switching-threshold changes. Supply voltage, temperature, loading, and op-amp selection also affect these saturation voltages. You can clamp the op amp's output with reference diodes, but such diodes are expensive and power hungry.

The circuit of **Figure 1b** overcomes these problems and has other advantages as well. Gates A and B produce a rail-to-rail voltage swing to feed back to the circuit's input, eliminating the saturation-voltage drops of the op amp. If you select the proper op amp, only the circuit's passive components will affect its frequency stability. The circuit's output symmetry is nearly perfect over a wide range of supply voltages. Further, the buffers' output transitions are much faster than the op amp's slew-rate-limited transitions, allowing you to use a micropower op amp.

The circuit's output frequency is:

$$f_o=\frac{\log e}{2\log\left(1-\frac{2R_1}{2R_1=R_2}\right)RC},$$

$$R_1=\frac{R_1'R_2'}{R_1'+R_2'},$$

$$\text{if } R_2=3R_1,\ f_o\approx\frac{0.979}{RC}.$$

EDN

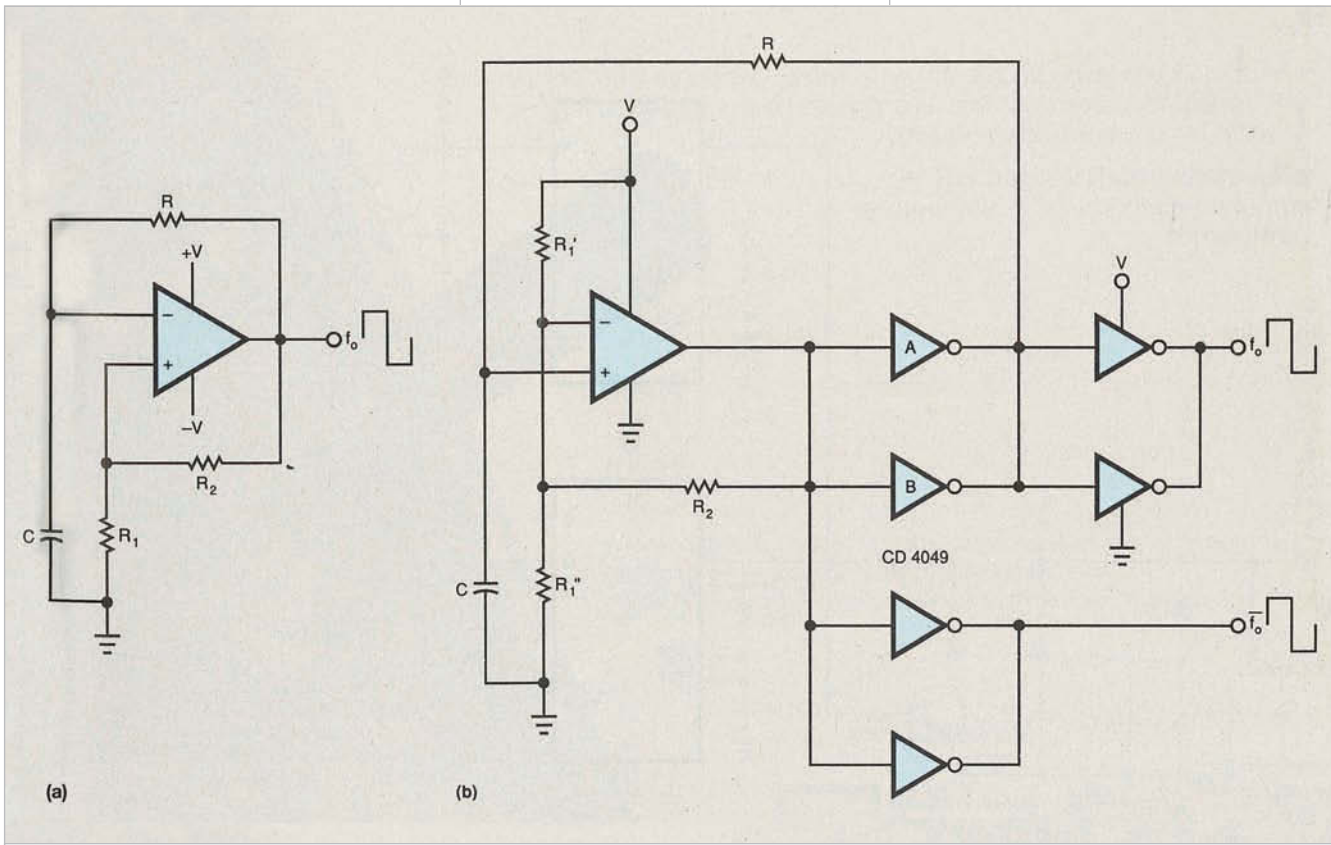


Figure 1 Adding CMOS buffers to a classic op-amp oscillator (a) improves the oscillator's performance without significant increases in power consumption or cost (b).

Global supply chain: still a work in progress

If manufacturing had remained in one place, the supply chain would look very different today. But globalization has changed the very nature of the industry. Supply-chain partners source, build, and deliver all over the world. Whether it means maintaining facilities in strategic locations or establishing partnerships that span the globe, the supply chain now operates 24/7.

Developing the optimum global footprint is still a work in progress. Component makers, following their OEM customers around the world, initially built regional factories. Since the early 1980s, economic downturns, obsolescence, and overcapacity have shuttered many of those sites, and the fabless semiconductor model has gained strength. Distributors, which expanded primarily through acquisition, have struggled with disparate IT systems, inconsistent franchises, and the need to retain local identities. For these two key suppliers to OEMs, flexibility remains the defining strategy for success.

Cost-cutting measures during the 1980s and 1990s drove suppliers to create hubs. Instead of maintaining manufacturing facilities and sales offices in all locales, suppliers began to centralize production and warehousing regionally. Local warehouses were replaced by mega-warehouses serving the Americas, EMEA, and the Pacific Rim. Financially, this approach strengthened the supply chain. Distributors could leverage economies of scale through centralized inventory, and manufacturers honed their just-in-time and lean skills. Twin natural disasters in 2011, however, forced a reassessment of those strategies.

A recent Gartner Group report (http://bit.ly/MpVrH4) argues that the best supply-chain performers are adopting a "multilocal" strategy. Companies are trying to balance the advantages of global economies of scale with local service and responsiveness, the report says.

The Gartner report identifies several other factors driving the multilocal trend: "Tax and other government incentives, coupled with meaningful concessions from organized labor, are enticing manufacturers to set up or expand operations in mature markets. Annual wage increases between 9% and 35% in China, combined with rising logistics expenses, are leading to higher core supply-chain costs in a traditionally low-cost country."

A demand to remain responsive to local markets is further fueling this trend, according to Gartner, and a growing sophistication with such techniques as cost-to-serve analysis is enabling it. Even within emerging markets, manufacturers are shifting capacity based on regional wage and logistics-expense differentials.

Two global companies have recently announced plans to expand in the Americas. Microsoft Corp said it would manufacture its Surface tablet in the United States, and Apple Inc announced plans to expand in Texas. Apple has had a well-known partnership in China with Foxconn Electronics, but the Taiwan-based EMS provider has been raising wages following a public outcry over its treatment of workers. Foxconn also has announced plans to expand in Brazil, which has been a center of activity for a number of high-tech companies, including Avnet Inc, Samsung, Motorola, Research In Motion, SinoHub, and Ciao Telecom.

Suppliers and distributors are generally well prepared in these regions but continue to expand. In Europe, the struggling economy has provided acquisition opportunities for distributors. In early July, Arrow Electronics Inc and Avnet announced a number of acquisitions of European IT and component distribution companies. Though the distributors merge operations when it makes sense, local offices and practices are often maintained long after mergers are completed. Even global customers tend to have unique requirements from region to region, so channel partners manage both sales and engineering resources accordingly.

Most tier-one distribution companies have established a physical presence in each of the world's regions. A global footprint, however, does not make all sales and service offerings identical. Some services that have been around for decades, such as kitting and programming, are offered in all regions, but others have yet to migrate. Reverse logistics and aftermarket services, for example, started in the Americas but are expected to roll out worldwide.

> The best supply-chain performers are adopting what Gartner calls a multilocal strategy.

One persistent challenge is that regulatory mandates governing the collection and disposal of electronic products vary considerably from region to region. In addition, regional franchises limit distributors' ability to sell all products in all locales. Pricing disparity also presents hurdles.

Distributors and component suppliers acknowledge it is their job to work through those issues for OEM customers. Being there, as the saying goes, is only half the battle.

—by Barbara Jorgensen, *EBN* community editor

This story was originally posted by EBN: *http://bit.ly/Ns3lQa.*

TOP GUNS.

IP&E SOLUTIONS FROM AVNET

Your top flight semiconductor cannot work alone.

You need world-class interconnect, passive and electromechanical components to support your design. Avnet's legacy in the IP&E business dates back to 1921 and is stronger than ever today. As a worldwide distributor of IP&E products, we source from the leading global manufacturers – and you can count on us to provide top quality components to meet your needs. We are ready to help your products take flight.

What can we do for you? www.avnetexpress.com

Accelerating Your Success!™
1 800 332 8638 | www.avnetexpress.com | @avnetdesignwire

AVNET® electronics marketing

productroundup

PROCESSORS

NI control system supports digital energy conversion in the field

The NI Single-Board RIO GPIC (general-purpose inverter controller) from National Instruments provides a standard RapidIO architecture for smart, grid-tied power-conversion systems. It includes a comprehensive NI LabVIEW system-design tool chain to reduce the cost and risk of embedded-system design. The GPIC provides a standard set of analog and digital I/O and 58 DSP cores embedded in the FPGA fabric to meet the specific control, I/O, performance, and cost needs of most smart-grid power-electronics applications. NI says the 58-DSP-core hardware-parallel Xilinx Spartan-6 FPGA outperforms the performance per dollar, per chip, and per watt of typical dual-core DSPs by a respective 40, 24, and 10×. The embedded, 400-MHz PowerPC processor with VxWorks real-time OS supports smart-grid networking protocols DNP3, IEC 60870-5, and IEC 61850. An evaluation kit sells for $1499.

National Instruments, www.ni.com

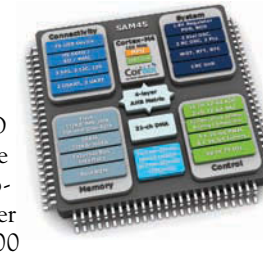
TI KeyStone multicore DSPs offer scalability

Texas Instruments has fielded a highly dense and scalable solution, including development software, for developers migrating from single-core to multicore designs for enterprise gateway applications such as session border controllers and IP PBX gateways. The pin-compatible KeyStone-based TMS320C665x multicore DSPs provide a balanced alternative that scales for voice processing, signaling, and system control. The single-core, 850-MHz TMS320C6654 DSP supports up to 64 G.729AB channels, delivering 27.2 GMACs and 13.6 Gflops; the single-core, 1-GHz TMS320C6655 supports up to 128 G.729AB channels, delivering 40 GMACs and 20 Gflops. The TMS320C6657, with two 1.25-GHz DSP cores, delivers up to 80 GMACs and 40 Gflops. Under normal operating conditions, the C6654, C6655, and C6657 power numbers are 2, 2.5, and 3.5W, respectively. Pricing starts at just under $30 (10,000).

Texas Instruments, www.ti.com

Atmel Cortex-M4-based microcontroller delivers high flash density

Atmel Corp expects volume availability this month for the SAM4SD32, a Cortex-M4 processor-based microcontroller with 2 Mbytes of embedded flash for industrial and consumer applications requiring increased program memory and data storage with low power consumption, such as wireless thermostats, GPS sport watches, smart meters, and 1D bar-code readers. The SAM4SD32 microcontroller offers power consumption of 200 µA/MHz in active mode—a savings of more than 50% over the nearest competitor, according to Atmel—when running at its maximum operating frequency of 120 MHz. It integrates cache memory for accelerated code execution out of flash, as well as 160 kbytes of SRAM. The dual-bank flash enables in-field firmware upgrades. In QFP100 packaging, the microcontroller sells for $7.94 (1000).



Atmel Corp, www.atmel.com

IMMERSE YOURSELF

Santa Clara Convention Center Oct 30-Nov 1, 2012

Welcome to the premier annual industry event for engineers and developers of next-generation smart, connected devices. Explore chip and system design. Connect with software development pros. Ponder the next phase of innovation in IT for the enterprise. It's all here at ARM® TechCon™, where the future starts today.

Register online and **Save 15%** with promo code ARM15.

Register here: www.ARMTechCon.com

ARM 2012 TechCon™

Join the community defining the future

productroundup

Freescale builds 32-bit microcontrollers around Cortex-M0+

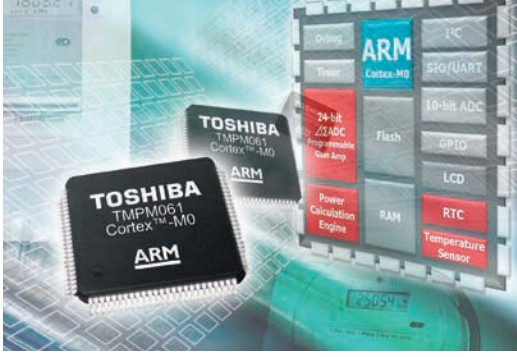
Freescale Semiconductor touts the Kinetis L series as the first microcontrollers built on the ARM Cortex-M0+ processor. The 32-bit devices target consumer and industrial apps using 8- and 16-bit architectures. The series supplements the energy efficiency of the 498-MHz Cortex-M0+ core with a low-power microcontroller-platform design, low-power operating modes, and energy-saving peripherals.

The product consumes 50 µA/MHz in very-low-power run mode. The entry-level Kinetis L0 has 8 to 32 kbytes of flash and comes in a 4×4-mm QFN package. The L1 offers 32 to 256 kbytes of flash and additional communications and analog peripheral options. The L2 adds USB 2.0 full-speed host/device/OTG (On-the-Go). Devices are sampling now; volume pricing will start at 49 cents (10,000). The Freescale Freedom development platform, available in the third quarter, sells for $12.95.

Freescale Semiconductor,
www.freescale.com

TAEC optimizes microcontroller for smart meters

The TMPM061, a 32-bit RISC microcontroller built around the ARM Cortex-M0 processor core, replaces a two-chip analog front end with a single IC to reduce the footprint and the component and system costs for smart meters. An onboard power-calculation engine calculates active and reactive energy and power factor while monitoring voltage and frequency fluctuation. Developers can modify and update the basic energy-use calculation function. The microcontroller includes a three-channel, high-precision, 24-bit delta-sigma ADC; a 10-bit ADC; a temperature-compensated real-time clock; and up to 128 kbytes of on-chip flash ROM and 8 kbytes of on-chip RAM. It comes



in a 14×14-mm, 100-pin low-profile quad flat package; operates with input voltages from 1.8 to 3.6V; and has four standby modes to conserve power. Samples are available for $3.50 each.

Toshiba America Electronic Components,
www.toshiba.com/taec

On Semi designs PLC modem SOC for harsh environments

On Semiconductor is offering a PLC (power-line carrier) modem SOC for use in e-metering, home automation, solar energy, and lighting control. The NCN49597 combines a low-power, 32-bit ARM Cortex-M0 with a high-precision analog front end. Based on a dual 4800-baud spread-frequency shift-keying channel technology, the SOC is optimized for power efficiency and performance but provides robustness and reliability for operation in harsh environments. The NCN49597 fully complies with the prevailing IEC 61334-5-1 standard but also supports customized implementations. It comes with open-source PLC platform code and a development environment. The NCN49597 operates from a 3.3V power supply, has a junction operating temperature range of −40 to +125°C, and is housed in a QFN-52 package measuring 8×8×1 mm. The price is $4.99 (2500); lead times are eight to 16 weeks.

On Semiconductor,
www.onsemi.com

ARM, Cadence collaborate to optimize Cortex-A-based SOCs

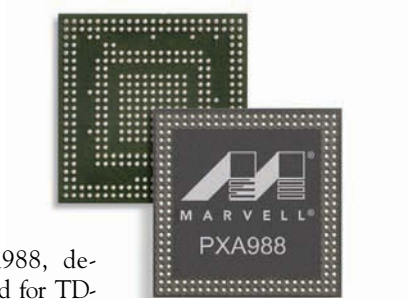
ARM and Cadence Design Systems Inc have announced the first in a series of combined solutions to improve performance, power, and time to market for SOCs based on ARM Cortex-A series processors. Available for license from ARM, the initial offering optimizes ARM POP (Processor Optimization Pack) intellectual-property technology—using the Cadence Encounter digital platform—for the Cortex-A9 on TSMC's 40LP process, including an ultralow-threshold-voltage version. The resulting solution is available for license from ARM to accelerate the implementation of ARM processors. ARM's POP comprises core-hardening acceleration technology that taps ARM Artisan advanced physical IP to optimize power, performance, and area metrics. The collaborative solution couples the POP IP to Cadence Encounter RTL-to-GDSII offerings, including RTL Compiler-Physical and clock-concurrent-optimization design technology. Extending to TSMC 28HPM, the collaboration addresses single-, dual-, and quad-core implementations of Cortex-A9 and Cortex-A15 processors.
ARM, www.arm.com
Cadence, www.cadence.com

Digital Core Design 32-bit core runs µCLinux

The D68000 IP Core from Digital Core Design is 100% compatible with the Motorola/Freescale 68000 but runs with the µCLinux operating system. µCLinux is a Linux derivative for embedded systems that dispenses with the memory-management unit but supports the Common Linux Kernel API, multitasking, full-featured TCP/IP networking, and Virtual File System. The D68000 ships with a fully automated test bench and complete test set to simplify package validation at each stage of the SOC design flow. It also is equipped with a DoCD-BDM hardware debugger. The D68000 is binary-compatible with the m68k family of MPUs, and it has a 16-bit data bus and a 24-bit address data bus. Its code is compatible with the MC68008 and upwardly code compatible with the MC68010 virtual extensions and the MC68020 32-bit implementation of the architecture.
Digital Core Design, www.dcd.pl

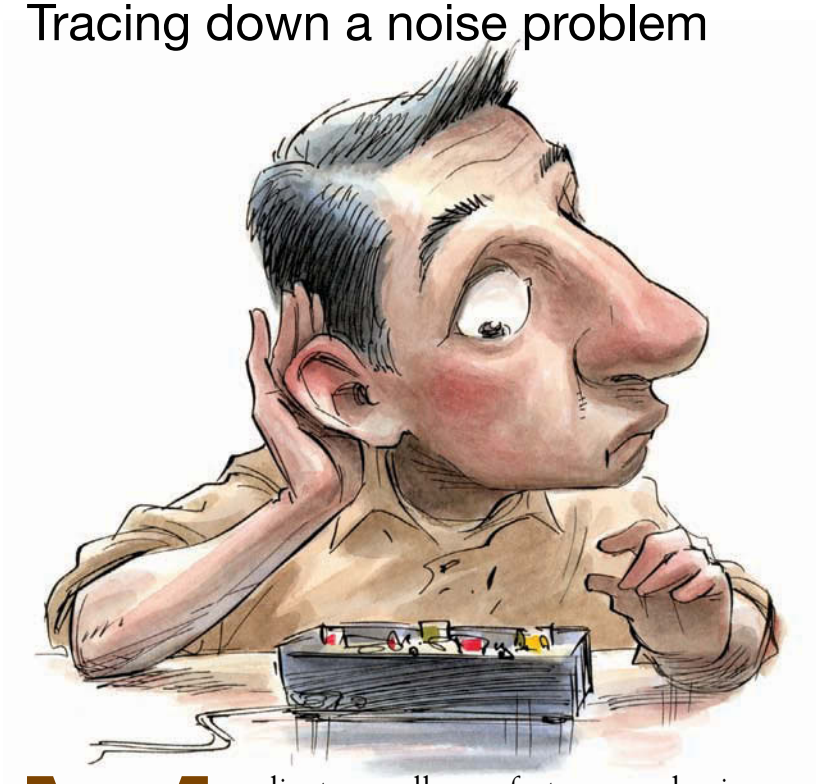
Marvell tunes dual-core SOCs for TD-SCDMA, W-CDMA

Marvell designed the PXA988 and PXA986, based on 1.2-GHz dual-core processors with wireless modems, as a 3G chip set for the TD-SCDMA and W-CDMA markets. The unified 3G design incorporates an application and communications processor with wireless chips for Wi-Fi and Bluetooth; FM radio, near-field communications, and GPS; RF transceivers; and power management. The dual-core



PXA988, designed for TD-SCDMA, uses 1.2-GHz Cortex-A9 processors and supports full 1080p encode/decode. It has an integrated image-signal processor, an advanced graphics-processing unit that can achieve 192 million triangles/sec, and a 533-MHz LPDDR2 memory architecture. A TD-HSPA+ R8 modem supports dual-carrier aggregation. The PXA986 is pin compatible with the PXA988. Evaluation boards and silicon samples are available now; form-factor reference designs are slated to be available by the end of the third quarter.
Marvell, www.marvell.com

Tracing down a noise problem



My client, a small manufacturer, was having a noise problem with a new batch of 1500V-dc supplies. It had been a while since the company manufactured this product. The original engineer was long gone, and the only documentation was a schematic. The approach was a straightforward closed-loop design. An op amp controlled an oscillator that used a step-up transformer to create the high voltage, which the system rectified and filtered into dc. A small part of the output voltage fed back into the inverting input of the op amp as an error signal to adjust the oscillator frequency when necessary. The noninverting input was grounded.

The manager assured me that no changes to the design had been made between this lot and the last one. None of the old, working units were available, however, so I had to jump in cold.

Noise appeared on the output and on the error signal entering the op amp and exiting the op amp. This situation is typical of a closed-loop system, and opening the loop only causes the circuit to fail. I saw the same noise on the power supplies; that could have been either a cause of the problem or just a symptom.

I tacked a couple of capacitors across the power supplies to filter out the noise. No difference. I tried additional capacitors at different places, again to no avail.

After asking permission to cut some traces, I isolated the power entering the op amp. I inserted a 50Ω resistor in series to the positive and negative supplies and bypassed that with 100- and 0.1-µF capacitors. This lowpass filter should have removed the noise and provided clean power to the chip, but noise was still everywhere.

The result told me something important, however: The noise had to be coming from the loop itself and not from outside. The power-supply noise was a result of the problem, not the cause. The rapidly varying high-voltage output was stressing the supply too quickly for the three-terminal regulators to compensate. And because noise on the filtered op-amp supply was still occurring, that meant the op amp was drawing current erratically and causing its local power to fluctuate.

I examined the noise for a clue to its source, but it looked like just plain noise. A spectrum analyzer might have been useful, but an oscilloscope and volt-ohm milliammeter were all I had.

I cut the loop to see if something was generating the noise. As soon as I did, the noise went away, but the circuit failed—more confirmation that the noise was being generated inside the loop.

I contemplated the schematic; there had to be a point at which noise was getting into the loop. Finally, I saw it.

The noninverting input to the op amp was grounded. What if it hadn't been grounded? An open circuit here could certainly pick up noise and affect the loop. I measured that pin's resistance to ground. It was 0.23Ω, which was just the ohmmeter's lead resistance. Rats!

It did get me thinking, though. Everything pointed to the op amp as the source of the noise. If it wasn't coming from the inverting input, it had to be coming from the noninverting input.

I put the oscilloscope probe on the noninverting input; it was as quiet as a mouse. I then saw that my scope's ground lead was close to the chip. I moved the ground clip to the power-supply ground and found noise on the "grounded" noninverting input. I took some thick hookup wire and ran it directly from the power-supply ground to the noninverting input. The noise went away, and the circuit worked perfectly. Success!

Clearly, someone had made changes to the PCB; otherwise, the previous batch would have failed, too. The manager admitted there had been some PCB changes, "but the circuit wasn't changed." In other words, change is in the eye of the beholder. EDN

Gerard Fonte is the principal engineer for electronic-product design and development firm The Pak Engineers (East Amherst, NY).

DANIEL VASCONCELLOS

From extreme value to extreme performance.

InfiniiVision 2000 & 3000 X-Series

Infiniium 90000 Q-Series

New Infiniium 90000 Q-Series

The fastest real-time oscilloscope with 63 GHz bandwidth

Whether you need the fastest real-time oscilloscope on earth with the highest measurement accuracy anywhere, or something a little more basic, Agilent oscilloscopes outperform in every category. That's why discerning engineers have made Agilent the fastest growing oscilloscope company in the world since 1997. Like you, we're working on what's next.

That's thinking ahead. That's Agilent.

See the 90000 Q-Series
http://goo.gl/ngThk

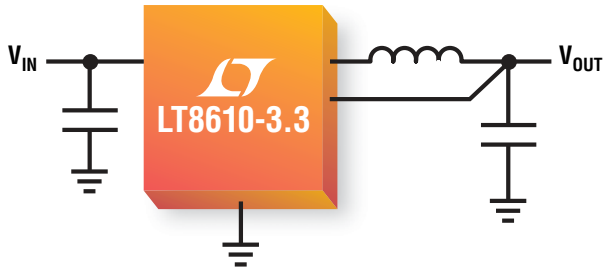
See the fastest real-time scope
www.agilent.com/find/90000QSeries

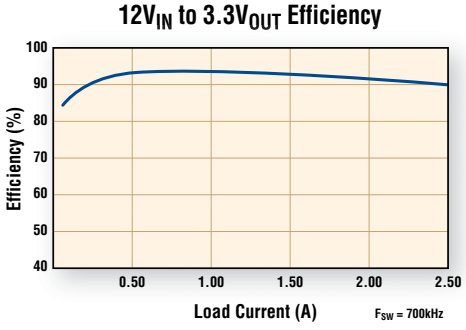
u.s. 1-800-829-4444 canada 1-877-894-4414

Anticipate ___Accelerate ___Achieve

Agilent Technologies

42V, 2MHz Sync Buck





2.5A Output Current, 2.5µA I_Q, 94% Efficient

The LT®8610/11 are our first constant frequency, ultralow quiescent current high voltage monolithic synchronous buck regulators. They consume only 2.5µA of quiescent current while regulating an output of 3.3V from a 12V input source. Their low ripple Burst Mode® operation maintains high efficiencies at low output currents while keeping output ripple below $10mV_{P-P}$. Even at >2MHz switching frequency, high step-down ratios enable compact footprints for a wide array of applications, including automotive. The LT8611 enables accurate current regulation and monitoring for driving LEDs, charging batteries or supercaps, and for controlling power dissipation during fault conditions.

Features

- 3.4V to 42V Input Range
- 2.5µA I_Q Regulating @ $12V_{IN}$ to $3.3V_{OUT}$
- Output Ripple $<10mV_{P-P}$
- 99.9% Duty Cycle for Low Dropout
- 94% Efficiency at 1A, $12V_{IN}$ to $3.3V_{OUT}$
- >2MHz Operation even with High Step-down Ratios
- Accurate Input/Output Current Regulation, Limiting and Monitoring (LT8611)

LT8610 Demo Circuit

Actual Size
15mm x 18mm

Info & Free Samples

www.linear.com/product/LT8610

1-800-4-LINEAR

http://video.linear.com/114

LINEAR TECHNOLOGY