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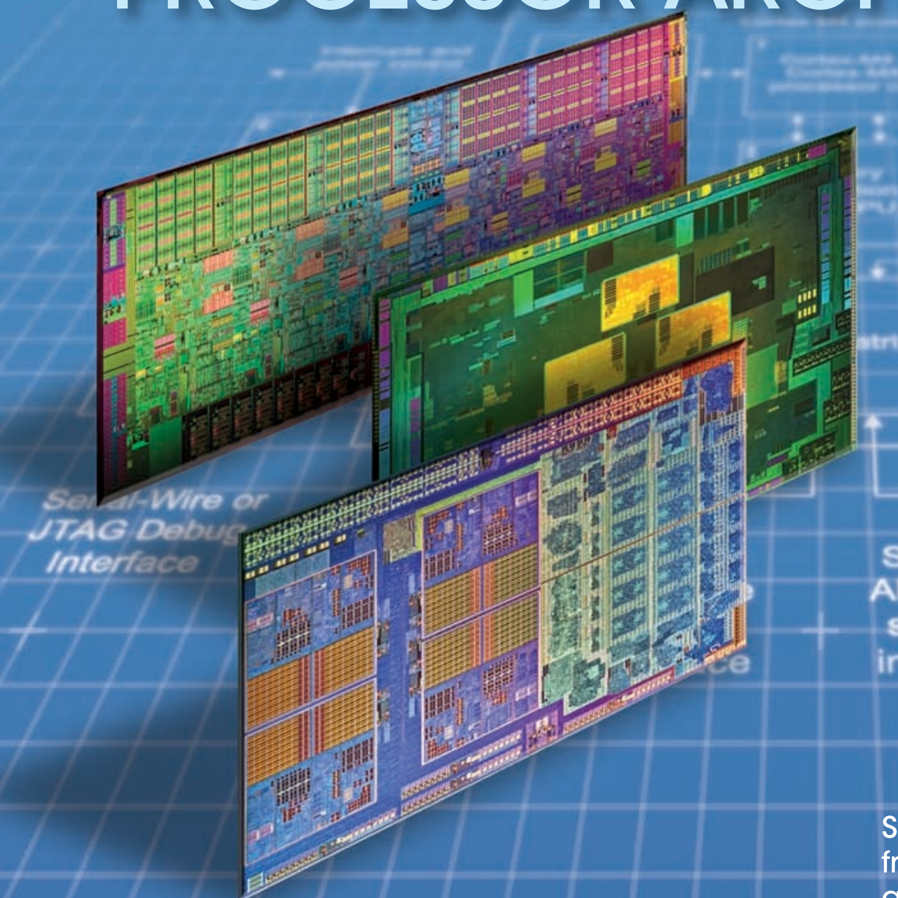

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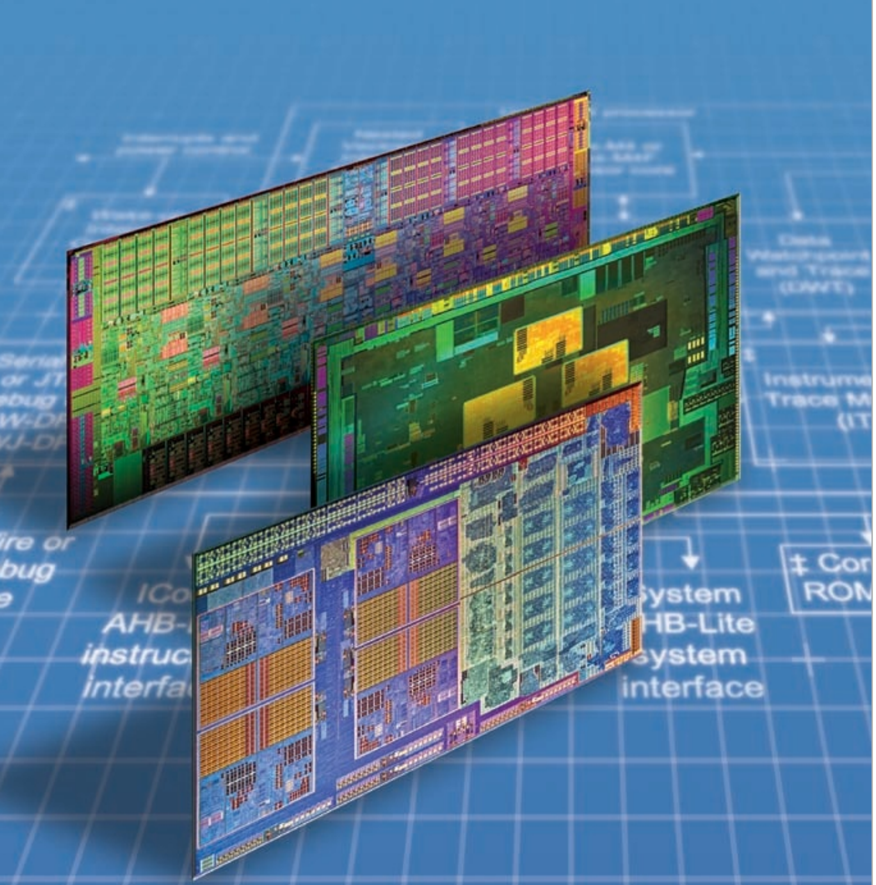

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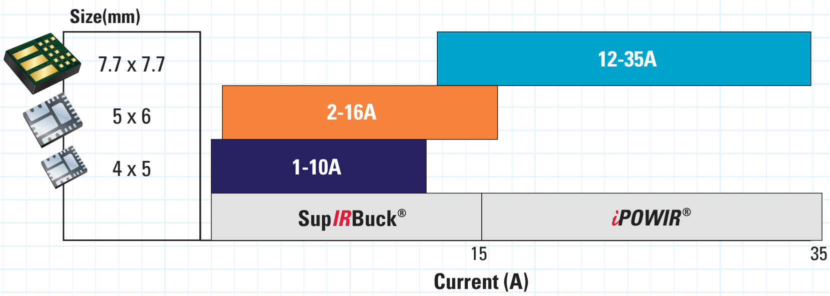

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JOIN THE CONVERSATION

Comments, thoughts, and opinions shared by *EDN*'s community

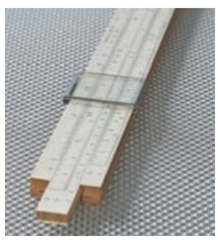
In response to the blog post "5 Engineers: What makes someone an engineer?" at www.edn.com/4396843, Roger.Harker commented:

"An intense curiosity about how things work was the starting point for me; then wanting to build and fix things; and, finally, getting an education and experience to do original design. Although I am retired, I still try to stay current. Lifelong learning is a key part of being an engineer."

In response to "Morse code on Earth," a blog post by Doug Grant at www.edn.com/4397154, Deloca commented:

"For me, the beauty of Morse code is that it can be used not just with radio, but literally with any carrier signal that can be modulated with 'on-off' actions—for instance, visible light using a bulb or even a mirror reflecting a bright source of light, such as the sun. As someone mentions on the page, in a disaster scenario there may be no other way to communicate the state of survivors other than using Morse with the available medium."

In response to the slideshow "Slide rules and charts—a personal collection" at www.edn.com/4396854, skenn_ie commented:



"A slide rule, like an abacus, is much quicker in experienced hands, as long as you don't need four-digit accuracy. It's also great for verifying that you haven't dropped or gained a decimal place."

EDN invites all of its readers to constructively and creatively comment on our content. You'll find the opportunity to do so at the bottom of each article and blog post.

CONTENT

Can't-miss content on EDN.com

SLIDESHOW: WORLD MAKER FAIRE 2012

More than 500 engineers, hobbyists, and makers from around the world showcased their diverse creativity and innovations in technology, craft, science, fashion, art, food, and more at World Maker Faire in late September—all in an attempt to openly exchange ideas and knowledge while sparking one another's inventiveness. Review some of the highlights of the New York event and other Maker Faires in this collection of content.

www.edn.com/4397366

APPLE TEARDOWN AND ANALYSIS COLLECTION

What makes Apple so great, anyway? *EDN* looks at the designs that give Apple products their shine through hands-on teardowns and analysis of popular Apple consumer electronics in this collection of content, including teardowns of the recently released iPhone 5 and its associated earbuds.

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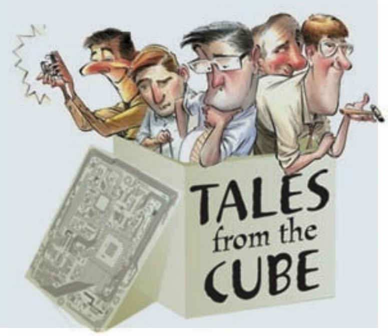
In *EDN*'s Tales from the Cube, engineers relate their most vexing design challenges—and how they conquered them. From the cubicle to the test bench to the field, hear how your peers solve real-world problems. If you've got a story to share, e-mail it as an 800-word document to *EDN* at **teamEDN@ubm.com.** Make sure to include your name and a brief bio.



BY PATRICK MANNION, BRAND DIRECTOR

Could this take the $10 million Tricorder X Prize?

Graham Ewing's demonstration of Virtual Scanning, his entry for the $10 million Qualcomm Tricorder X Prize competition, had all the hallmarks of a "Mission Impossible" scene: a new, as yet untapped but all-seeing chromotherapy analysis technique; top-secret mathematical formulas, developed by an obscure Russian scientist named Igor; visa-dodging meetings in Istanbul. Where was the candid camera?

I would have checked for that camera, perhaps hidden somewhere high on the DESIGN East conference ceiling, but Ewing's demo was engrossing. It took me a while to figure out how adjusting colors on a computer could help diagnose everything from diabetes to mental characteristics. Ewing didn't want me looking at his mental state on the screen, so we focused on the biological portion. That was OK; there was still a lot to digest.

I got lessons in medical diagnostics, chromotherapy, organ-brain information transfer and processing, and the effects of various medical conditions on proteins. From there, I got a primer on how the light absorption and reflection of the characteristics of those affected proteins could be measured and then put through secret mathematical formulas to come up with a full physical and mental analysis. Heady, intoxicatingly perplexing stuff; I wanted to know more. So I persisted.

The demo itself started with an image, in this case of animals roaming an African plain. The subject gets a few minutes to memorize the image's hues. A monochrome version of the same image is then presented, and the subject has to re-create the colors of the original by adjusting a color palette. The subject repeats the process for a number of images to yield the final analysis data.

That data, showing the various mental and physical parameters of the subject, was mind-blowing—if it was accurate. Ewing, CEO of Montague Healthcare, swears by the Virtual Scanning technology and has vested his company with promoting and generating funding for the concept.

I wanted to get into how various organ ailments create and affect proteins, and to what level of accuracy the Virtual Scanning system could be relied upon. But then the X Prize folks with whom I'd arranged to meet (before I got somewhat hijacked by Ewing) arrived on the scene.

Alan Zack, senior director of marketing for the X Prize Foundation, and Mark Winter, senior director for the Qualcomm Tricorder X Prize (http://bit.ly/y6cSzE) and the Nokia Sensing X Challenge (http://bit.ly/K0BbgI), are encouraging collaboration between the competitors vying for the Tricorder X Prize and those pursuing the $2.25 million purse for the Nokia Sensing X Challenge, announced in May. They made their case by noting that the sensing requirements for a true tricorder would be demanding, and sensors would be fundamental to a tricorder's success.

As I listened, though, the Virtual Scanning demo nagged at the back of my mind; I couldn't put my finger on it, but something was bothering me. Later, as I walked the show floor, it hit me: The Virtual Scanning technique can't win the Tricorder X Prize, because for the technology to work the subject must be conscious, mentally stable, and responsive, as well as able to see without being impaired by color blindness.

A true tricorder, as any "Star Trek" fan knows, can render an accurate diagnosis regardless of the subject's physical or mental condition. In fact, as a Trekkie, I take issue with the Tricorder X Prize's vision of "a portable, wireless device in the palm of your hand that monitors and diagnoses your health conditions." That sounds, well, like a simple health monitor, not a tricorder. But the $10 million prize is nothing to sneeze at, and any advancement in this field is good.

The Virtual Scanning data was mind-blowing—if it was accurate.

On a DESIGN East panel later that day, Ewing sat next to another Tricorder X Prize contestant, Nanobiosym CEO Anita Goel, whose tricorder approach involves taking a blood sample and performing genetic analysis. That seems a lot more viable in the X Prize context than Virtual Scanning, but we'll learn more as the competition unfolds. To date, more than 260 teams have signed up for the Qualcomm competition, and 65 teams have already accepted the Nokia Sensing X Challenge.

I don't mean to write off the Virtual Scanner before it has a chance to prove itself. Ewing estimates the total market at £8 million to £12 million for a user base of 2 billion to 3 billion patients, though I don't think he's factoring in the caveats I've pointed out here. Still, the Virtual Scanner could be one more arrow in the medical-diagnostics quiver.

To judge the technology for yourself;. read "New Light on Chromotherapy: Grakov's 'Virtual Scanning' System of Medical Assessment and Treatment" (http://bit.ly/QY33Cl). Then weigh in at www.edn.com/4397726. EDN

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INNOVATIONS & INNOVATORS

Tektronix adds lower-priced mixed-domain scopes

Tektronix has added four attractively priced models to its 4000 series of DPOs (digital phosphor oscilloscopes), MSOs (mixed-signal oscilloscopes), and MDOs (mixed-domain oscilloscopes). The four instruments all possess four analog-input channels, with a 20M-point record length. Two are MDOs that combine the MSO's four analog- and 16 digital-input channels with a DSP-based spectrum-analysis function whose ability to capture and process analog, digital, and RF signals and quickly present them in multidomain, time-correlated displays is unmatched by any other instrument, according to Tektronix.

Prices are $7150 for the 100-MHz-bandwidth DPO, $9500 for the 100-MHz MSO, and $12,200 for a 100-MHz MDO that adds 50-kHz to 3-GHz spectrum-analysis capability to the 100-MHz MSO. An otherwise similar MDO that provides 350-MHz analog-input bandwidth sells for $16,700.

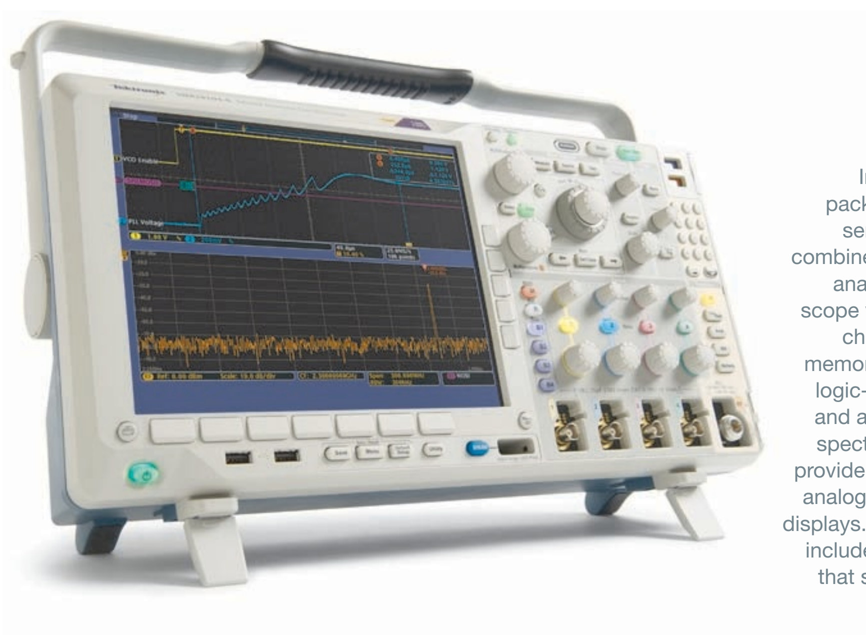
Thus, by reducing the scope function's analog bandwidth, the new products extend the lower end of the 4000 series DPO/MSO price range to less than $10,000 and add two MDOs at prices as low as $12,200. Previously, MDO prices started at $19,900.

Inexpensive RF technologies are finding their way into everyday applications, from apparel tags to live-stock-monitoring clips, price displays on store shelves, and short-range wireless remote control of household objects. Although many of these applications do not need high performance, the addition of RF greatly complicates debugging.

The value-priced models address this trend by letting engineers capture time-correlated analog, digital, and RF signals for a complete system view, saving days or weeks of debugging. The lower-priced instruments sacrifice analog bandwidth, but the bandwidth provided is suitable for debugging cost-sensitive embedded systems.

—by Dan Strassberg

▷**Tektronix Inc**, www.tektronix.com



In a 5.8-in.-deep package, MDO4000 series instruments combine a four-channel analog-input digital scope with 20M-point/channel waveform memory, a 16-channel logic-timing analyzer, and a DSP-based RF spectrum analyzer to provide time-correlated analog, digital, and RF displays. The series now includes MDO models that start at $12,200.

TALKBACK

"Familiarity breeds contempt. The more I know about the equipment I work with, the more weaknesses and errors I find. I work around them, but I am always on the lookout for new 'issues.' "

—Commenter Douglas.Butler, in response to the 5 Engineers blog question "Do you trust technology?" Add your own comment at www.edn.com/4397355.

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NATIONAL INSTRUMENTS™

8-bit USB microcontrollers slash power, form factor

For mobile and portable applications, small size and low power consumption are critical, but no market-leading embedded system can compromise on functionality. With its introduction of three new families of 8-bit USB PIC microcontrollers, Microchip offers engineers an array of devices that eliminate the need for an external crystal and feature ultralow power consumption while providing essential peripherals in a range of configurations. With up to 4 kbytes of RAM and 128 kbytes of flash on chip, the PIC MCUs require only 35 μA/MHz in active mode and offer sleep current as low as 20 nA.

The three families are the PIC16F145X and PIC18F2X/4XK50, both comprising three members, and the full-featured PIC18F97J94, comprising nine members. The 14- and 20-pin PIC16F145X devices are Microchip's lowest cost and smallest form factor USB MCUs to date, available in packages as small as 4×4 mm. The PIC18F2X/4XK50 family, available in 28- and 40/44-pin packages, includes Microchip's Charge Time Measurement Unit for touch-sensing and measurement applications and offers a pin-compatible migration path for legacy designs based on the PIC18 USB MCUs.

All devices in the three new 8-bit USB PIC MCU families include Microchip's mTouch technology to enable low-cost capacitive touch and proximity sensing.

The PIC18F97J94 family is Microchip's first to offer an integrated 60×8 LCD controller (for a total of 480 segments), real-time clock with V_{BAT}, and USB on a single 8-bit PIC MCU. Available in 64-, 80-, and 100-pin packages, devices in the PIC18F97J94 family include a 12-bit ADC, I^2C and SPI interfaces, and four enhanced USARTs.

All devices in the three new families include Microchip's mTouch for low-cost capacitive touch and proximity sensing.

The devices operate without an external crystal, saving as much as 15 cents in designs and shrinking the final design form factor. At the same time, they achieve the 0.25% accuracy required for USB. Here, the new PIC MCUs use an internal clock-tuning module that keys off of the USB start-of-frame bits received from a USB host. The devices nevertheless can self-tune from an external crystal.

Samples are available for all families. MCUs in the low-cost PIC16F145X family are available in volume now; the two other families are expected to ship in production volumes in early November. Pricing starts at 50 cents in volume.

—by Stephen Evanczuk

▷**Microchip Technology**, www.microchip.com

DILBERT By Scott Adams

10.12

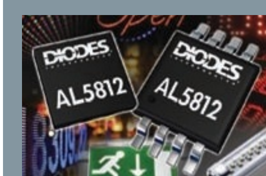
LINEAR LED DRIVER TARGETS LOW-CURRENT LIGHTING

The 60V AL5812 linear LED driver from Diodes Inc delivers a constant current of up to 150 mA. It is designed to provide designers of low-current illumination and signage applications with a simplified circuit solution for accurately controlling 0.5W LEDs. Housed in small-footprint, thermally enhanced SM package options, the driver can meet power-handling requirements over wide supply-voltage and ambient-temperature ranges.

LED current is set using a high-value resistor on the driver's low-voltage, 0.5V R_{SET} pin, enabling the specification of a lower-cost, smaller-footprint resistor to reduce total system BOM (bill of materials) cost. A standard low-value decoupling capacitor is the only other external component needed.

—Toni McConnel

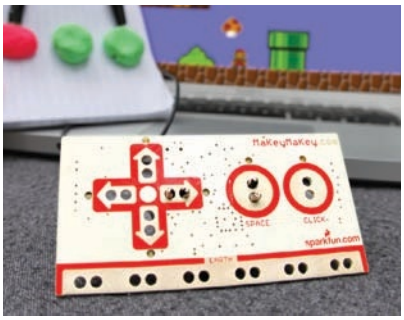
▶**Diodes Inc**, www.diodes.com



The 60V capability of the AL5812 lets it drive long LED chains while operating from rails as low 3.5V.

DIY is kick-started for the masses

A new kit is billing itself as an "invention kit for everyone," with no programming, no breadboarding, and no software needed. MaKey MaKey is a simple product that lets users "make anything a key." Basically, it's a PCB with an ATMega32u4 microcontroller running Arduino Leonardo firmware. It uses the USB HID (human interface device) protocol to communicate with a computer and can send key presses, mouse clicks, and mouse movements.



The simple MaKey MaKey invention kit lets beginners and experts in the fields of art, engineering, and everything in between turn everyday objects into touchpads and combine them with the Internet.

The MaKey MaKey site offers several simple ideas—a banana piano, for example—for using the kit. But with the kit's Arduino base, use of high-resistance switching for sensing closed switches, use of a 10- to 50-MΩ pull-up resistor with a moving window averager to lowpass the noise in software, and inclusion of six inputs on the front plus 12 on the back, there's a good deal a maker could do with it in a DIY project.

SparkFun Electronics is shipping the MaKey MaKey kit as part of its mission to lower the point of entry for beginning electronics enthusiasts and to encourage interest in engineering. Representatives from SparkFun are currently on a West Coast tour to support the company's Inventor Kit LabPack and other classroom kits. The focus is particularly, but not exclusively, classrooms. If you've ever wished SparkFun would present a workshop in your town, send a note to education@sparkfun.com.

MaKey MaKey was not born at SparkFun; MIT graduate students Jay Silver and Eric Rosenbaum designed it. It was, however, the first product SparkFun sold through the crowd-funding Web site Kickstarter. With a modest goal of raising $25,000, the site saw more than $550,000 invested by people all over the world who were looking to get their hands on this kit. That's some impressive public support of DIY and the maker movement!

The basic kit is priced at $39.95 and comes with the MaKey MaKey HID board, an alligator-clip pack, and a mini-USB cable. The deluxe kit, priced at $49.95, includes the same components as the basic kit, in addition to a second alligator-clip pack, a jumper-wires pack, and a roll of copper tape.

—by Suzanne Deffree

▷**MaKey MaKey**, www.makeymakey.com

VOICES

Avnet's Roy Vallee: Design careers are marathons, not sprints

Avnet Inc's Roy Vallee, who started in the stockroom and worked up the ranks to become CEO and chairman, retired his executive seat and is not seeking re-election to the board when his term expires in October. During his more than 35 years with Avnet, Vallee was instrumental in increasing the distributor's geographic coverage, scale, and design scope. He spoke with *EDN* in late September about the changes he's seen in the electronics industry, the evolving needs of design engineers, and the career advice he'd offer to those just starting out. Excerpts of that conversation follow. Read the full interview at www.edn.com/4398412.

Why did you retire your CEO seat in July 2011?

A There's a time and place for everything. There's a certain amount of CEO turnover that's good for the business. Too much is bad. But too little is also bad; you run the risk of becoming a little bit stale. I wanted to make sure I passed the baton before I got to that point. We had a candidate ready to go, and, therefore, I think it was time for me to go.

How have the global electronics business and design evolved since you joined Avnet three and a half decades ago?

A Dramatically. When I joined, the role of distributors was primarily to stock things and sell them to a broad base of customers that the suppliers couldn't economically serve directly. Oftentimes, we'd hand out [catalogs] to buyers, not even the engineers.

Then the microprocessor was introduced, and with it came the introduction of [distributor] registrations. That process brought field application engineers into the distribution industry.

At that point in time, distributors had to make a choice between staying in the traditional, wholesaler space or moving into the technical distribution space, which meant an investment in people and training and certification.

When ASICs came along, some of us got into the business of designing ASICs for customers who preferred to outsource that activity. Then FPGAs came along and were getting larger in density. Some customers started turning to us for FPGA design, too.

From there, we evolved into doing reference designs of entire systems. So [we've gone from] traditional, wholesale distribution to full-out design capabilities with design engineers. It's been nothing less than dramatic in terms of the role that distribution has evolved into from a technical-support perspective.

What types of opportunities do you see ahead for the overall electronics business and design engineers, and how will design-chain efforts fit into that?

A I think about all of the devices that increase human productivity and efficiency. I think about medical and what's happening there. The defense industry, of course, with smart missiles and unmanned aircraft—this is Buck Rogers science-fiction stuff going on in the real world. [Then there's] perhaps the fastest growing market: leisure or recreation that enhances the quality of people's lives.

All of that is manifesting itself in two primary ways. One is mobility; it's unbelievable how much we can do with portable and mobile products. The other is embedded. As the cost of electronics has gone down and pressures like product life cycles have decreased, customers want to buy higher levels of integration and are buying embedded products.

As long as Moore's Law stays intact, we have this ever-accelerating rate of change in the world. The economy continues to become more and more of a global event, where we bring literally billions of consumers into the marketplace who historically were excluded due to economic disparities. For a company that can support the notion of design anywhere, build anywhere, there's an exciting future ahead.

What do you wish someone had told you 35 years ago?

A Make a top priority the people side of the equation, as opposed to the strategy, operations, and financial side. And the [idea that] "By the way, that starts with you." One of the most important things you can do for your career is to be self-aware.

And when you keep score—yes, revenue and margins are important—make sure you pay attention to return on capital. That's what really matters.

In terms of advice, develop your own explicit personal values, what is important to you personally. In the course of a career, there are going to be all sorts of opportunities and challenges that come at you. Having explicit core values, and staying true to them, really helps in making those decisions.

Focus on balance. There's career, and there's personal. Careers are marathons, not sprints. If you sprint to a job and achieve it and end up with a messed-up personal life, you haven't achieved success. The definition of success, from my perspective, is happiness.

My last two points are on the fuzzy side. Do the right thing, always—not just when it's convenient. And, last, enjoy the journey. We put a large portion of our lives into our careers. If you add up the hours, it's a little frightening. If those hours are going into something you are not enjoying, then at the end of the day you're going to be unhappy.

—interview conducted and edited by Suzanne Deffree

BY HOWARD JOHNSON, PhD

Nickel matters

Jason Mills at Sandvine Inc was testing a complex system involving a long backplane with daughtercards at each end. He was running a number of 3.125-Gbit/sec XAUI signals through the system. The trace configuration for each signal comprised approximately 5 in. total of inner-layer routing divided between the two daughtercards, plus 20 in. of outer-layer routing on the backplane. The 5.5-mil differential microstrip traces on the backplane were built on an ordinary FR-4 substrate using a process called SMOG (solder mask over gold).

The SMOG process passivates the microstrip traces, covering them with an inert coating through which corrosion will not penetrate and to which lead-free solder will readily adhere. Pure gold seems ideal for that purpose. It is impervious to corrosion and bonds well to lead-free solder. A microscopically thin layer of gold, only 5 microinches thick, should be all that is necessary. That is the good news.

The bad news is that layers of gold and copper placed in direct contact slowly diffuse into one another. Eventually, the thin layer of gold diffuses so deeply into the copper that it no longer provides a passivating effect. Shortly after that, the underlying copper corrodes.

A barrier layer of nickel 120 microinches thick, placed between the gold and copper layers, stops the diffusion. That is the SMOG idea. The SMOG system starts with an ordinary copper microstrip trace several hundred microinches thick, plates it with 120 microinches of nickel, and then covers that with 5 microinches of gold. The process keeps your metallurgists happy, but what about signal quality?

As explained in my article "Nickel-Plated Traces" (http://bit.ly/QzpcuX), nickel plating substantially increases the high-frequency resistance of a PCB trace. It lengthens the step response of the trace, exacerbating both intersymbol interference and jitter. Microwave engineers have known this for decades.

When Jason got his first boards back and observed poor eye quality, he quickly surmised that the nickel might be hurting him. That's a good guess, but frankly, a lot of people might have guessed that. Jason's next move is what distinguishes him from other engineers. He wanted a way to test his hypothesis, directly and convincingly, in a few minutes, without respinning the boards. Here's what he did.

First, he measured the system eye pattern. Then, he physically sanded the board, using #220-grit sandpaper, completely removing all of the solder mask, gold, and nickel covering the long, exposed sections of the microstrip traces on his backplane, and reshot the eye pattern (**figures 1** and **2**). Brilliant.

Sanding removes solder mask and also thins the traces; both effects incrementally raise the differential trace impedance. Sanding also introduces a considerable amount of surface roughness. Despite those disadvantages, Jason's sanded traces show markedly better performance than the original SMOG trace.

In the final system, Jason used a solder-mask over bare-copper process to cover the long copper microstrips and eliminate nickel from those regions. He then treated all of the exposed soldering pads with a different process to make them solder friendly. **EDN**

Howard Johnson of Signal Consulting Inc frequently conducts technical workshops for digital engineers at Oxford University and worldwide. Visit www.sigcon.com, or e-mail him at howie03@sigcon.com.

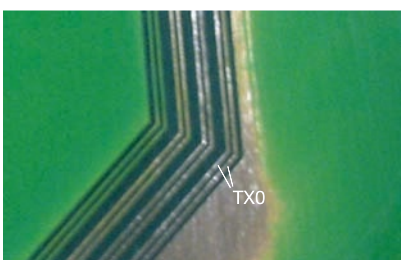
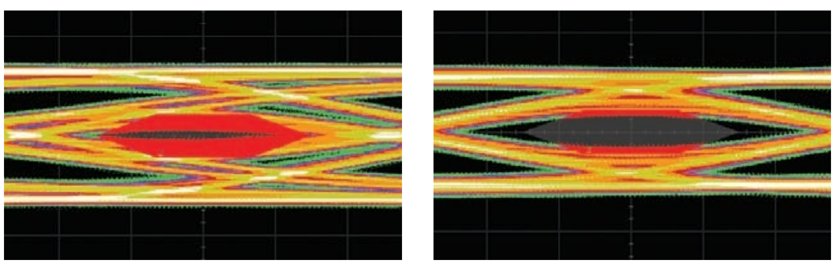


Figure 1 Sanding the full length of each trace removes all of the solder mask and nickel plating.



(a) (b)

Figure 2 The sanded trace exhibits a better eye with less jitter and a larger eye opening; shown are eye diagrams created before (a) and after (b) sanding.

BY BONNIE BAKER

Collecting light power: voltaic or conductive?

Photovoltaic versus photoconductive terminology for photodetecting circuits has always been confusing for me. My research shows that others share my confusion.

In photoconductive mode, a photodetector has a consistent voltage impressed across the anode and cathode of the diode. The constant voltage can range from approximately 0V (less than 20 mV) to hundreds of negative volts. Higher negative voltages across the photodetector decrease the diode's parasitic capacitance, which in turn increases the system's frequency response. At a given reverse bias voltage, the magnitude of the parasitic capacitance remains constant.

The trade-off for this improvement in capacitance is an increase in the dark current through the diode. The configuration in **Figure 1a** creates a very linear response in terms of the irradiance of the light source and the resulting magnitude of the photodiode current (I_{PH}).

A photovoltaic diode (or solar cell) generates electrical power from solar radiation. The solar cell converts solar rays into a direct current (**Figure 1b**) that forward biases the diode and creates an output voltage. In this configuration, the output voltage versus the photocurrent is nearly logarithmic (**Figure 2**), as would be the case with any diode. This logarithmic response gradually gets more linear as the load resistance decreases.

Three basic types of photodetectors are available today: PDs (photodiodes), PIN-PDs (positive-intrinsic-negative PDs), and APDs (avalanche PDs). A PD is an ordinary PN-junction diode. The PIN-PD has an intrinsic (undoped) region between the N- and P-doped regions. This feature provides a thicker depletion area, leading to lower capacitance and wider bandwidths. APD designs support high reverse bias voltages (tens to hundreds of volts). For best results, bring the reverse bias voltage to just below the diode's breakdown voltage, creating an amplification factor. An APD can achieve very high detection bandwidths.

This is just a short overview of uses for the many types of photodetectors available in the market. I imagine that you have had some experience with this topic. If you've used a photodiode in a system, I'd love to hear about it. Experts are welcome to offer additional comments or suggestions. EDN

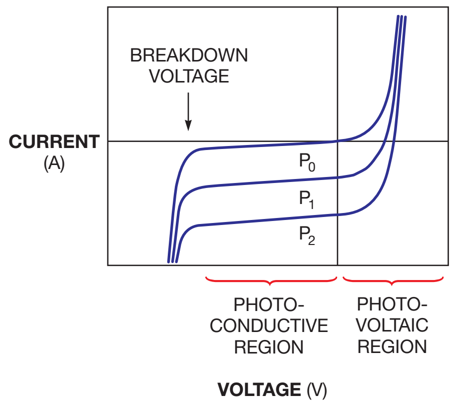


Figure 2 Photoconductive and photovoltaic sensing cells exhibit the same behavior. Characteristic IV curves of a photodiode for photoconductive and photovoltaic modes of operation are shown; P_0, P_1, and P_2 represent different light levels.

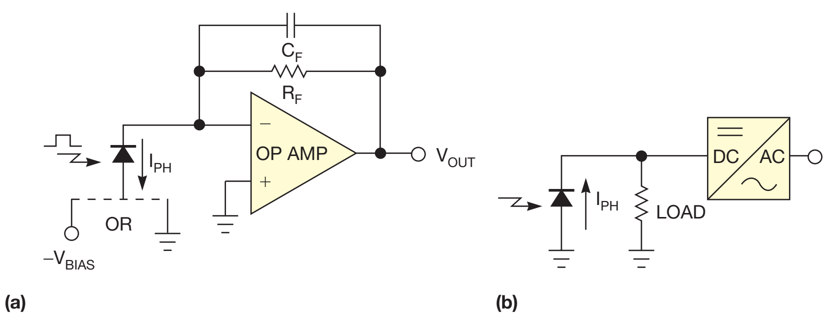


Figure 1 A photoconductive circuit, with zero bias voltage or a reverse bias voltage (a), uses a transimpedance amplifier circuit to convert the light-generated current to voltage. A photovoltaic circuit, with no voltage impressed across the photodetector (b), generates its own voltage and current because of light hitting the photosensor element.

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Bonnie Baker is a senior applications engineer at Texas Instruments.

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PillCam exposes your innards

Anyone who's ever had to endure an endoscopy or colonoscopy knows that those tests can be, so to speak, a bitter pill to swallow. Given Imaging's PillCam Colon 2 ingestible capsule offers a friendlier alternative for getting a good look at your innards, from stomach to lower intestine, with less chance of mortality. Now *there's* an incentive.

A bit larger than your average vitamin, without the option to blend it in a shake, the PillCam Colon 2 is a classic exercise in low-power wireless system design, with advanced imaging and novel packaging techniques. To use the device, the subject swallows the capsule. The images it captures are sent to a sensor array, which connects to a data recorder and is worn strapped to the subject's abdomen. The subject returns the recorder to the doctor the next day and excretes the use-once PillCam within a couple of days. (FYI—or perhaps this is TMI—subjects have been known to retrieve and save their capsules for posterity.)

Just to show how smart Given Imaging really is, the PillCam Colon 2 developers didn't do the wireless design themselves. Other companies had tried that but eventually turned to the experts; see "FitBit blends wireless, MCUs, and MEMS with online interface" (http://bit.ly/QJEBrf). Instead, Given Imaging consulted the experts at Zarlink Semiconductor, now part of Microsemi Corp. Microsemi, in turn, worked closely with the image-sensor experts at Aptina Imaging Corp to develop the device and optimize it to the nth degree.

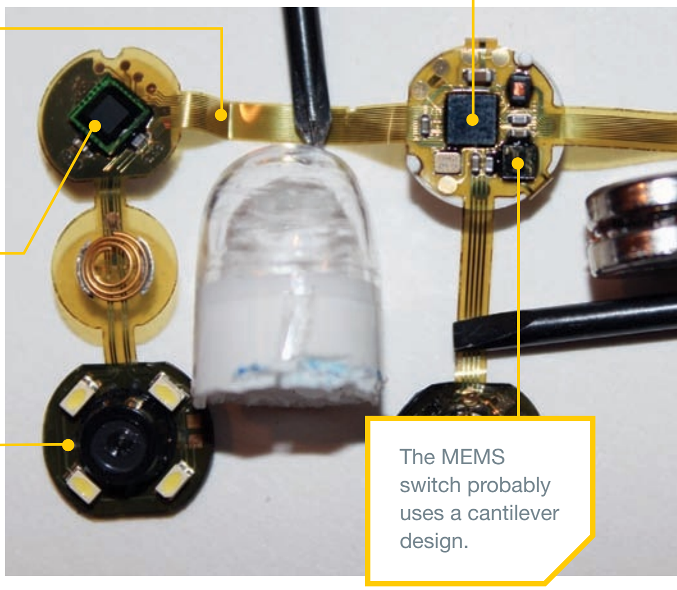
The Colon 2 received the CE Mark in September 2009 and is commercially available in Canada, Europe, Latin America, and parts of Asia. Given Imaging has submitted the product for FDA approval.

The PillCam Colon 2 measures 11×26 mm and weighs less than 4g. The four LEDs on each end of the pill flash alternately and allow images to be taken looking forward and behind, deep into the colon mucosa, as the capsule tumbles. There is one Aptina CMOS image sensor at the center of each end of the PillCam.

When the unit is closed, two magnetic strips on the lid activate a MEMS switch to keep the PillCam in the off state. The PillCam activates when the lid is opened.

Power derives from two Energizer 399 1.55V, 54-mAhr silver-oxide coin cells, each weighing 0.8g and taking up a third of the overall volume.

The custom chip includes a proprietary Microsemi (Zarlink) fully integrated, third-generation sub-GHz ISM-band radio combined with a custom, 8-bit Harvard-architecture control circuit. The radio link is asymmetric: Tens of kbits/sec down-channel allow device control (frame rate, power use, etc.); 5 Mbits/sec up-channel enable 28-fps, full-color image transfer. The range is 1 to 2 feet in the body and tens of meters line of sight.



The polyimide flex circuit allows the device to be fully assembled flat using standard manufacturing assembly, then folded around the battery in the center of the capsule.

This is one of the unit's two Aptina MT9S526 5.6-μm CMOS image sensors, capable of 4 to 5 fps in a 1/6-in. optical format.

Here's one of the two lenses, surrounded by four white LEDs.

The MEMS switch probably uses a cantilever design.

Modeling the MEMS gyroscope

Knowing how this ubiquitous device works is essential in the age of model-based design.

By Kevin C Craig, PhD

The MEMS gyroscope affects so much of our everyday lives, in particular in consumer electronics, that engineers now design systems that include MEMS gyros as essential components. In this age of model-based design, it is critical to know how this device works and how to model it.

A gyroscope measures the angular velocity of a body about a specified axis of rotation. A MEMS gyro, however, is not the bulky, spinning-disk gyroscope we see in science museums. **Figure 1** shows a physical model of a typical MEMS vibratory gyroscope designed to measure the angular velocity of the body about the *z* axis of the ground reference frame.

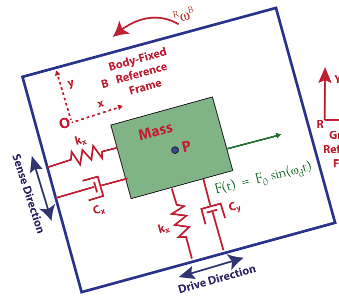


Figure 1 This physical model shows a typical MEMS vibratory gyroscope designed to measure the angular velocity of the body about the z axis of the ground reference frame. The main principle of MEMS gyros is the transfer of energy between two modes of vibration through the Coriolis acceleration.

The main principle of MEMS gyroscopes is the transfer of energy between two modes of vibration—the drive and the sense modes—through the Coriolis acceleration. How does this happen, and what are the challenges? Developing a mathematical model for the physical model shown in **Figure 1** will answer those questions; every engineer thus needs to know how to do so.

It all starts with a fundamental kinematic relationship specifying the absolute acceleration of the mass translating in the body, whose rotation rate we want to know. This is shown with a matrix relationship between the ground and body-fixed reference frames, here assumed to have a common origin:

$$\begin{bmatrix}\hat{i}\\ \hat{j}\\ \hat{k}\end{bmatrix}=\begin{bmatrix}\cos\theta & \sin\theta & 0\\ -\sin\theta & \cos\theta & 0\\ 0 & 0 & 1\end{bmatrix}\begin{bmatrix}\hat{I}\\ \hat{J}\\ \hat{K}\end{bmatrix}$$

$$\overset{R\to P}{a} = \overset{R\to O}{a} + \left[\overset{R\to B}{\omega}\times\left(\overset{R\to B}{\omega}\times\overset{\to OP}{r}\right)\right] + \left[\overset{R\to B}{\alpha}\times\overset{\to OP}{r}\right] + \overset{B\to P}{a} + 2\left[\overset{R\to B}{\omega}\times\overset{B\to P}{v}\right]$$

$$\overset{R\to O}{a}=0 \qquad \overset{R\to B}{\omega}=\omega\hat{k} \qquad \overset{\to OP}{r}=x\hat{i}+y\hat{j}$$

$$\overset{R\to P}{a}=\left(\ddot{x}-\alpha y-2\omega\dot{y}-\omega^2 x\right)\hat{i}+\left(\ddot{y}+\alpha x+2\omega\dot{x}-\omega^2 y\right)\hat{j} \qquad \overset{R\to B}{\alpha}=\alpha\hat{k} \qquad \overset{B\to P}{v}=\dot{x}\hat{i}+\dot{y}\hat{j}$$

We next apply Newton's Second Law to the mass in both the x and y directions, resulting in two coupled differential **equations** of motion, shown below, where $F_0\sin(\omega_d t)$ is the driving force. Note the Coriolis acceleration terms, $2\omega\dot{x}$ and $2\omega\dot{y}$:

$$-k_x x-c_x\dot{x}+F_0\sin(\omega_d t)=m\left(\ddot{x}-\alpha y-2\omega\dot{y}-\omega^2 x\right)$$
$$-k_y y-c_y\dot{y}=m\left(\ddot{y}+\alpha x+2\omega\dot{x}-\omega^2 y\right)$$

Assume a constant angular speed ω, and since ω is usually much smaller than the natural frequencies of the system, neglect terms involving ω^2. The sense-mode response y is much smaller than the drive-mode motion x, so the term $2\omega\dot{y}$ can be dropped. The resulting **equations** are

$$m\ddot{x}+k_x x+c_x\dot{x}=F_0\sin(\omega_d t)$$
$$m\ddot{y}+k_y y+c_y\dot{y}=-2m\omega\dot{x}$$

The first **equation** can be solved independently. You can then substitute its solution into the second **equation**, which can be solved for the sense-mode response y. The resulting amplitudes of motion X and Y are given below; Y/ω is the gyroscope sensitivity:

$$X=(F_0/m)\omega_x^2\frac{1}{\sqrt{(1-r_x^2)^2+(2\zeta_x r_x)^2}} \qquad \omega_x=\sqrt{\frac{k_x}{m}} \quad \zeta_x=\frac{c_x}{2m\omega_x} \quad r_x=\frac{\omega_d}{\omega_x}$$

$$\frac{Y}{\omega}=\left(\frac{2m\,\omega_d X}{k_y}\right)\frac{1}{\sqrt{(1-r_y^2)^2+(2\zeta_y r_y)^2}} \qquad \omega_y=\sqrt{\frac{k_y}{m}} \quad \zeta_y=\frac{c_y}{2m\omega_y} \quad r_y=\frac{\omega_d}{\omega_y}$$

The sensitivity is proportional to the oscillating mass, which puts some restrictions on the level of miniaturization that can be achieved. To achieve maximum sensitivity, resonance in both modes is desirable; that is, $\omega_d=\omega_x=\omega_y$. The expression for the gyroscope sensitivity then becomes

$$\frac{Y}{\omega}=\frac{2m\,\omega_d F_0 Q_x Q_y}{k_x k_y} \qquad Q_x=\frac{1}{2\zeta_x} \qquad Q_y=\frac{1}{2\zeta_y}$$

Q_x and Q_y are the quality factors of the drive and sense modes, respectively. High quality factors are desirable to improve sensitivity.

All engineers should count the ability to do this kind of work as a critical element of their skill set; it is what differentiates model-based design engineers in the 21st century. EDN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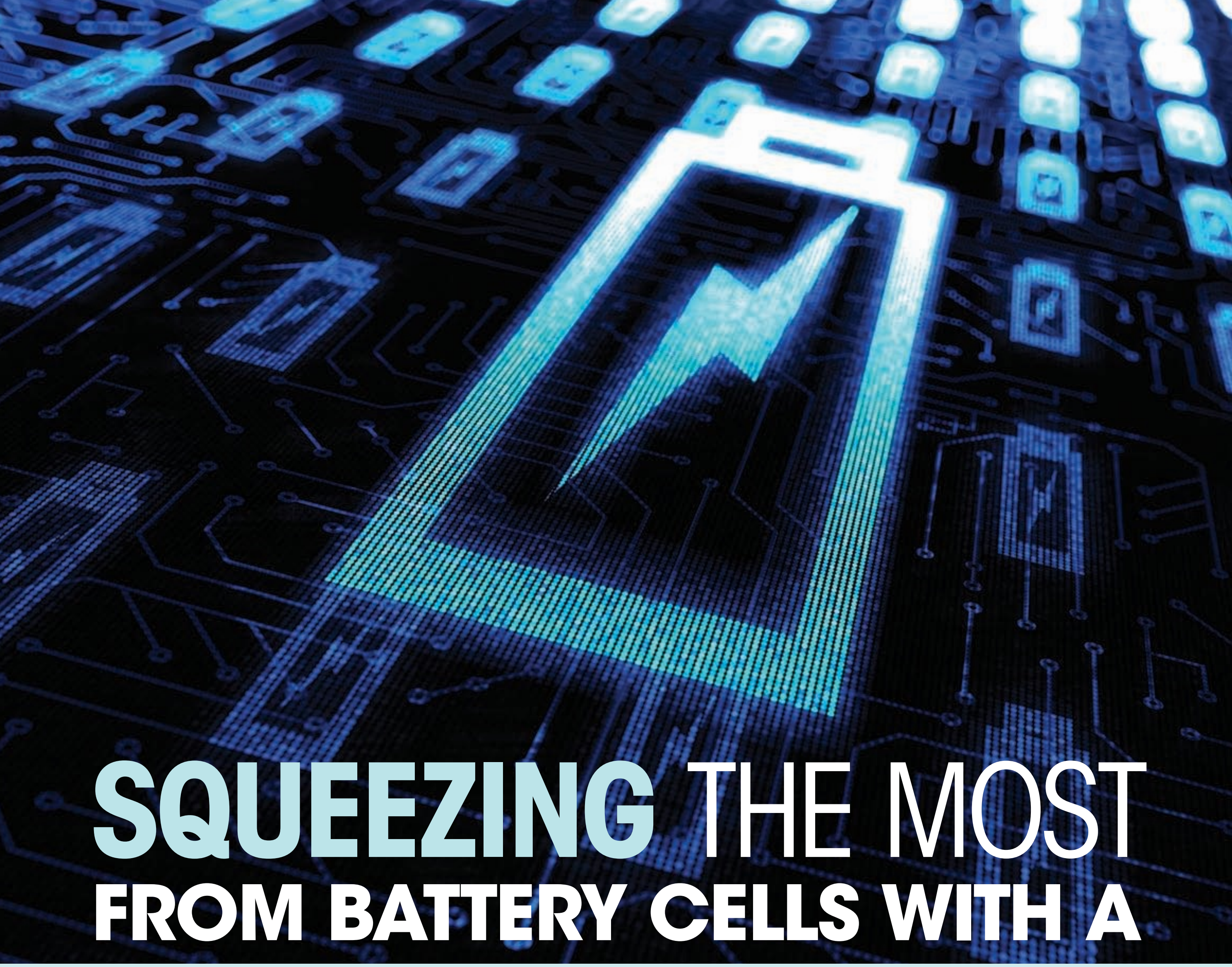

IMAGE: ISTOCK

SQUEEZING THE MOST FROM BATTERY CELLS WITH A SWITCHED-MODE PUMP

MANY OF TODAY'S MICROCONTROLLER AND SOC ARCHITECTURES INCLUDE AN ON-CHIP BOOST CONVERTER THAT CAN ACCEPT AN INPUT VOLTAGE SUPPLIED BY A BATTERY OR OTHER SOURCE AND PRODUCE A SELECTABLE OUTPUT VOLTAGE THAT EXCEEDS THE INPUT.

BY GAUTAM DAS G • CYPRESS SEMICONDUCTOR CORP

Achieving long battery life in portable applications is a challenge. Designers working to optimize power consumption must consider such factors as power-supply design, component selection, efficient firmware structure (if any), management of multiple low-power operating modes, and PCB-layout design. Many of today's microcontroller and SOC architectures include an on-chip boost converter that can accept an input voltage supplied by a battery or other source and produce a selectable output voltage that exceeds the input. This article explores the use of an SMP (switched-mode pump) as a boost converter to solve system-power issues.

The typical operating voltage required for any microcontroller is at least 3.3V, though 1.8V is sufficient for the core in any microcontroller to be functional. Because an AA or AAA battery will deliver 1.3 to 1.5V when fully charged, systems need at least two battery cells to operate. As the battery decay gradually falls below 0.9V, it becomes impossible to operate the system even with two batteries.

With the use of a boost converter, however, a microcontroller can operate on a single battery cell that has been boosted to deliver 1.8V or higher. The boost converter not only lets systems operate from just one battery cell but also lets them sustain operation even when the voltage drops to 0.5V. Alternatively, solar-cell-powered devices—typically consumer-oriented products that require a small form factor—can use boost conversion to enable operation from a single 0.5V solar cell rather than the three 0.5V cells that otherwise would be required. Developers can also protect system data when voltages drop too low to boost by employing such techniques as low-power mode with RAM retention, which lets a user replace the battery and resume operation with no interruption.

AT A GLANCE

- The use of a boost converter can enable a microcontroller to operate on a single battery cell or a 0.5V solar cell.
- An SMP (switched-mode pump) can also boost battery voltage to access stored capacity that the system would otherwise be unable to extract.
- The efficiency of an SMP is limited by the losses in its passive components.
- An integrated SMP can enable a microcontroller to supply subsystems such as RF ICs with the required higher voltage.

SQUEEZING THE BATTERY

Figure 1 shows the discharge graph of an AA battery of 2500-mAhr capacity. Consider an application comprising a controller or SOC that operates at 1.8V and consumes an average current of 10 mA. The battery is expected to last for 2500 mAhr/10 mA, or 250 hours. As the graph shows, once the battery voltage drops to 0.9V, it has discharged about 2200 mAhr. Beyond this point, even with two batteries (assuming the microcontroller works at 1.8V), the features available in the controller may not operate normally. That means the remaining 300 mAhr, or more than 10%, of battery power cannot be used.

A switched-mode pump, if available on the microcontroller, can boost the battery voltage to an appropriate usable voltage. Microcontroller manufacturers provide an option to select this usable voltage, allowing the voltage to be boosted to 1.8V or higher for powering the application, even when battery voltage drops below 1V. The system thus is able to extract a part of the remaining 300-mAhr capacity still available in the battery cell.

Below a certain input voltage, however, the boost circuitry may not be able to operate, thus limiting the system from extracting all of the remnant power. Note that the battery should be able to source enough current for the boost to function. The input current to the boost circuitry is a function of the input battery voltage and the output boosted voltage. This current increases as the difference between the input voltage and the output voltage increases—that is, as the battery voltage drops.

For example, consider an SMP being used to boost to a constant 3V output. In any system, the power is always constant—that is, output power is equal to the input power. The output power from a boost converter is slightly lower than the input power because of losses in the components used for conversion, but for our purposes let us assume an ideal boost system, with no loss. With the initial, 1.5V battery input boosted to 3V, in order to supply 50 mA to a load, the input current would be (3×50)/1.5=100 mA. Once the battery voltage drops to 1V, to maintain the output voltage, the required input current would increase (power is constant); the input current in this case would be (3×50)/1=150 mA. Thus, the boost converter provides a constant voltage-output regulation.

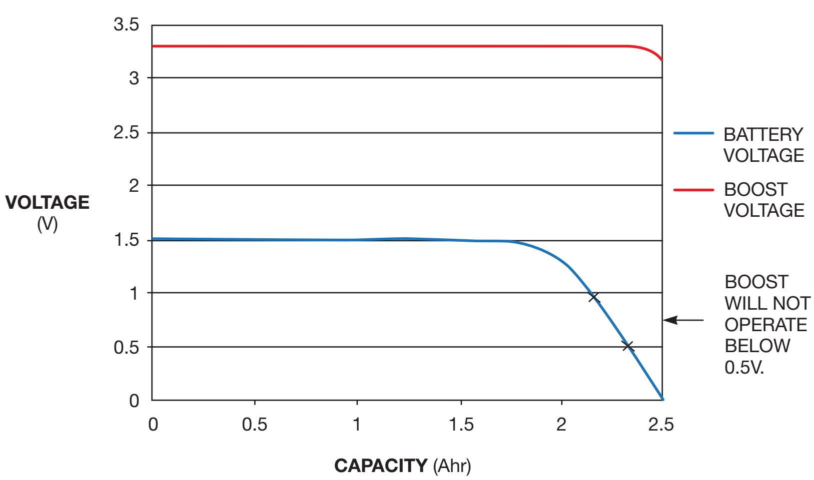

Figure 1 This discharge graph of an AA battery with 2500-mAhr capacity indicates that when the battery voltage drops to 0.9V, approximately 2200 mAhr has been discharged.

ARCHITECTURE

Figure 2 shows the architecture of an SMP boost converter in an SOC compared with an external boost-converter circuit. The boost converter shown in **Figure 2a** has two phases: a storage phase, during which the switch is on, and a discharge phase, during which the switch is off. When the switch is conducting, the inductor stores energy from the battery in the form of a magnetic field. When the switch is opened, the inductor current continues to flow in the same direction, causing the voltage at node V_{SMP} to "fly back" to a voltage higher than the capacitor voltage. This action triggers the diode to begin conducting, which in turn allows the charge

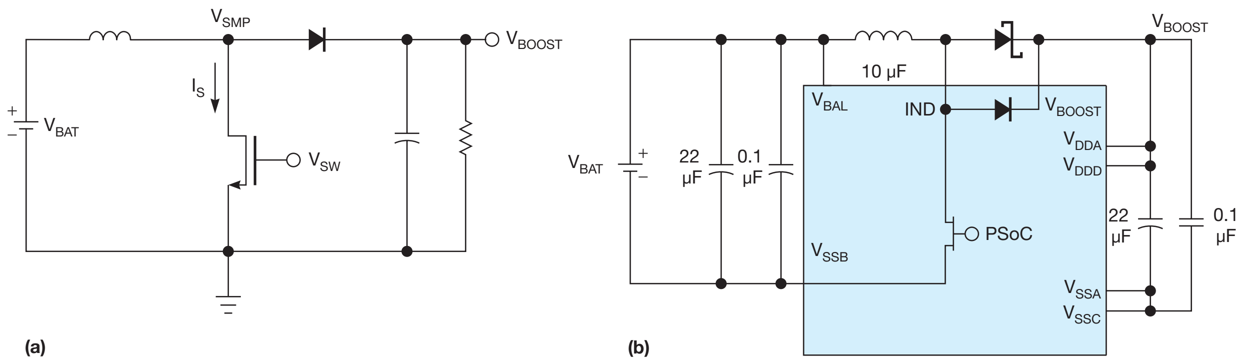

Figure 2 A boost converter circuit (a) is shown in comparison with the switched-mode pump in a microcontroller (b). V_{BAT} is the input battery voltage; V_{SW} is the switching waveform, which is a PWM with a 50% duty cycle.

stored in the inductor to be transferred into the filter capacitor. A PWM, V_{SW}, turns the switch on and off.

In a microcontroller (**Figure 2b**), an on-chip generation unit makes this switching waveform available. The protection diode can be internal to the microcontroller chip or can be connected externally. The only components a developer has to connect are the inductor coil and filter capacitors. In the SOC shown in **Figure 2b**, V_{DDA} and V_{DDD} are the chip supply voltage.

DESIGN TIPS

High efficiency is desirable in low-power, low-input-voltage SMPs used in embedded solutions, which impose space and cost constraints, but switch and passive-component losses can limit efficiency. The MOSFET switch, which is internal to the controller, contributes to ohmic losses as well as switching losses; the higher the switching frequency, the greater the switching losses. The impedance of this switch is pretty much determined at the design stage of the chip. The inductor losses are similar to those of the switch. The designer must choose the switching frequency appropriately to optimize power and must choose an inductor based on the switching frequency.

The output capacitor's ESR (equivalent series resistance) can cause significant ripple. If aluminum capacitors are chosen to reduce cost, a ceramic capacitor should also be connected in parallel to minimize ripple. The size of the capacitor used determines the hold time of the output. Schottky diodes are recommended because they have a low forward voltage and fast switching speed, though the Schottky diode's forward drop and its own impedance account for some loss. The current rating of the diode should be greater than twice the peak load current.

The SMP shown in **Figure 2b** has an internal diode. In microcontrollers, however, this diode is mimicked using a MOSFET switch, which is operated in synchronization with the SMP. Having an external Schottky diode results in higher power loss, attributed to the diode forward drop, which typically would be around 0.4V. The internal synchronous FET has lower drop (0.1V) and thus minimizes losses, resulting in better efficiency.

The nature of the load also affects the efficiency of the SMP; efficiency is reduced if the load is not a constant load.

The layout design of a low-input-voltage SMP circuit must be done with extreme care. Consider a boost converter that starts up at 0.5V, as is the case in Cypress Semiconductor's PSoC3 programmable system on chip. Let us assume that the boost output is expected to be 3V with 50-mA current capability. With 100% efficiency, the input current is expected to be ((3×50)/0.5)=300 mA. With 300-mA current being pumped in, a PCB trace of 1Ω can easily produce a voltage drop of 0.3V. Though the actual input voltage is about 0.5V, what appears at the boost input would be 0.2V. As a result, the SMP would not start at 0.5V input. The board designer can avoid this situation by using wider traces of shorter length, placing the components in a way that keeps the conduction paths short.

Another design issue is the emissions that result from the switching current into the SMP. When the inductor stores charge, the input current is higher. In addition, this current switches between two extremes as the inductor stores and discharges power.

Consider a scenario in which 0.5V is being boosted to about 3V; assume the load draws about 50 mA. The input current in this case for an ideal SMP would be 300 mA. If the converter is not ideal, this current will be even higher. If there are any long traces through which this current flows, electromagnetic emissions can result that affect the operation of nearby circuits. If there are any analog components nearby, for example, their performance might not be acceptable. To avoid this situation, isolate the switching path from the other sensitive components by using guard traces that are connected to ground.

BOOST-CONVERTER FEATURES

The boost converter may also be used in any system that requires a higher operating voltage than the supply provides. One example would be driving a 5V LCD in a 3.3V system.

Another example would be an application that uses a controller and an RF chip for wireless communication

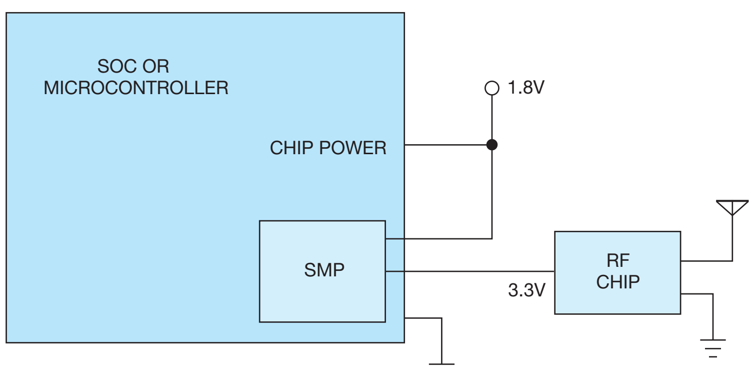

Figure 3 In this example of a controller and an RF chip for wireless communications, the RF chip needs 3.3V for its operation, whereas 1.8V is sufficient for the controller.

(**Figure 3**). The RF chip may require 3.3V for its operation, whereas 1.8V might be sufficient for the controller. In this scenario, an input-regulated voltage can power the controller; at the same time, the SMP available on the controller can boost the input voltage to 3.3V and supply the RF chip. The SMP on a controller thus can be used in applications that require multiple supplies.

A number of manufacturers provide SOCs with on-chip SMPs that offer unique features. Cypress Semiconductor's PSoC architecture, for example, has an SMP in addition to other resources, such as precision programmable analog and digital components. The boost converter on the SOC can be operated in either active or standby mode. Active mode is the normal mode of operation, wherein the boost regulator actively generates a regulated output voltage from the battery input. In standby mode, most boost functions are disabled to reduce the boost circuit's power. The converter can be configured to provide low-power, low-current regulation in standby mode. An external, 32-kHz crystal can be used to generate inductor boost pulses on the rising and falling edges of the internal clock when the output voltage is less than the programmed value; this mode is called ATM (automatic thump mode).

The boost typically draws 200 μA in active mode and 12 μA in standby mode. The switching frequency can be set to 100 kHz, 400 kHz, 2 MHz, or 32 kHz to optimize efficiency and component cost. The 100-kHz, 400-kHz, and 2-MHz switching frequencies are generated using oscillators internal to the boost-converter block. When the 32-kHz switching frequency is selected, the clock is derived from the 32-kHz external crystal oscillator. The 32-kHz external clock is primarily intended for boost standby mode.

An on-chip SMP in microcontrollers and SOCs is helpful in powering low-power embedded applications. Improving a battery's efficiency helps improve its endurance, resulting in fewer discarded batteries. SMPs also encourage designers to develop solar-cell-powered systems.EDN

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AUTHOR'S BIOGRAPHY

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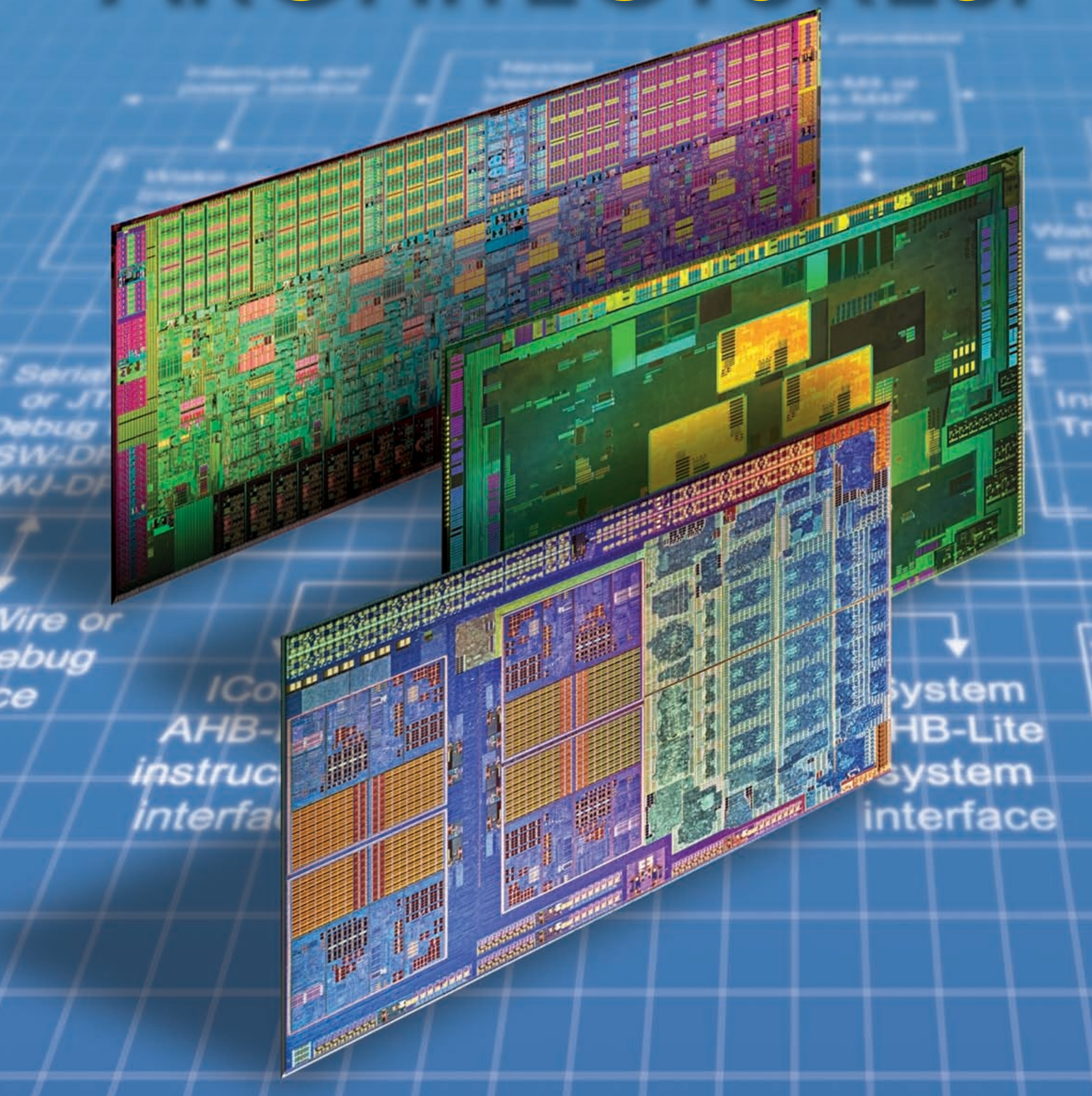
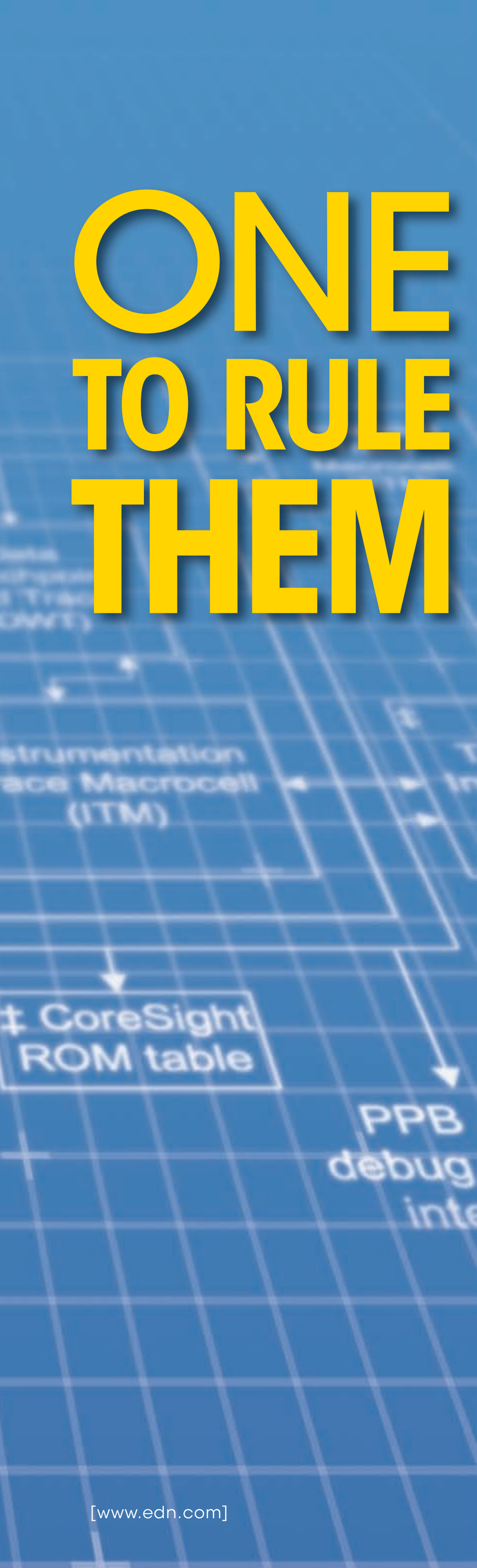
PROCESSOR ARCHITECTURES:





ONE TO RULE THEM ALL?

CAN A SINGLE PROCESSOR ARCHITECTURE DO IT ALL, AND IF SO, WOULD IT BE A GOOD IDEA?

BY ROBERT CRAVOTTA • EMBEDDED INSIGHTS INC

Much like Middle-earth in *The Lord of the Rings*, the ecosystem for embedded and computing systems is home to a diverse population. Instead of elves, dwarves, Hobbits, and humans, all manner of processor architectures inhabit the compute and embedded-processing ecosystem. The various microprocessors, digital signal processors, and microcontrollers implement different optimization choices to meet system designers' myriad design requirements.

That analogy occurred to me as I read a number of recent articles and public online discussions. Collectively, they ask two questions that implicitly share the same underlying architecture: Are 8-bit processors dying, and is ARM winning the processor war? The articles and discussions all suggest that the ARM architecture will be the one to put the final nail in the coffin of smaller-bit-width microcontrollers and will possibly even crowd out other 32-bit microprocessors in other application spaces. In this rapidly evolving ecosystem, can the ARM architecture become the one to rule them all?

The analogy serves only as an illustration of the common, implied architectural theme running through these questions and the accompanying discussions; it is not meant to be a statement about the discussed processor architectures or about the ecosystem companies that support them. At least for me, however, the analogy provides a visual image that captures the almost palpable expectation that a single processor architecture might finally deal the death blow to 8- and 16-bit architectures one day soon, as well as possibly dominate traditional applications for 32-bit and larger microprocessors.

Is such a consolidation of processing architectures possible? Is it even desirable?

Let's begin this exercise by stipulating that with regard to cost, workload capacity, and energy consumption, a specific 32-bit processor has achieved or surpassed parity with a specific 8-bit processor that is being used for a specifically defined workload. The point of this precisely worded stipulation, beyond avoiding data-sheet debates, is to emphasize that the replacement of any processor with another is performed on a case-by-case basis that distinguishes between explicit alternatives in the context of an explicit workload (expected or already implemented). When the new alternative is superior to the incumbent implementation, there is an opportunity for a migration to the new alternative.

Migrating a workload to an alternative device as part of the life cycle of both the workload and the available processing options, however, is not the same as migrating to an alternative expressly because the incumbent processor width or architectural implementation has become obsolete.

As an example, consider the analogous, long-debated statement that FPGAs will drive DSPs to obsolescence. It has been repeatedly demonstrated that FPGAs can perform arbitrarily wide signal-processing tasks more quickly and efficiently than dedicated DSPs. For a given workload, however, a specific processor that incorporates the optimal type and number of execution units to implement that specific workload can negate an FPGA's performance and efficiency advantage.

In fact, a realistic life-cycle scenario for contemporary signal-processing workloads could initially see a workload

AT A GLANCE

- The ARM 32-bit architecture is currently the strongest candidate for obsoleting 8-bit architectures.
- As 32-bit processors rely on smaller size fabrication nodes, the opportunity for price and energy parity improves.
- Each processor size and type best serves a different problem domain, which justifies the expenditure to make targeted best-in-class devices and software.
- Innovation can arise in any direction—possibly even including going smaller to go faster.
- A single development approach may limit the types of new opportunities that can be identified and solved.

Protecting IGBTs with Avago Optical Isolation Amplifiers

Introduction

Insulated-gate bipolar transistors (IGBTs) can fail when subjected to overloads and overvoltages. Isolation amplifiers (iso-amps) can respond quickly to over-current and overload conditions when used on the output phases and the DC bus.

A typical block diagram of a power converter in an AC motor drivet consists of an inverter that converts the DC bus voltage to AC power at a variable frequency to drive the motor. IGBTs are expensive power switches that form the heart of the inverter. These power devices must operate at a high frequency and must be able to withstand high voltages.

Iso-amps such as the ACPL-C79A work with shunt resistors to accurately measure power converter current even in the presence of high switching noise. When used with a resistive divider, iso-amps work as precision voltage sensors to monitor the DC bus voltage. The microcontroller monitors the current and voltage information from the iso-amps and uses the data to calculate the feedback values and output signals needed to for fault management in the IGBTs and power converters.

Fault Protection

However, the IGBT protection must be such that its cost doesn't affect that of the motor drive system. IGBT gate drivers such as the ACPL-332J and current sensors with protection features can detect faults economically in this regard. They eliminate the need for separate detection and feedback components.

Over-current conditions in an IGBT can arise from a phase-to-phase short, a ground short or a shoot through. The shunt + iso-amp devices on the output phases and DC bus can, besides measuring current, detect such faults.

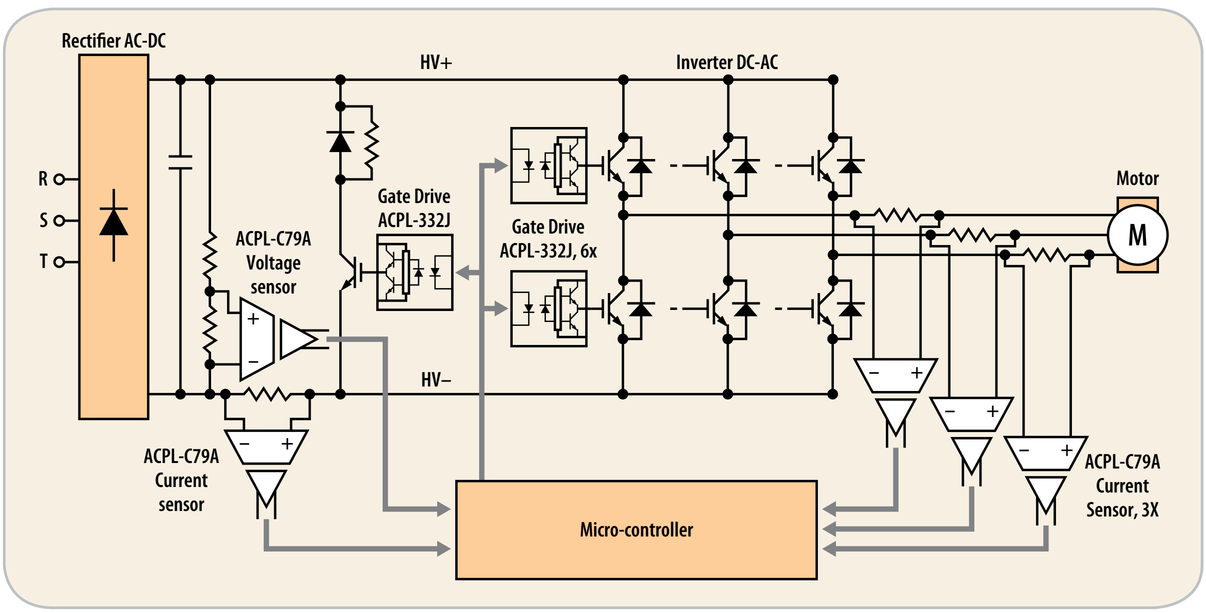
Typical IGBT short-circuit survival times are rated up to 10 µsec. So any protection must prevent this limit from being exceeded. Within 10 µsec, the circuit must detect the fault, notify the controller and complete the shutdown. Iso-amps use various methods to get these results.

For instance, the ACPL-C79A has a fast, 1.6 µsec response for a step input. That lets the iso-amp capture transients during short-circuits and overloads. The signal propagation delay from input to output at mid point is only 2 µsec, while it takes just 2.6 µsec for the output signal to catch up with input, reaching 90% of the final levels.

Another example is the HCPL-788J, which responds quickly to over-currents using a different approach. In addition to the signal output pin, it has a Fault pin that toggles quickly from High to Low level when over-current occurs. This iso-amp provides ±3% measurement accuracy.

In the fault feedback design, nuisance tripping can be an issue. This is a triggering of fault detection in the absence of any damaging fault condition. To avoid false triggering, the HCPL-788J employs a pulse discriminator that blanks out di/dt and dv/dt glitches. The advantage of this method is that

Figure 1: Block diagram of power converter in a motor drive



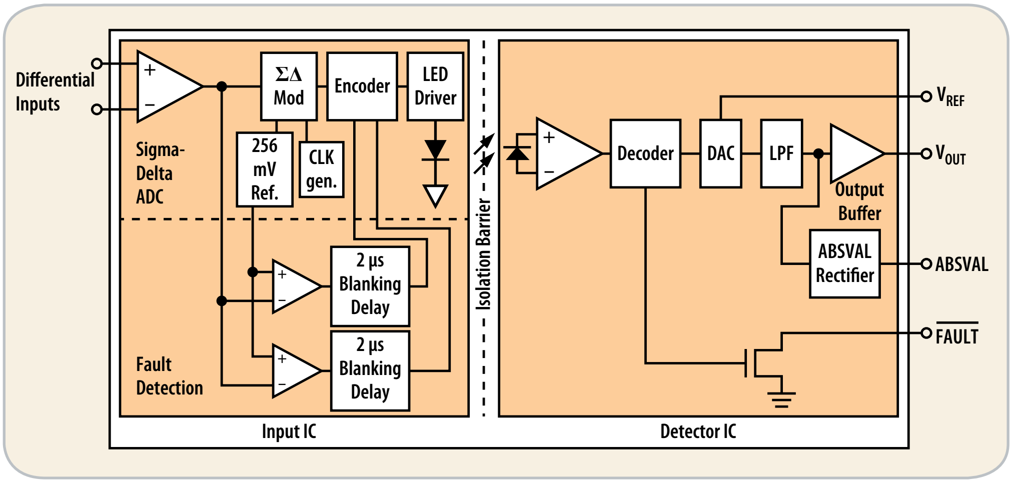


Figure 2: In the HCPL-788J iso-amp, the differential input voltage is digitally encoded by a sigma-delta A/D converter and then fed to the LED driver, which sends the data across the isolation barrier to a detector and D/A.

rejection is independent of amplitude, so the fault threshold can be set to low level without risking nuisance tripping.

The circuit that detects faults quickly contains two comparators in the Fault Detection block to detect the negative and positive fault thresholds. The switching threshold is equal to the sigma-delta modulator reference of 256 mV. The outputs of these comparators connect to blanking filters with a blanking period of 2 µsec and then go to the Encoder block.

To ensure speedy transmission of the fault status across the isolation boundary, two unique digital coding sequences represent the fault condition, one code for negative, the other for affirmative. Detection of a fault interrupts the normal data transfer through the optical channel and replaces the bit stream with the fault code. These two fault codes deviate significantly from the normal coding scheme, so the decoder on the detector side immediately recognizes the codes as a fault conditions.

The decoder needs about 1 µsec to detect and communicate the fault condition across the isolation boundary. The anti-aliasing filter adds a 400 nsec delay to give a propagation delay of 1.4 µsec. The delay between the fault event and the output fault signal is the sum of the propagation delay and the blanking period (2 µsec) for an overall 3.4 µsec fault detection time.

The Fault output pin allows fault signals from several devices to be wire-ORed together forming a single fault signal. This signal may then be used to directly disable the PWM inputs through the controller.

Overload Detection

An overload condition refers to a situation where the motor current exceeds the rated drive current, but without imminent danger of failure, as when the motor is mechanically overloaded or is stalling because of a bearing failure

Inverters usually have an overload rating. The time period of the allowable overload rating depends on the time it takes before overheating becomes an issue. A typical overload rating is 150% of nominal load for up to one minute.

The ACPL-C79A accepts full-scale input range of ±300 mV and the data sheet specifications are based on ±200 mV nominal input range. Designers can choose the overload threshold at or in between either of the two figures. Usually the measurement accuracy of the overload current is less stringent than that of the normal operating current. Here, setting the threshold near 300 mV is a good choice. This allows full use of the iso-amp's dynamic input range. However, a threshold set at 200 mV ensures accurate measurement of the overload current. Once the voltage levels are decided, the designer must choose appropriate sense-resistor value according to corresponding current level.

The HCPL-788J includes an additional feature, the ABSVAL output, which can be used to simplify the overload detection circuit. The ABSVAL circuit rectifies the output signal, providing an output proportional to the absolute level of the input signal. This output is also wire OR-able. When three sinusoidal motor phases are combined, the rectified output (ABSVAL) is essentially a DC signal representing the RMS motor current. This DC signal and a threshold comparator can indicate motor overloads before they can damage to the motor or drive.

Overvoltage Detection

The DC bus voltage must also be continuously controled. Under certain operating conditions, a motor can act as a generator, delivering a high voltage back into the DC bus through the inverter power devices and/or recovery diodes. This high voltage adds to the DC bus voltage and puts a very high surge on the IGBTs. That surge may exceed the maximum IGBT collect-emitter voltage and damage them.

The miniature iso-amp (ACPL-C79A) is often used as a voltage sensor in DC bus monitoring applications. A designer must scale down the DC bus voltage to fit the input range of the iso-amp by choosing R1 and R2 values to get an appropriate ratio.

under development implemented as software on a high-performance microprocessor or DSP in simulations and prototypes. As the volatility and uncertainty of the workload implementation stabilized, the developers would migrate it to an FPGA to optimize performance, price, and energy consumption. Once designers adopted the workload for a large number of high-volume designs, a semiconductor company might decide to produce a specialized processor or coprocessor integrated with a microprocessor or DSP that targeted the specific workload; that development, in turn, would justify yet another migration of the workload, this time to a software implementation on said device. None of those migrations would be cause for concern that microprocessors, FPGAs, or DSPs were becoming obsolete.

SWEET SPOTS

The real-world experience for these different processing implementations (microprocessor, DSP, and FPGA) is that the "best choice" among them will depend on the targeted type of processing, and that as a result they often sit side by side in the same design. Is the "When will 8-bit be dead?" question likewise subject to different circumstances?

The spectrum of processing sweet spots (**Figure 1**) helps to illustrate how and why these migration events might be different. The spectrum maps each type of processor architecture onto a two-dimensional space that represents a design's processing complexity as a function of computational or workload intensity versus the number of contexts a system must manage.

Workload intensity is represented on the horizontal axis and can indicate the peak magnitude, total amount, or sustained amount of processing performance the system needs within a unit of time or energy. Workloads that are farthest to the left on the spectrum tend to optimize to a limited energy budget; those toward the right end of the spectrum tend to optimize to a limited time budget for completion.

The number of contexts a system must manage is represented on the vertical axis and can indicate internal system states, the number of system inputs and outputs, whether the data is scalar or aggregate in structure, or even a level of possible states or conditional control flows that the system must support.

These two complexity measures enable the major processor architectures to be mapped into zones in which they are best suited to operate. Although the spectrum indicates specific regions for each type of processing-architecture option, there is usually significant overlap between the bordering edges of each region; in **Figure 1**, the overlap between regions is implied so as to reduce the clutter of an already complex figure. In each identified region, the processing offerings that fit within that area share common architectural features that differ from those of devices residing in other regions (see **sidebar**, "Architectural differences").

Unlike the identified sweet-spot regions, the various processor bit widths do not map mutually exclusively to specific processor architectures (**Figure 2**). Notably, however, 4- and 8-bit processors fall only within the microcontroller zone (with the technical exception of soft 8-bit cores used as microcontrollers in FPGAs), and it is specifically the 32-bit microcontroller that is the presumptive usurper of the 8-bit microcontroller; hence the justification and opportunity for the continually posed question about the pending death of the 8-bit processor.

Four-bit processors reside at the bottom-left corner of the sweet-spot spectrum (**Figure 2**), and they are explicitly included because companies are still making 4-bit processors in quantity, despite the lack of public marketing from vendors and users. In fact, companies involved in the 4-bit market appear reluctant to reveal much, presumably for competitive reasons; but I have teased out some non-intuitive, useful insights about the market through informal conversations with participants.

These companies do not sell their 4-bit processors to the public developer community in the same way that participants in the market for 8-, 16-, and 32-bit processors generally sell their offerings. Like the semiconductor companies that produce processors at the bleeding edge of technology (along the rightmost edge of the spectrum), 4-bit processor providers actively seek out and identify the designers that can best make use of their processors—not the other way around. A 4-bit processor provider approaches a potential developer and works out specific implementation details to demonstrate how its 4-bit device can provide differentiation to the developer's design and end product.

DATA SHEETS

For a collection of data sheets on the latest FPGAs, DSPs, and other processors, go to **www.datasheets.com**.

Four-bit processors are manufactured only for dedicated high-volume products. Some, if not all, 4-bit processors are available only as ROM-based devices. To accommodate the high labor intensity of verifying the mask sets, vendors of such devices limit the number of engaged customers to those who will consume very large quantities.

Further, 4-bit processors are programmed in assembly language only. The software development tools cost in the range of $10,000, and, at least according to the company that shared its information with me, the vendor lends the development tools to its clients; it does not sell the tools.

The sweet spot for 4-bit processor designs is single-battery applications for which the typical life span is 10 years and the device is active perhaps 1% of that time, spending the other 99% in standby mode. An interesting differentiator for 4-bit processors is that they can operate at 0.6V; this provides an energy-consumption advantage over even 8-bit processors. Also, 4-bit processors have been supporting energy-harvesting designs since 1990, whereas 8-, 16-, and 32-bit processor vendors have started offering development and demonstration kits only within the past few years.

STRIVE FOR RIGHTSIZING

We have already stipulated that we are looking at a 32-bit microcontroller that has reached price and energy-performance parity with an 8-bit microcontroller or has even surpassed it on those parameters. How is this possible?

Let's tackle price first. The 32-bit device is manufactured in a state-of-the-art process geometry, whereas the 8-bit device is manufactured in a much larger process node but in a fully depreciated facility. Even though the buses in the 32-bit core are four times as wide, the relative area of silicon each

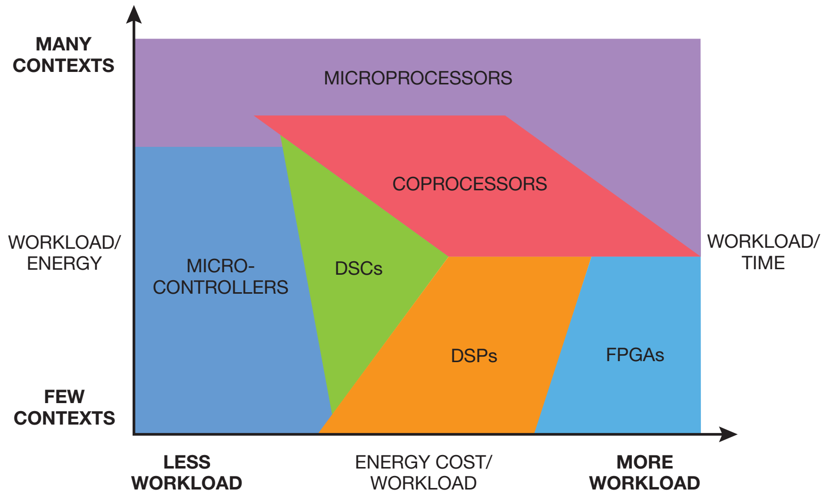


Figure 1 This taxonomy mapping identifies the processing sweet-spot spectrum of mainstream processing architectures. The labels near the edges of the chart identify the key trade-offs for extreme processing innovations for processors near those edges (courtesy Embedded Insights).

CPU consumes approaches parity as the distance between the two process nodes increases. Additionally, in larger devices, the core itself represents a diminishing share of the silicon; the memory and peripherals consume the vast majority of the silicon area. In fact, 32-bit microcontrollers broke the $1 barrier years ago, and the smallest devices have even broken the 50-cent price point, placing those devices squarely in the price range of 8-bit microcontrollers.

There are a few costs, however, that the 32-bit microcontrollers must cover but the 8-bit devices can avoid. We've already mentioned the depreciation on the fabrication facilities. Further, because we are assuming the 32-bit device is an ARM microcontroller, the price must cover the royalty fee due for using ARM's IP (intellectual property), further cutting into relative margins.

Also cutting into relative margins is the fact that 32-bit devices are more support intensive; this is where using a 32-bit IP enables a semiconductor company to leverage some of the support costs through shared development

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resources with other companies. The support costs for 8-bit devices can be lower because the target applications are generally simple in scope and size, operate at "slow" clock rates, and are supported by a fiercely dedicated and cooperative developer/user community external to the supplying vendor. In short, there are probably multiple vectors that let an 8-bit vendor wiggle on price and manufacturing when a 32-bit device poses a real threat solely because of price parity.

What about when the 32-bit processor meets or exceeds the 8-bit microcontroller's energy performance? Here, the 32-bit device leverages a double-prong approach to challenge 8-bit devices: code density and the time to perform a wake/sleep cycle.

Rob Cosaro, senior director for architectures and systems at NXP Semiconductors' microcontroller business, says the company's benchmarking research has shown up to a 50% reduction in code size when performing the same algorithm on a Cortex-M0-class processor as on an 8051. But benchmarks are tricky unless they reflect the code your design is using. For example, the Coremark benchmark from EEMBC (the Embedded Microprocessor Benchmark Consortium) contains func-

ARCHITECTURAL DIFFERENCES

The characteristics for mapping processing sweet spots as indicated in Figure 1 are relative computational workload and number of contexts. Workload can indicate the peak magnitude, total amount, or sustained amount of processing performance the system needs within a given amount of time or energy. The number of contexts can indicate internal system states, the number of system inputs and outputs, or a level of possible contexts that the system must support.

Each of the identified processor types evolved over time at different rates, and each trades off one or more measures of performance to maximize one or more other measures of performance.

Microcontrollers are specialized processors that offer a cost and energy-efficiency advantage at the expense of flexibility and workload processing. They provide a cost advantage by integrating memories and peripherals into a single package. They provide an energy-consumption advantage partly because they target workloads that operate with lower clock rates and partly because they implement only the minimum set of circuitry to perform control processing. If a design needs the flexibility of a larger or a smaller memory, different peripheral set, or higher clock rate, the designer must swap out the processor for a different one. Some microcontrollers provide deterministic operation by not employing caches or pipelines. Microcontrollers often target system control workloads with frequent and prioritized context switching.

DSPs also focus on optimizing cost and energy efficiency at the expense of workload flexibility. They sacrifice efficiency in handling context switching to maximize their performance of continuous and repetitive calculations. They do not integrate many peripherals, because they are not ideally structured to handle the context switching that accommodating many peripherals could require. The most common integrated peripheral is an ADC that the DSP uses to collect a stream of real-world data to process.

DSPs employ multiple buses and memory structures so that they can perform simultaneous memory operations to support continuous single-cycle multiply/accumulate operations. They may employ specialized registers to minimize memory accesses and enable zero-overhead looping. DSPs are used in systems that perform continuous signal processing on sustained streams of data and are often combined with hardware accelerators or FPGAs to perform heavy lifting for intensive computational workloads.

DSCs (digital signal controllers) focus on optimizing cost and energy efficiency by combining features of DSPs and microcontrollers in a single processor to handle both context switching and signal processing competently. These devices provide more workload flexibility than DSPs while retaining the ability to perform repetitive workloads efficiently on a sustained stream of data.

FPGAs provide a highly flexible programmable hardware platform that can leverage arbitrarily wide signal-processing algorithms and act as hardware-acceleration blocks. FPGA signal processing works well when it involves few decision states and large amounts of processing per data point.

The coprocessors category relies on hardware acceleration to speed workload processing, reduce energy consumption, or both. Coprocessors are usually not stand-alone, instead typically connecting with or being integrated directly into a single package with another processor, such as a DSP or a microprocessor.

Microprocessors excel at workload flexibility by employing general-purpose architectures that enable them to perform well enough across the range of processing tasks. They do not handle context switching as quickly or deterministically as microcontrollers do, nor can they handle looped processing as quickly or efficiently as DSPs can. Microprocessors are ideal, however, when the processing requirements are not well known, such as when a system supports user-loaded applications.

Microprocessors generally support large memory-address spaces and rely on large on-chip caches to compensate for time penalties from off-chip memory accesses. They are appropriate for "quick and dirty" prototyping and proof-of-concept exploration when cost and energy efficiency are less important than a short development cycle.

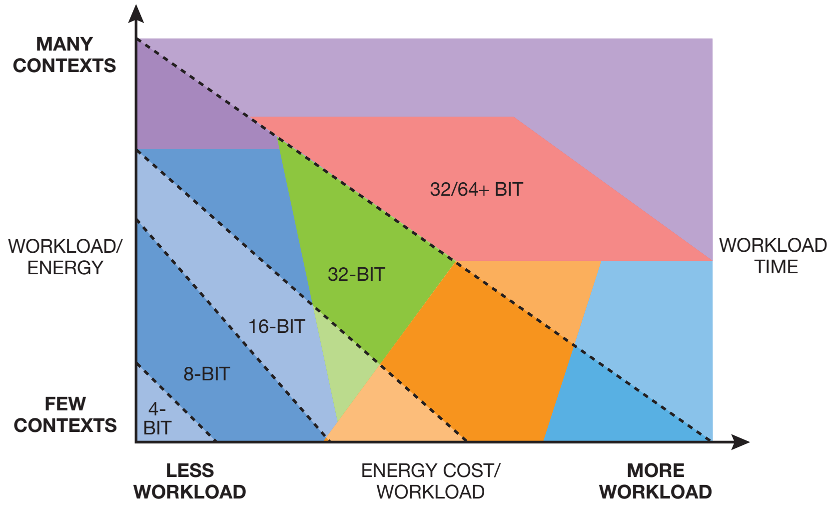

Figure 2 Processor bit widths are superimposed over the sweet-spot spectrum to indicate the processing sizes implemented in each sweet spot (courtesy Embedded Insights).

tions that test 8-, 16-, and 32-bit CPUs, but functions such as a double link list and matrix manipulation are likely tasks you would not consider performing on an 8-bit device.

The opportunity for a 32- or even a 16-bit processor to provide better code density arises when an 8-bit processor is used outside its ideal region of use, such as for operating on data larger than 8 bits (because it requires multiple data accesses to operate on a single datum), operating on data sets that exceed 16 to 64 kbytes of address space, operating at high clock rates (higher than 20 to 50 MHz), or even supporting heavy network communication stacks. In such cases, the application may be mismatched with an 8-bit processor because maintenance-related feature growth has crept into the system over a period of years.

In embedded designs that are energy sensitive, the microcontroller spends most of the time in a low-power sleep mode and wakes up periodically to perform its tasks. As in the case of code density, if the task that the 8-bit microcontroller is performing is mismatched, a 32-bit microcontroller may be able to wake up, perform the tasks, and go back to sleep fast enough that it actually consumes less energy than the 8-bit device performing the same task.

A key advantage of an 8-bit microcontroller over a 32-bit processor that may be able to take over its tasks is that the 8-bit device may have enabled the task to be performed at a cost- and energy-effective level several years before the 32-bit device was able to replace the 8-bit controller. The excitement in the small-processor segment centers on the smallest ones—the ones that push the cost and energy-performance limits of what has been possible. What we describe as low power is a constantly shifting target. Smaller data widths will always significantly lead wider widths in when they become able to support those small tasks.

There is one other factor that will not show up in a data sheet but that matters when choosing between 8- and 32-bit devices that have achieved price and energy-performance parity: domain expertise. Though programming an 8-bit device may require fluency in assembly or even C language, the most important knowledge a developer can have is domain knowledge.

Consider why COBOL programmers are still in demand, even though most people consider COBOL to be an obsolete programming language. The language is straightforward and easy to understand. The assumption about—and perceived value of—experienced COBOL programmers is that they understand the business issues that COBOL programs solve.

In a similar way, 8-bit microcontrollers target different problem sets than 32-bit devices do, and developers of 32-bit systems address different domains than 8-bit developers do. For example, in a properly sized 8-bit application, there are no awkward memory limitations, because the application is fully understandable and can be sized to fit within the architecture's natural limits. A 32-bit application can handle much more uncertainty and can leverage and manage a larger memory space via dynamic memory in a way no 8-bit developer would ever consider.

The size of the data should reflect the natural size of the processor; special handling of large numbers or floating-point operations should not be extensively performed on a device that was not designed for them. Eight-bit microcontrollers ideally target simple or constrained tasks. Systems that use operating systems and middleware do so for developer productivity because the system is too complicated to build from scratch, whereas building a simple scheduler from the ground up is relatively straightforward.

Ultimately, each type of processor architecture requires the designer to employ a different thought process when building systems with it. As long as there is a demand for new development to push the edge of what is possible with ever smaller energy budgets, and as long as processor vendors actively support small-width devices for those designs, there will be a market—even if only temporarily—for 8-bit devices. It might be easier if we stopped thinking of low-power, small-data-width processors as essentially the same as their larger, 32-bit cousins, because they best address a different set of issues.

MICROPROCESSORS

The explosion of ARM-based processors contained in mobile devices has caused some people to ask whether ARM will displace other microprocessor architectures in other markets. The incumbent microprocessor architectures, however, have a secret weapon that is analogous to the 8-bit microcontrollers: domain knowledge that is embedded in the architecture and ecosystem of the incumbent architecture.

Consider that specific variants of a microprocessor architecture will include features—developed, tested, and refined over the years—that make those variants especially well suited to the target application's specific requirements. Also consider the body of software that serves the given market. A strong incumbent microprocessor architecture, much like the 8-bit microcontrollers, is surrounded by a strong and mature ecosystem of developers, tools, operating systems, and middleware that provides a buffer for the incumbent to respond to a challenger.

A specific example of incumbent advantage can be seen in the current battle to determine which microprocessor architecture will ultimately own the tablet space. The ARM architecture currently has the apparent incumbent advantage because many tablet designs treat the device as a large smartphone, and the ARM architecture has many man-years of design knowledge tied up in the hardware and software to support the smartphone market. If the tablet space stays anchored to the smartphone model, the ARM architecture is well positioned. There are tablet products based on other microprocessors, however, that may define tablets differently. For example, if Microsoft can redefine the tablet market to leverage the ecosystem for its Windows OS, the market could be completely different from today's tablet market.

By some estimates, vendors have introduced more than 200 processor architectures over the past few decades. Most of those have disappeared or have been absorbed into other architectures. The few dozen architectures that currently provide developers with the tools and means to create today's applications encompass complex ecosystems of processors and development tools, along with domain-specific engineering and software support. Would the developer market be better served if there were even fewer architectures from which to choose?

The massive churn in the processor market is a testament to the complexity and difficulty of figuring out the correct way to serve that market. The uncertainty is not an artifact of the past but remains very much a part of today's technology. One indicator of that uncer-

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tainty is the lingering question of whether 8-bit is dead.

I have recently learned that some companies are quietly exploring ways to increase raw processing performance significantly by reducing the data word size in certain DSP applications. Part of the challenge is determining an acceptable trade-off between the problems that the short word size might introduce and the benefits of the resultant higher performance at lower power. There are some DSPs available today that support 8×8 MACs (multiply-accumulates) within a larger execution engine. In short, is an 8-bit DSP in our future? You never know from what direction the next best idea will come. If we had fewer processor architectures to choose from, there would be fewer opportunities for crazy ideas like an 8-bit DSP to bubble up.

MANY COMMENTERS ARGUE THAT IF WE HAD FEWER ARCHITECTURAL CHOICES, SOFTWARE CODE WOULD BE EASIER TO MAINTAIN.

Many commenters argue that if we had fewer architectural choices, software code would be easier to maintain because a larger base of developers would be able to access, use, and maintain it. Would a common architectural base improve the transferability of existing domain expertise and, more important, the development of new domain expertise?

Based on what I see large semiconductor companies doing, I suspect fewer architectural choices would lead to slower innovation because there would be only enough resources within the development support ecosystem to address the engineering issues of the largest volume applications. That could negatively affect efforts toward discovering emergent applications that would otherwise replace the current large-volume applications.

Like the different races of Middle-earth, each available processor architecture encompasses its own unique domain culture or development ecosystem that enables it to be the best at performing some tasks better than the alternatives. Most designs already use multiple processors, and the wide variety of processor offerings lets developers pick and use best-in-class devices and software in their designs. The successful rise of a single architecture to rule them all may be the key to opening up developer productivity—but it could also become a shackle that enforces conformity and limits the direction and opportunity for disrupting innovation.

Be careful what you wish for; you might get it. **EDN**

AUTHOR'S BIOGRAPHY

Robert Cravotta is principal analyst and cofounder at Embedded Insights. He covered embedded processors as a technical editor at EDN, and before that he worked in the aerospace industry on electronics and controls for pathfinding projects such as fully autonomous vehicles, space and aircraft power management systems, and space-shuttle payloads, as well as building automation systems. He received a master's degree in engineering management from California State University Northridge and a bachelor's degree in computer-science engineering from the University of California, Los Angeles.

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Common inter-IC digital interfaces for audio data transfer

UNDERSTANDING THE PROS AND CONS OF DIFFERENT INTERFACES BEFORE SELECTING PARTS HELPS TO STREAMLINE YOUR COMPONENT SELECTION AND ENSURE THAT YOU HAVE THE MOST EFFICIENT IMPLEMENTATION OF THE SIGNAL CHAIN.

As audio integrated circuits move to finer geometries, it becomes more difficult to design—and less cost-effective to integrate—high-performance analog circuits on the same piece of silicon with high-density digital circuits. Audio-system architects thus are pushing analog portions of the audio signal chain further toward the input and output transducers and are connecting everything in between digitally.

A traditional audio signal chain may have analog signal connections between microphones, preamps, ADCs, DACs, output amplifiers, and speakers, as shown in **Figure 1**. As the analog circuits are pushed to the edges of the signal chain, however, digital interfaces between ICs in the chain become more prevalent. DSPs have always had digital connections, but now digital interfaces are being included on the transducers and amplifiers, which typically have had only analog interfaces.

IC designers are integrating ADCs, DACs, and modulators in the transducers on opposite ends of the signal chain, thereby eliminating the need to route any analog audio signals on the PCB, as well as reducing the number of devices in the signal chain. **Figure 2** shows an example of a completely digital audio signal chain.

Many standards exist for transmitting digital audio data. Some formats, such as I^{2}S (inter-IC sound), TDM (time-division multiplexed), and PDM (pulse-division multiplexed), are typically used to enable inter-IC communication on the same PCB. Other formats, such as S/PDIF and Ethernet AVB, primarily target data connections from one PCB to another through cabling.

This article focuses on the differences, advantages, and disadvantages of the inter-IC digital audio formats. Choosing audio components with mismatched digital interfaces needlessly complicates the system design. Understanding the pros and cons of the different interfaces before selecting parts helps to streamline component selection and ensure the most efficient implementation of the signal chain.

Inter-IC Sound (more commonly called "I squared S" or "I two S") is the most common digital audio format used for audio data transfer between ICs. Philips Semiconductors—now NXP—introduced the I^{2}S standard in 1986; the format was revised in 1996. The interface was first popularly used in CD-player designs and now can be found in almost any application that involves the transfer of digital audio data from one IC to another. Most audio ADCs, DACs, DSPs, and sample-rate converters, as well as some microcontrollers, include I^{2}S interfaces.

An I^{2}S bus uses three signal lines for data transfer: a frame clock, a bit clock, and a data line. The receiving IC, the transmitting IC, or even a separate clock-master IC can generate the two clocks, depending on the system architecture (**Figure 3**). An IC with an I^{2}S port often can be set to be in either master or slave mode. Unless the design uses a sample-rate converter in the signal chain, a system will usually have a single I^{2}S master device so that there are no issues with data synchronization.

The Philips standard for these signals uses the designations

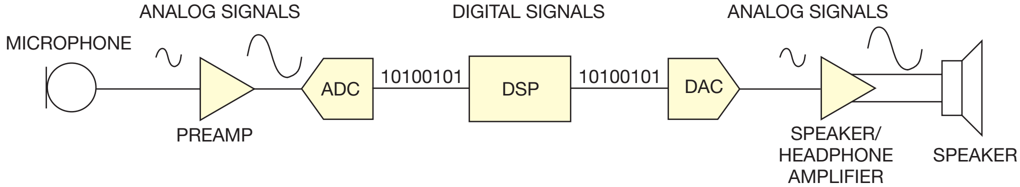

Figure 1 A traditional audio signal chain may have analog signal connections between microphones, preamps, ADCs, DACs, output amplifiers, and speakers.

WS for word select, SCK for the clock, and SD for the data, although IC manufacturers seem to use those names only rarely in their IC data sheets. Word select is also commonly called LRCLK, for "left/right clock," and SCK may alternatively be called BCLK, for "bit clock," or SCLK, for "serial clock."

The name of an IC's serial data pin varies most from one IC vendor to another and even among a single vendor's products. A quick survey of audio IC data sheets shows that the SD signal may also be called SDATA, SDIN, SDOUT, DACDAT, ADCDAT, or other variations on these, depending on whether the data pin is an input or an output.

An I²S data stream can carry one or two channels of data with a typical bit-clock rate between 512 kHz, for an 8-kHz sampling rate, and 12.288 MHz, for a 192-kHz sampling rate. The data word length is often 16, 24, or 32 bits. For word lengths less than 32 bits, the frame length is often still 64 bits; the unused bits are just driven low by the transmitting IC.

Although it is rare, some ICs support only I²S interfaces with a maximum of 32- or 48-bit clocks per stereo-audio frame. When using such an IC, the system

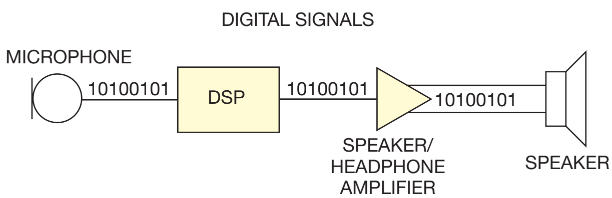

Figure 2 IC designers are integrating ADCs, DACs, and modulators in the transducers on opposite ends of the signal chain, thereby eliminating the need to route any analog audio signals on the PCB and reducing the number of devices in the signal chain. An example of a completely digital audio signal chain is shown here.

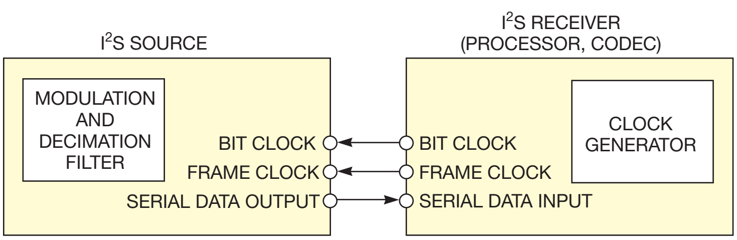

Figure 3 An I²S bus uses three signal lines for data transfer: a frame clock, a bit clock, and a data line. The receiving IC, the transmitting IC, or even a separate clock-master IC can generate the two clocks, depending on the system architecture.

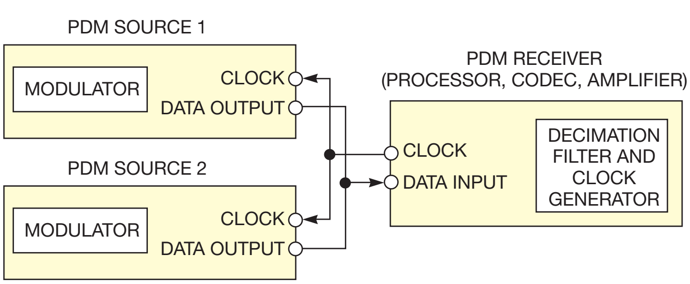

Figure 4 In this system diagram, two PDM sources drive a common data line into a receiver.

designer must take care to ensure that the devices on the other end of its connections also support those bit-clock rates.

Though I^{2}S is the most commonly used format, there are other variants of the same three-wire configuration, such as left-justified, right-justified, and PCM modes. Such formats differ from I^{2}S based on the position of the data word in the frame, the polarity of the clocks, or the number of bit-clock cycles in each frame.

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TDM FORMATS

Some ICs support multiple I^{2}S data inputs or outputs using a common clock, but such an approach obviously increases the number of pins necessary to transfer the data. TDM formats are used when more than two channels of data are to be transferred on a single data line. A TDM data stream can carry as many as 16 channels of data and has a data/clock configuration similar to that of I^{2}S.

Each channel of data uses a slot on the data bus that is 1/Nth the width of the frame, where N is the number of channels being transferred. For practical purposes, N is usually rounded up to the nearest power of two (2, 4, 8, or 16), and any additional channels are left empty. A TDM frame clock is often implemented as a single bit-wide pulse, as opposed to the 50% duty-cycle clock of I^{2}S. Clock rates above 25 MHz are not commonly used for TDM data, because higher frequencies cause board-layout issues that PCB designers would rather avoid.

TDM is commonly used for systems in which multiple sources feed one input or one source drives multiple devices. In the former case (multiple sources feeding one input), each TDM source shares a common data bus. The source must be configured to drive the bus only during its appropriate channel and to tristate its driver when other devices are driving other channels.

No standard akin to the Philips standard for I^{2}S exists for TDM interfaces, and as a result many ICs have their own, slightly different flavor of TDM implementation. The variants can differ in such aspects as clock polarity, channel configuration, and tristating or driving unused channels. Of course, the different ICs will usually work together, but the system designer must take care to ensure that the outputs of one device will spit out data in the format that the inputs of another are expecting.

PDM DATA CONNECTIONS

PDM data connections are becoming more common in portable audio applications, such as cell phones and tablet computers. PDM is an advantage in size-constrained applications because it allows audio signals to be routed around noisy circuitry, such as LCD screens, without having to deal with the interference issues that analog audio signals may have.

With PDM, up to two audio channels can be transmitted with only two signal lines. **Figure 4** shows a system diagram with two PDM sources driving a common data line into a receiver. The system master generates a clock that can be used by two slave devices, which use alternate edges of the clock to output their data on a common signal line.

The data is modulated at a 64× rate, resulting in a clock that is typically between 1 and 3.2 MHz. The bandwidth of the audio signal increases as the clock rate increases, so lower-frequency clocks are used in systems that can trade off a reduced bandwidth for lower power consumption.

A PDM-based architecture differs from I^{2}S and TDM in that the decimation filter is in the receiving IC rather than the transmitting IC. The output of the source is the raw high-sample-rate modulated data, such as the output of a sigma-delta modulator, rather than decimated data, as it is in I^{2}S. A PDM-based architecture reduces the complexity in the source device and often makes use of decimation filters that are already present in a codec's ADCs.

With this approach, system designers not only can use audio codecs that they may already be using but also can take advantage of a digital data connection's reduced sensitivity to interference. Further, decimation filters may be more efficiently implemented in the finer silicon geometries used for fabricating a codec or processor, rather than in the processes used for the microphone ICs.

Codecs, DSPs, and amplifiers have had I^{2}S ports for years, but until now a system's input devices, such as microphones, have had either analog or PDM outputs. As digital interfaces are pushed further toward the ends of the signal chain, new ICs will be needed to support the new system architectures.

Microphones, such as the Analog Devices ADMP441

MEMS microphone, that have an integrated I^2S interface make it easier for designers to build this component into systems in which PDM microphones are not easily used or analog interfaces are not desired. Only a subset of audio codecs accepts a PDM input, and very few audio processors outside of those specifically designed for mobile phones and tablets natively accept this type of data stream.

In some designs, an I^2S output microphone could completely eliminate the need for any analog front-end circuits because many designs may have only an ADC and PGA to support a microphone input to the processor. An example of such a system is a wireless microphone with a digital transmitter. The wireless transmitter SOC may not have a built-in ADC, so using an I^2S output microphone enables completely digital connections between the transducer and transmitter.

I^2S, TDM, and PDM audio interfaces each have their advantages and applications for which they are best suited. As more audio ICs transition from analog to digital interfaces, system designers and architects will need to understand which interface would be most appropriate for a particular design. With a digital signal chain from microphone to DSP to amplifier, analog signals can be pushed completely off of the PCB and exist only in the acoustic domain. **EDN**

ACKNOWLEDGMENT

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AUTHOR'S BIOGRAPHY

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READERS SOLVE DESIGN PROBLEMS

Booster circuit enables reliable solenoid operation

SV Nakhe and DVS Raju, Raja Ramanna Centre for Advanced Technology, Indore, India

Solenoids at turn-on draw current that is much higher than the current needed to keep the armature pulled in. Further, because of the power dissipated in the coil, the solenoid's temperature will rise, and its dc resistance will increase. The applied voltage, therefore, must be increased to ensure reliable pull-in. Rather than increase the power supply voltage and current capability, this Design Idea presents a novel workaround based on a momentary voltage boost to turn on the solenoid.

The booster circuit operates from the existing supply voltage provided for the solenoid. Whenever the solenoid is to be switched on, the voltage-booster circuit is activated and charges a capacitor to approximately double the supply voltage. After the capacitor is charged (after 470 msec), it is connected to the solenoid. The charged capacitor provides additional energy that augments the nominal power source used to operate the solenoid. The circuit will reliably operate the solenoid under low-supply-voltage and high-temperature conditions. The booster circuit remains in standby mode after the solenoid is switched on.

The circuit in **Figure 1** is designed to drive a solenoid rated at a 12V dc, nominal, supply voltage and a 0.8A, nominal, current. The 12V supply used to operate the solenoid also powers the voltage-booster circuit. With power applied, but before the control signal is

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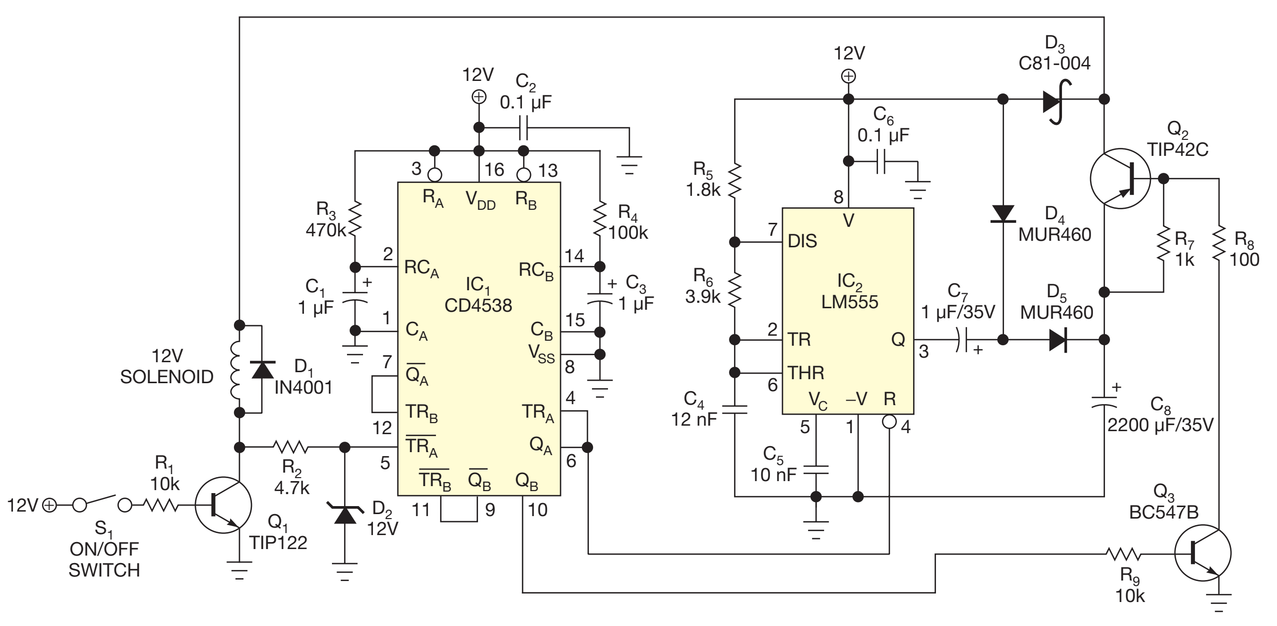

Figure 1 The voltage-booster circuit is designed to drive a solenoid rated at a 12V dc, nominal, supply voltage and a 0.8A, nominal, current.

LINEAR TECHNOLOGY DESIGN NOTES

High Voltage Inverting Charge Pump Produces Low Noise Positive and Negative Supplies – Design Note 507

Marty Merchant

Introduction

Dual-polarity supplies are commonly needed to operate electronics such as op amps, drivers, or sensors, but there is rarely a dual-polarity supply available at the point of load. The LTC®3260 is an inverting charge pump (inductorless) DC/DC converter with dual low noise LDO regulators that can produce positive and negative supplies from a single wide input (4.5V to 32V) power source. It can switch between high efficiency Burst Mode® operation and low noise constant frequency mode, making it attractive for both portable and noise-sensitive applications. The LTC3260 is available in a low profile 3mm × 4mm DFN or a thermally enhanced 16-lead MSOP, yielding compact solutions with minimal external components. Figure 1 shows a typical 12V to ±5V application featuring the LTC3260.

Inverting Charge Pump

The LTC3260 can supply up to 100mA from the inverted input voltage at its charge pump output, V_{OUT}. V_{OUT} also serves as the input supply to a negative LDO regulator, LDO⁻. The charge pump frequency can be adjusted between 50kHz to 500kHz by a single external resistor. The MODE pin is used to select between a high efficiency Burst Mode operation or constant frequency mode to satisfy low noise requirements.

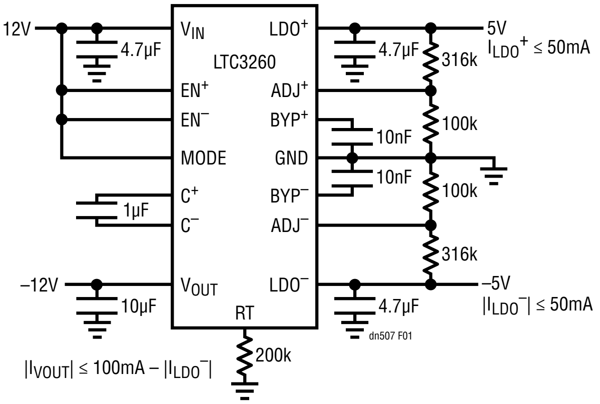

Figure 1. Typical 12V to ±5V Supply

Constant Frequency Mode

A single resistor at the RT pin sets the constant operating frequency of the charge pump. If the RT pin is grounded, the charge pump operates at 500kHz, where the open-loop output resistance (R_{OL}) and the output ripple are optimized, allowing maximum available output power with only a few millivolts peak-to-peak output ripple.

Light load efficiency can be increased by reducing the operating frequency, as shown in Figure 2, but at the expense of increased output ripple. The lower operating frequency produces a higher effective open-loop resistance (R_{OL}), but the reduced switching rate also reduces the input current, resulting in increased efficiency at light loads. Furthermore, at relatively heavy loads, the increased R_{OL} reduces the effective difference between V_{OUT} and LDO⁻—decreasing the power dissipation in the negative LDO. The cumulative result is higher overall efficiency with high input voltages and/or light loads.

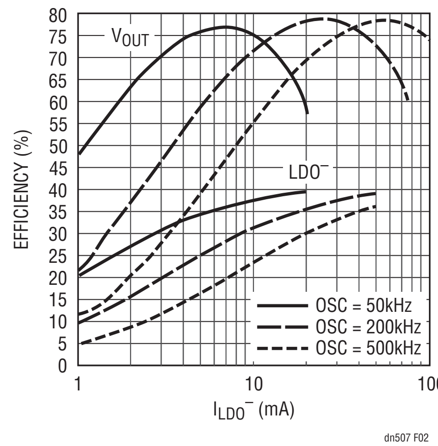

Figure 2. LTC3260 V_{IN} to V_{OUT} and V_{IN} to LDO⁻ Efficiency vs Frequency for the Circuit in Figure 1

Reducing the frequency increases the output ripple as shown by the expression below and in Figure 3.

$$V_{RIPPLE(PK-PK)} \approx \frac{I_{OUT} \bullet t_{OFF}}{C_{OUT}}$$

$$\text{where } t_{OFF} = \left(\frac{1}{f_{OSC}} - 1\mu s \right)$$

In general, constant frequency mode is suitable for applications requiring low output ripple even at light loads, but further gains in light load efficiency can be gained by using Burst Mode operation, described below.

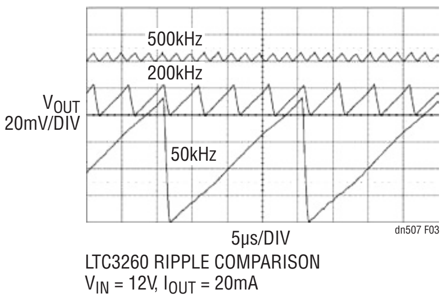

Figure 3. V_{OUT} Constant Frequency Ripple Comparison at 500kHz, 200kHz and 50kHz at 20mA Load

Burst Mode Operation

Figure 4 shows the light-load efficiency of the charge pump in Burst Mode operation. Burst Mode operation increases the output ripple over constant frequency mode, but the increase in ripple is only a small percentage of V_{IN}, as shown in Figure 5.

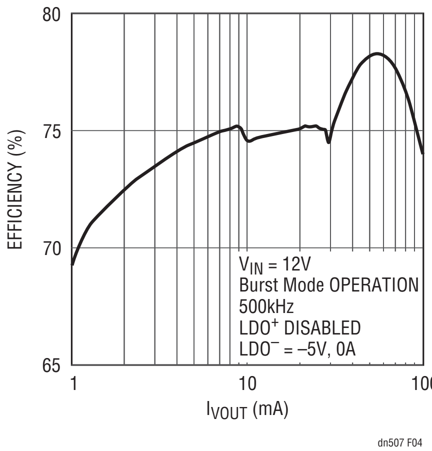

Figure 4. LTC3260 Burst Mode Operation Efficiency

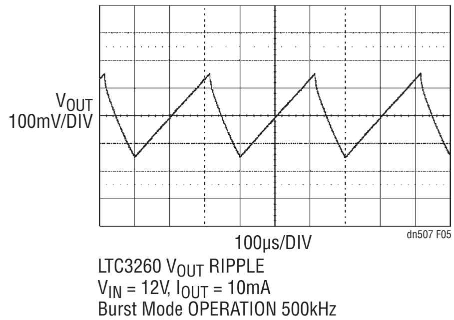

Figure 5. V_{OUT} Ripple in Burst Mode Operation

Burst Mode operation is implemented by charging V_{OUT} close to $–V_{IN}$. The LTC3260 then enters a low quiescent current sleep state, about 100μA with both LDO regulators enabled, until the burst hysteresis is reached. Then the charge pump wakes up and the cycle repeats. The average V_{OUT} is approximately $–0.94V_{IN}$. As the load increases, the charge pump runs more often to keep the output in regulation. If the load increases enough, the charge pump automatically switches to constant frequency mode in order to maintain regulation.

Dual LDOs

Both of the LTC3260's LDOs—the positive LDO regulator supplied from V_{IN}, and the negative LDO regulator supplied from V_{OUT}—are capable of supporting 50mA loads. Each LDO has a dropout voltage of 300mV with a 50mA output and has an adjust pin, allowing the output voltage to be set by a simple resistor divider. The LDO regulators can be individually enabled. The $EN^{–}$ pin enables both the inverting charge pump and $LDO^{–}$. When both regulators are disabled, the part shuts down with only 2μA of quiescent current. The LDO references can be filtered by adding a capacitor on each of the bypass pins to further reduce noise at the LDO regulator outputs.

Conclusion

The LTC3260 produces low noise positive and negative supplies from a single positive power source. The LTC3260 features optional Burst Mode operation for light-load efficiency in battery-powered devices, or low noise constant frequency mode for noise-sensitive applications. The LTC3260's combination of inverting charge pump and dual LDO regulators yields elegant solutions to applications with 4.5V to 32V inputs.

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DESIGN NOTES

Bootstrap Biasing of High Input Voltage Step-Down Controller Increases Converter Efficiency

Design Note 493

Goran Perica and Victor Khasiev

Introduction

High voltage buck DC/DC controllers such as the LTC3890 (dual output) and LTC3891 (single output) are popular in automotive applications due to their extremely wide 4V to 60V input voltage range, eliminating the need for a snubber and voltage suppression circuitry. These controllers are also well suited for 48V telecom applications where no galvanic isolation is required.

In a typical application for these controllers, the IC's supply voltage ($INTV_{CC}$) is provided by the on-chip LDO. This LDO produces 5V from input voltages up to 60V to bias control circuitry and provide power FET gate drive. Although simple, this built-in biasing scheme can be inefficient. Power losses can be significant in applications where the input voltage is consistently high, such as in 48V telecom applications. Reducing the power losses in the bias conversion can increase efficiency and also reduce the controller case operating temperature.

Employing $EXTV_{CC}$ to Improve Efficiency

One of the attractive features of the LTC3890 and LTC3891 controllers is the external power input ($EXTV_{CC}$). This is a second on-chip LDO, which can be used to bias the chip. When the input voltage is consistently high, it is more efficient to produce the biasing voltage by stepping down the converter's output voltage, which is fed into $EXTV_{CC}$, rather than generating 5V $INTV_{CC}$ from the high input voltage.

Figure 1 shows a block diagram for this scheme. The output can be directly connected to the $EXTV_{CC}$ pin of the chip as long as the output voltage is above 4.7V. However, extra circuitry (described in the following section) is required for outputs below 4.7V.

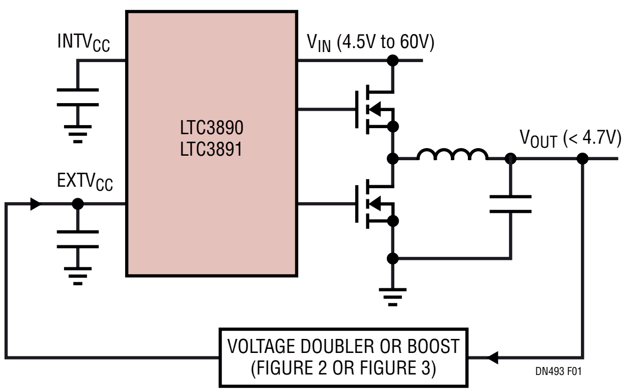

Figure 1. Block Diagram Showing External Bias

Voltage Doubler for Output Voltages Below 4.7V

When the controller's output is below 4.7V, it must be stepped up to allow the built-in LDO to work. A simple voltage doubler solves this problem as long as the output is higher than 2.5V. Below 2.5V output, a multivibrator-based circuit can be used.

Figure 2 shows a simple, low cost solution for output voltages between 2.5V and 4.7V. This is a voltage doubler scheme based on small P-channel and N-channel MOSFETs, Q1 and Q2. The gates of these transistors are controlled by the bottom gate driver, BG of the controller. When BG is high, Q2 is on, Q1 is off and capacitor C1 charges from output voltage V_{OUT} through D1. When BG is low, Q2 is off, Q1 is on and capacitor C1 delivers a voltage close to 2 • V_{OUT} to $EXTV_{CC}$.

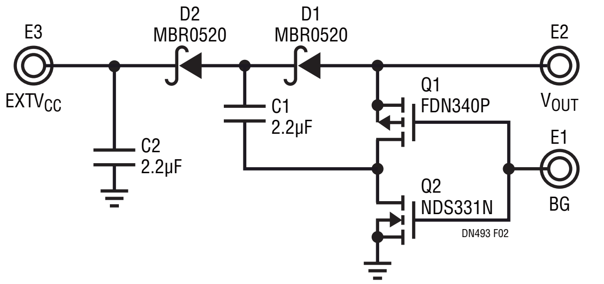

Figure 2. Voltage Doubler Allows External Bias from V_{OUT} in the Range of 2.5V to 4.7V

Figure 3 shows a solution for voltages below 2.5V. The circuit consists of an astable multivibrator based on transistors Q1 and Q2, and a boost based on N-channel Q3 and inductor L1. Q1 and Q2 are biased from $INTV_{CC}$ and output voltage V_{OUT} is stepped up to 5V, which feeds $EXTV_{CC}$. The multivibrator frequency is set at 50kHz to minimize the EMI signature. The pulse width is defined by the ratio of resistors R1 and R2, as per the following expressions:

$$R1 = \frac{T \bullet (1-D)}{0.7 \bullet C1}$$

$$R2 = \frac{T \bullet D}{0.7 \bullet C2}$$

$$D = \frac{EXTV_{CC} - V_{OUT}}{EXTV_{CC}}$$

$$T = \frac{1}{f}$$

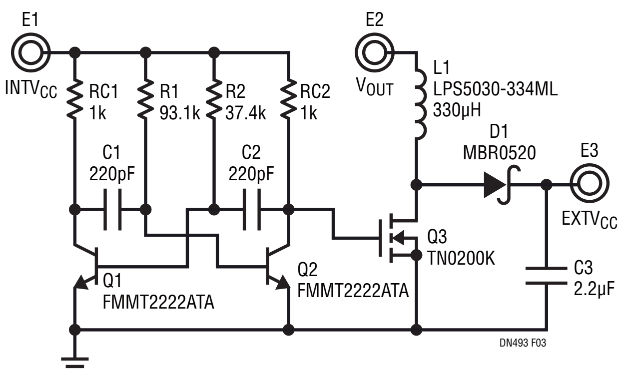

Figure 3. Boost Controlled By Astable Multivibrator Is Used for V_{OUT} Lower Than 2.5V

Conclusion

The efficiency of high input voltage DC/DC controllers can be significantly improved by using the controller's output voltage to power the IC, instead of allowing the internal LDO to produce the bias voltage. For input voltages above 30V, efficiency improvements of 2% to 3% are realized when a voltage doubler circuit is used for a 3.3V at 5A output (see Figure 4). Similar efficiency improvements are shown for a 1.8V at 7A converter with a multivibrator-based circuit.

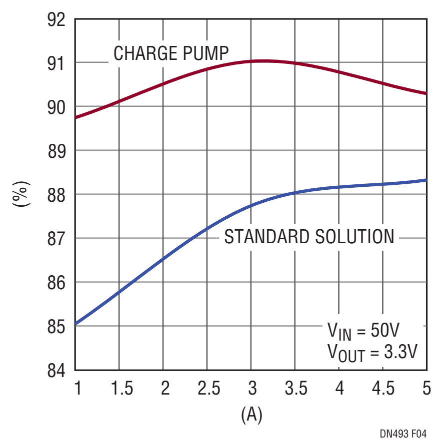

Figure 4. LTC3890/LTC3891 Efficiency Improvement

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high—that is, when switch S_1 is open—the Q output of IC_1 (first one-shot, pin 6) is low. This keeps IC_2, a 555 timer IC, disabled. Note that pin 6 also wraps around to pin 4 to form a nonretriggerable one-shot. The Q output of the second one-shot is also low at this time.

Closing switch S_1 turns on transistor Q_1, which grounds the low side of the solenoid coil and applies a low-going logic signal to the trigger input of the first one-shot (IC_1, pin 5). The Q output of IC_1 goes high for 470 msec and enables IC_2. IC_2 produces a rectangular waveform at its output (pin 3); through the voltage-doubler components (C_7, D_5, and D_4), C_8 is charged to approximately 24V dc.

After the first one-shot times out and $\overline{Q}$ goes high (pin 7), it triggers the second one-shot via the pin-12 input. This one-shot—also configured as nonretriggerable—produces a high-going pulse at its Q output (pin 10) of about 100 msec. This pulse turns on Q_3 and Q_2 and applies 24V dc to the high side of the solenoid coil. As C_8 discharges, the 24V decays to 12V dc, the steady-state voltage for the solenoid; D_3 supplies the steady-state voltage to the solenoid. **Figure 2** shows the voltage waveforms.

To turn off the solenoid, remove the control signal by opening S_1. This action turns off transistor Q_1 but has no effect on the one-shot circuits.

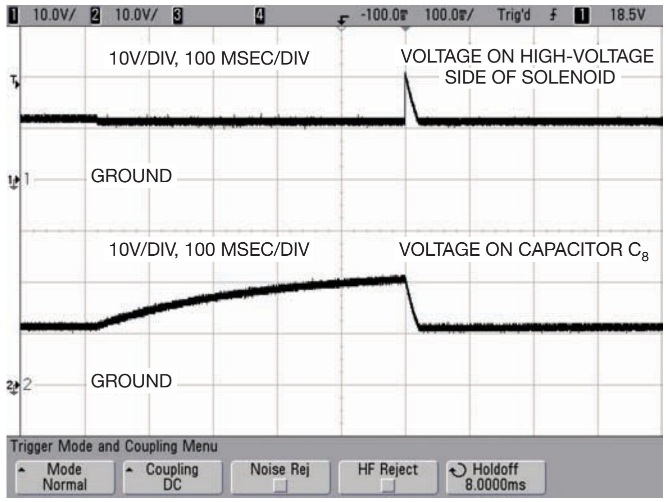


Figure 2 As C_8 discharges, the 24V decays to 12V dc, the steady-state voltage for the solenoid; D_3 supplies the steady-state voltage to the solenoid.

In applications where multiple solenoids are to be switched on sequentially, you can effectively use the circuit with slight modification. Also, you can easily modify the circuit shown for solenoids operating from dc voltages other than 12V. EDN

Injection-lock a Wien-bridge oscillator

Glen Brisebois, Linear Technology, Milpitas, CA

I recently had the opportunity to investigate a new micropower 6-MHz LTC6255 op amp driving a 12-bit, 250k sample/sec LTC2361 ADC. I wanted to acquire the FFT of a pure sinusoid of about 5 kHz. The problem is that getting the FFT of a pure sinusoid requires, well, a pure sinusoid. Most programmable signal generators, however, have fairly poor noise and distortion performance, not to mention digital "hash" floors, compared with dedicated op amps and good ADCs. You can't measure 90-dB distortion and noise using sources that are "60 dB-ish." So rather than try to find and keep an almost-ideal programmable signal generator, I decided to build up a low-distortion Meacham-bulb-stabilized Wien-bridge oscillator using an ultralow-distortion LT1468-2 op amp (**Figure 1**).

The lightbulb amplitude-stabilization technique relies on the positive temperature coefficient of the bulb impedance stabilizing the gain of the op amp to match the attenuation factor of 3 in the Wien bridge at its center frequency. As the output amplitude increases, the bulb filament heats up, increasing the impedance and reducing the gain and, therefore, the amplitude. I did not have immediate access to the usually called-for 327 lamp, so I decided to try a fairly low-power, high-voltage bulb, like the C7 Christmas bulb shown. At room temperature, it measured 316Ω; fresh out of the freezer (about –15°C), it measured 270Ω. Based on the 5W, 120V spec, it should be about 2.8k at white hot. That seemed like plenty of impedance range to stabilize a gain of 3, so I decided to linearize it a bit with a series 100Ω resistor.

For a gain of 3, the bulb plus 100Ω must be half of the 1.24k feedback (or equal to 612Ω), so the bulb must

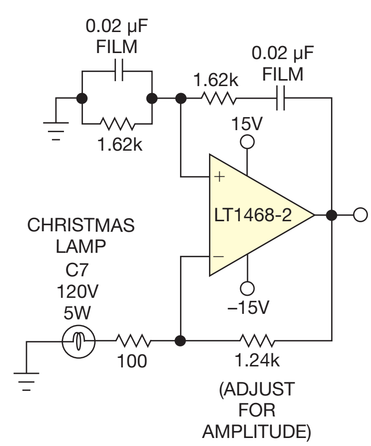


Figure 1 This Meacham-lightbulb-stabilized, low-distortion, low-noise 5-kHz Wien-bridge sinusoidal oscillator's RC feedback network attenuates by a factor of 3 at its midband. The bulb's self-heating forces a gain of 3 in the op amp.

settle at 512Ω. Roughly calculating a resistance temperature coefficient of

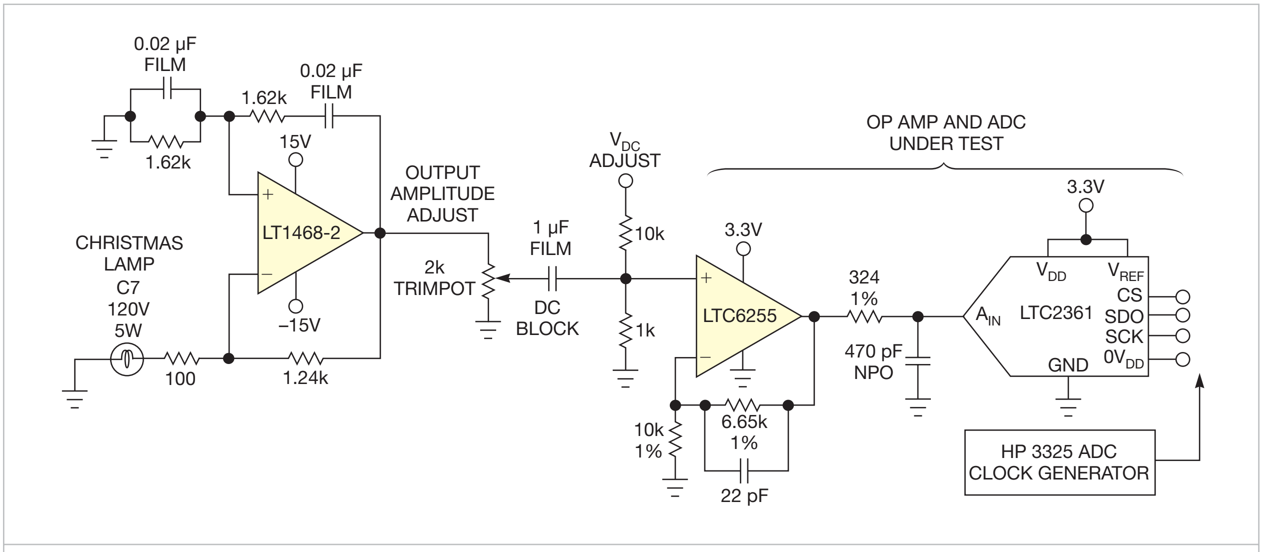


Figure 2 The Wien-bridge oscillator drives the op amp and ADC pair under test. The resulting FFT is clean after windowing, but not exceptional, as Figure 3 shows.

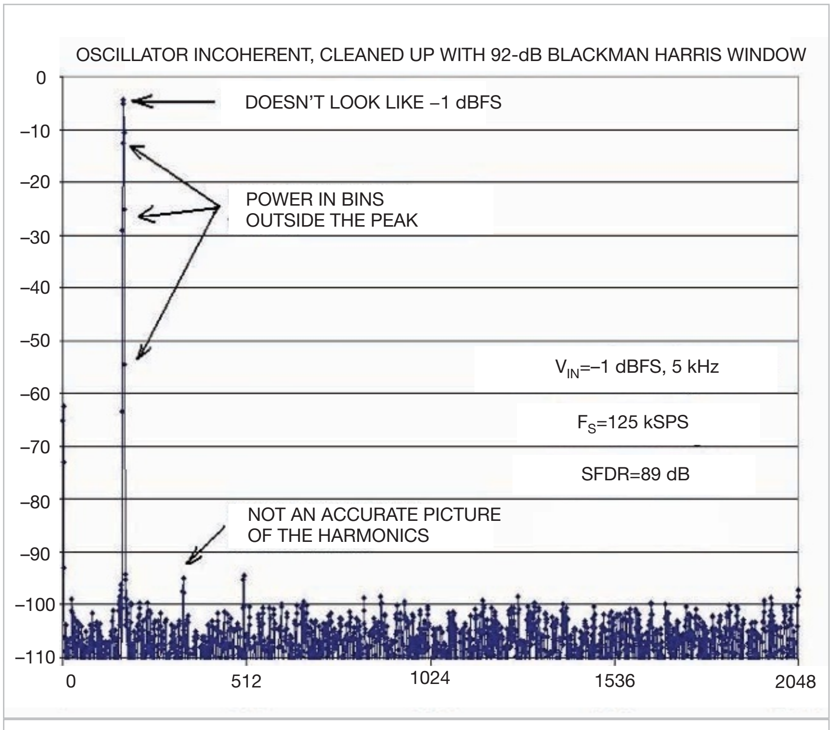


Figure 3 This 4096-point FFT was achieved using an unlocked oscillator with a 92-dB Blackman-Harris window. Note that the peak does not look like –1 dBFS and that there is power in the bins around the peak.

(316–270Ω)/[25–(–15°C)]=1.15Ω/°C means that the bulb filament will be about 195°C.

The oscillator powered up fine, giving a nice sinusoidal 5.15-kHz output at several volts, and independent measurements showed the second- and third-harmonic distortion products to be lower than –120 dBc. I applied the oscillator to the LTC6255 op-amp input after blocking and adjusting the dc level and ac amplitude, using the caps and pots as shown in **Figure 2**. The ac amplitude was adjusted for –1 dBFS, and the dc level was adjusted to center the signal within the ADC range. But, of course, this oscillator was purely analog and had no "10-MHz reference input" on the back to allow it to be synchronized with the ADC clock. The result is substantial spectral leakage in the FFT, so that it looks more like a circus tent than a single spike. Applying a 92-dB Blackman-Harris window to the data to reduce FFT leakage produced a fine-looking FFT (**Figure 3**).

Although this FFT is accurate in some ways, a closer inspection reveals some problems. For example, the input signal is –1 dBFS, but it certainly looks graphically lower than –1 dB down. The reason is that even an excellent windowing function leaves some of the fundamental power in the frequency bins adjacent to the main spike. The software includes these bins in its power calculations, and rightly so, but the fact is that the spike looks too low to make a good photograph.

The same can be said about the height of the harmonics; although they are calculated correctly and are accurate relative to the fundamental, they also look too low in absolute terms. So windowing is no substitute for a coherent phase-locked system.

When those objections were raised,


THEY SAY:
"ANALOG INTEGRATION CAN'T BE DONE."
TRANSLATION:
"UM...WELL, THAT SOUNDS LIKE A LOT OF WORK."

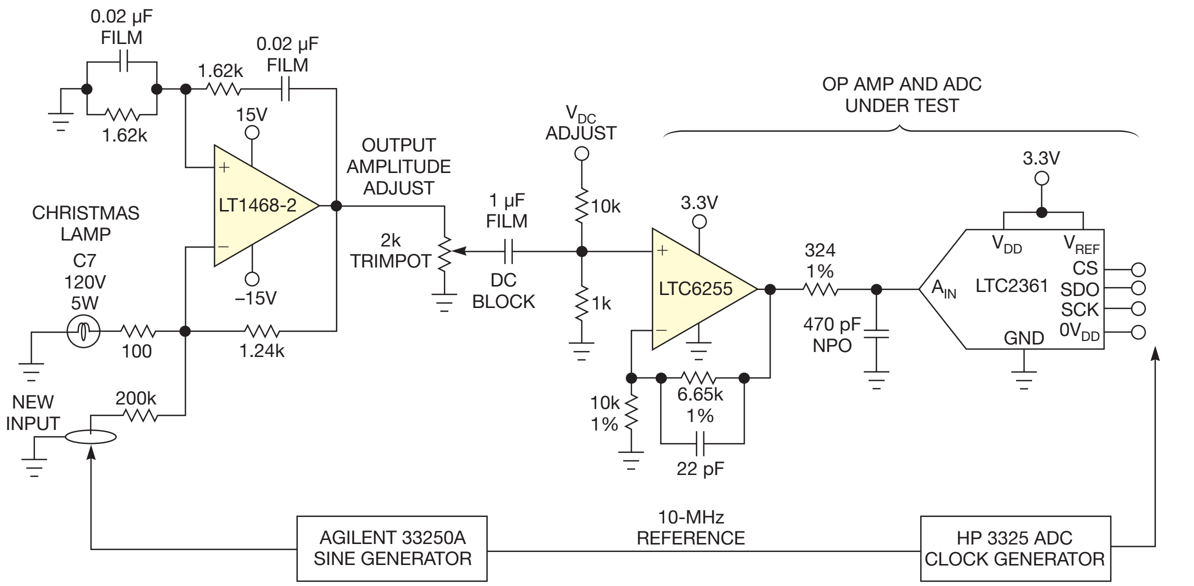


Figure 4 With the generators phase locked through the 10-MHz reference, the low-noise and -distortion Wien-bridge oscillator is gently nudged into coherence through the high-impedance, 200k resistor.

I despaired that I was going to have to return to the drawing board and maybe stay there, or find a locked oscillator with low distortion and noise or with awesome postfiltering. How could I ever make such a fundamentally analog oscillator coherent to an FFT bin in such an overwhelmingly digital environment? At 5 kHz, a passive filter with notches would be large and fussy. I thought of detuning the Wien-bridge oscillator by reducing the gain, thereby converting it into a filter.

But then it occurred to me that a gentle, analog sinusoidal nudge from a distorting but well-locked external oscillator might be enough to tweak the Wien-bridge frequency to where it needed to be. I decided to try injecting a sinusoid into the input of the Wien-bridge op-amp circuit, and opted to use a high series impedance to avoid simultaneously injecting noise and distortion. I came up with 200k—about 1000× the impedances already there—and put it in as shown on the left side of **Figure 4** (the "new input"). I set up the Agilent 33250A for a 5-kHz sine wave and applied it to the new input. Looking at both the 33250A and the Wien-bridge outputs with an oscilloscope, I slowly dialed up the 33250A frequency and was thrilled to finally see the sinusoids come "close" and then snap into lock.

I connected the 10-MHz back-panel references and changed the 33250A frequency to 5.157 kHz, the nearest coherent bin in the FFT. The sinusoids

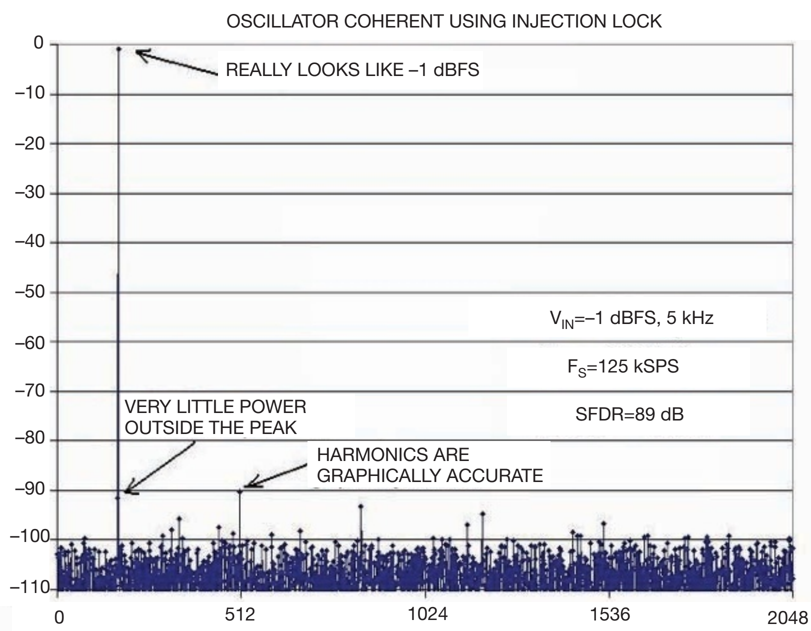


Figure 5 A more accurate FFT is obtained using the same Wien-bridge oscillator but with the frequency injection locked to a coherent 5.157 kHz using an HP33250A driving the 200k resistor at the "new input." Note that the peak is now visibly a believable –1 dBFS and that there is almost no power in the bins adjacent to the peak.

remained in lock, and the programmable 33250A generator successfully pulled the Wien-bridge oscillator slightly away from its natural frequency and into the desired frequency. The result was a nearly ideal FFT; all of the pertinent fundamental and distortion powers were situated in unique bins and were accurately represented (**Figure 5**).

Programmable sinusoidal generators often have excellent phase-noise characteristics and 10-MHz locking capabilities, but they also have high-output wideband noise floors and distortion. An FFT is sensitive to all of these forms of source corruption and also has a finite number of output bin frequencies. To test high-performance analog and mixed-signal systems, the right combination of classical Wien-bridge oscillators with programmable generators can provide a nearly perfect source with synchronous sampling, generating accurate FFTs. EDN

Convert your smartphone into a pedometer and tracking device

Ali Asgher and Abdus Sami, Sir Syed University, Karachi, Pakistan

When you go hiking or mountain biking, or simply take a long walk around the neighborhood, you might wonder about the distance you covered or specific details, such as speed. A specialized device for such a task is an expensive idea. Now, however, the increasing penetration of smartphones in the market with built-in GPS devices makes it possible to configure a mobile phone to log or send the current readings from its sensors to a server for viewing and processing.

This Design Idea describes a simple approach to log readings from a GPS using the Python scripting language. An advantage of Python is that an electronics engineer need not delve into the complex realm of C/C++ calls for Symbian/Android architectures to accomplish this simple task. All that is required is the installation on a phone of the Python interpreter, along with a text file containing the script.

The Python script initializes the mobile phone's GPS and records location and speed data periodically in a file. It can upload the information via GPRS (general packet radio service) or send it using SMS (short messaging service) to another mobile phone. A .NET application that runs on any PC with a mobile phone connected receives the SMS to track a user in real time on maps provided by Google Maps. In cases where the expense of a PC and receiving mobile would be extra, it's possible to import the tab-separated log file from the smartphone for manual data calculations.

The novelty of this idea, however, is in the use of a built-in accelerometer to calculate the number of steps taken when a user is walking or jogging and, based on this data, to calculate the amount of calories burned using one of many sample equations available (**references 1** and **2**). Hence, a total working pedometer and tracking system can be made using simple software in your smartphone without any additional hardware.

Figures 1 and **2** show two snapshots of the .NET application on the receiving PC. The app simply receives an SMS (with predefined format), parses it, displays the location/data on the map, and logs the information into a CSV file.

A few lines of code, available for download online at www.edn.com/4398333, enable the device to use its GPS for receiving its current location. A single line then sends the location data via SMS to the destination number. The destination can be connected to a PC for logging and is playing real-time data. The code writes all information to a file on the mobile phone itself, in case the SMS option is

Figure 1 The trackee's location is displayed just after he or she turns on the mobile application.

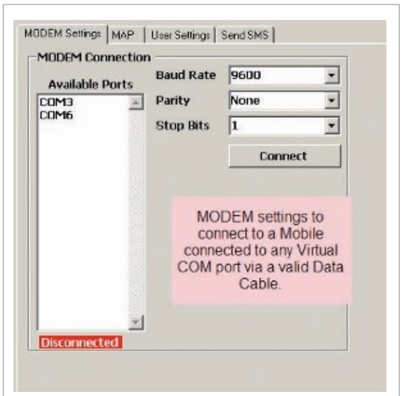


Figure 2 The user sets the COM port connection to the mobile device.

not required and all data needs to be on the device for later analysis. A flow chart shows the functions of the code listings (**Figure 3**).

Several components of the final design can be considered optional, as some users may want only the tracking app, and others might be content with a local file, without sending an SMS. EDN

REFERENCES

1 Scarlett, Jim, "Application Note AN-900: Enhancing the performance of pedometers using a single accelerometer," Analog Devices, 2007, http://bit.ly/TvjnLi.

2 "Pedometer Steps to Walking Calories and Distance Calculator," About.com, http://bit.ly/POkc3K.

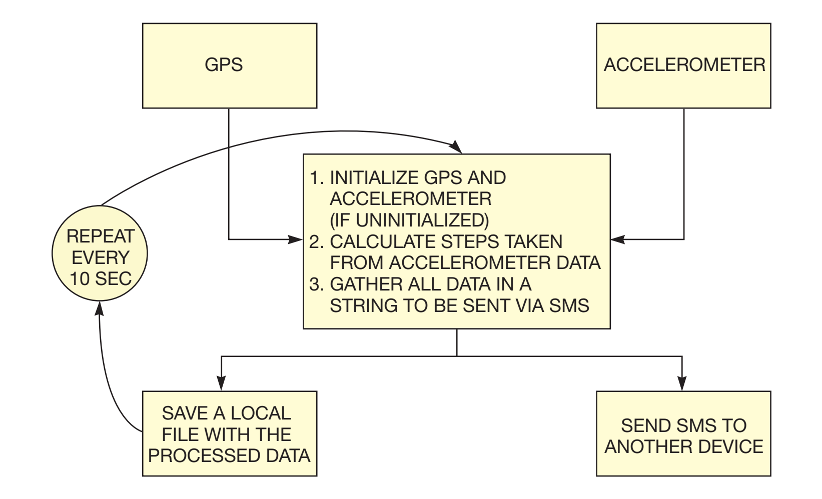


Figure 3 The code listings write and send the data and initialize the GPS.

Photo meter assesses ambient light

Raju Baddi, Tata Institute of Fundemental Research, Pune, India

Most PN-junction diodes can be used as photodiodes. While not optimized for this application, they do work. When the diode is reverse biased, it will produce a small photovoltaic output as the light level is increased. LEDs are particularly suited for this task because their housings are transparent.

You can construct a simple circuit that will assess the condition of ambient lighting and, because many LEDs' packages are tinted to enhance their emitted color, may even yield a reasonable evaluation of the detected color. The results are not as effective as those obtained using a high-quality optical filter, which typically has narrow bandpass characteristics, but they can be quite acceptable.

Though the design described here does not produce the accuracy of designs with laboratory-grade photodetectors and transimpedance amplifiers, it can be quickly assembled and will produce usable results at a low cost.

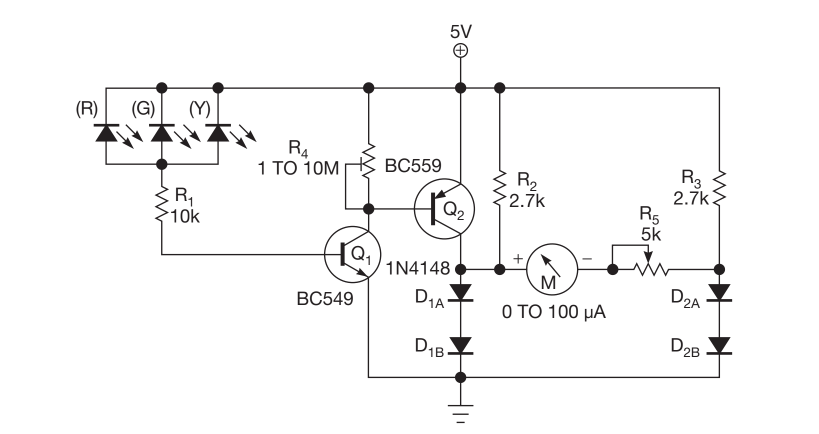


Figure 1 If the simplest version is required, use an inexpensive volume-unit meter to replace the 0- to 100-µA meter.

Three LEDs are used; experimentation will indicate which device has the best sensitivity to which color (**Figure 1**). The ambient light falling on the LEDs causes some current flow—typically in the range of 10 to 100 nA—through each LED, depending on the applied illumination level. This current flows through the base of a transistor, Q_1, and is amplified. Q_1's collector current then splits between potentiometer R_4, which acts as a first-stage gain calibration, and the base of Q_2.

Q_2 provides further amplification and drives the left side of a bridge circuit (D_{1A} and D_{1B}). Note that R_2/D_1 and R_3/D_2 form a balanced bridge. Q_2's collector current provides a slight imbalance to the bridge. The meter, M, measures this imbalance. R_5 adjusts the sensitivity of the meter.

Set R_4 and R_5 such that the meter has an appropriate deflection. R_4 is useful for selecting the quiescent point; R_5 is useful for adjusting the sensitivity.

Before building the circuit, check whether the LEDs can be used as photo sensors. To determine whether a given LED is a good photodiode, check the voltage across the LED using a common digital multimeter set to its most sensitive range—typically 200 mV. Typical output voltage should be approximately 0.3 to 1 mV with typical office illumination. EDN

Originally published in the Dec 23, 1993, issue of *EDN*

Postprocessing converts Spice to RF analyzer

Mojy C Chian, Harris Semiconductor, Melbourne, FL

Even though engineers designing IC and low-frequency products often use Spice to predict circuit-noise performance, designers of RF and high-frequency products have not been able to use Spice to determine RF-specific noise parameters. These engineers need a simulator that can predict noise figure at a given frequency, minimum noise figure, optimum reflection coefficient for noise, and noise resistance. Typically, these engineers use an RF simulator to determine the noise parameters.

But under the hood, both the Spice and RF simulators use the same noise-analysis algorithms and models. Thus, with a little postprocessing, you can transform the results of Spice noise analysis into terms familiar to an RF engineer.

As part of its noise analysis, Spice calculates the individual noise contributions (noise power spectral density, S_i, in units of V^2/Hz) from each noise generator (resistors and semiconductors) in the circuit. You can use this information to determine noise figure.

Noise figure (F) is a direct measure of signal-to-noise (S/N) ratio degradation caused by the circuit, or

$$F=(S/N)_{INPUT}/(S/N)_{OUTPUT}.$$

Another definition of noise figure is the ratio of the total available noise power at the output to the available noise power at the output that arises from input noise. Therefore, for a two-port network, if the noise-contribution components of the input and output resistors are SS and SL, respectively, then the noise figure is

$$F=10\log((ST-SL)/SS),$$

where ST is the sum of all noise components. If you must include the noise contribution of the load resistor in the two-port network's noise specification, then:

$$F=10\log(ST/SS).$$

Spice supplies SS, SL, and ST. A simple calculation, then, yields the noise figure for a specific frequency. For example, consider the Harris UHFN3 transistor in **Figure 1** simulated at 500 MHz. A Spice noise analysis produces the results in **Table 1**, yielding a noise figure of

$$F=10\log((4.75\times10^{-18}-5.0\times10^{-19})/2.5\times10^{-18})=2.3\text{ dB}.$$

Repeating the calculation for different frequencies produces a plot of noise figure versus frequency. You can easily extend this method to include other RF noise parameters. **EDN**

TABLE 1 SPICE NOISE-ANALYSIS RESULTS

Noise generators	Symbol	Noise contributions (V^2/Hz)
Source resistor	SS	2.5E–18
Load resistor	SL	5.0E–19
Total BJT	SQ	1.75E–18
Total	ST	4.75E–18

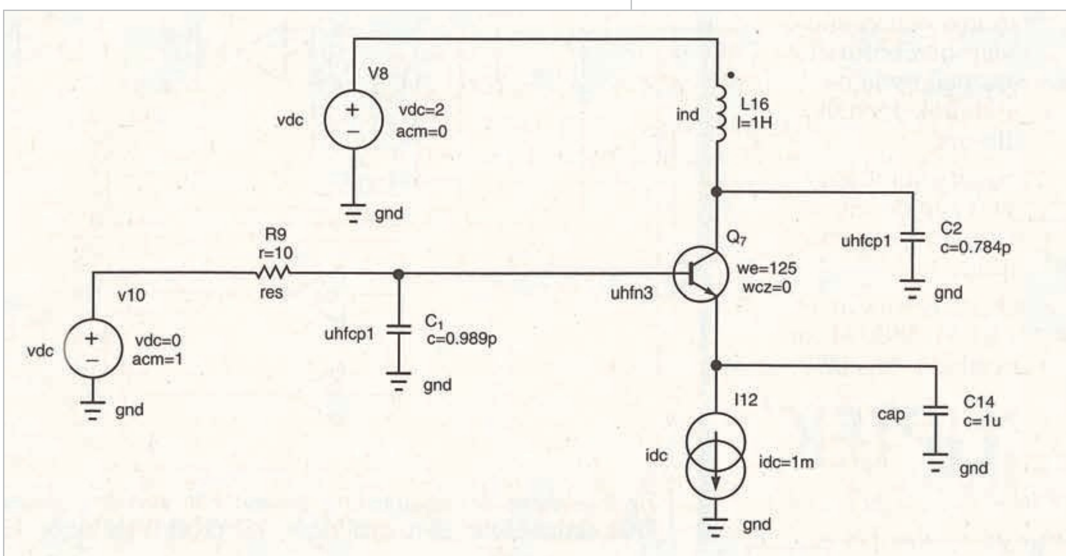


Figure 1 This Spice circuit can elicit noise parameters for the RF transistor being modeled.

supplychain

LINKING DESIGN AND RESOURCES

Integrating innovation into the supply chain

Few will dispute the notion that the Internet is an innovation. In the electronics supply chain, however, the Internet hasn't quite changed the game the way many expected.

In its heyday, the Internet was going to replace entire business models and enable buyers to bid for the components they needed. Inventory management was going to resemble the Amazon.com model. Entire BOMs could be matched to components with a single click. The possibilities were endless.

There are a number of reasons that those developments haven't panned out to the extent predicted. Chief among them is that buyers simply didn't want to change their habits.

It's not that buyers resist change altogether. Practices such as total quality management, just in time, and lean manufacturing have caught on with a vengeance. Procurement is always looking for ways to save costs.

But in high-volume, high-cost businesses such as electronics, buyers want to know where their inventory is. They want some level of pricing predictability before they place their orders. Most important, they don't want to give up the human relationships they have forged.

Two academic researchers, Martin Christopher and John Gattorna, found some commonalities among buying behaviors, which they outlined in a white paper published in 2005 in the *Journal of Industrial Marketing Management* (http://bit.ly/SUEbky). According to Christopher and Gattorna, the mix of four "dominant" buying behaviors—collaborative, consistent, dynamic, and innovative solutions—will vary across product and service categories as well as countries. The authors conclude that supply chains must align with customer behavior. An understanding of behaviors allows for the easy development of a pricing strategy by customer-segment type.

There are some upsides to the industry's refusal to move exclusively to the Web. The industry has changed drastically since the dot-com boom of the late 1990s. Components are becoming more complex as suppliers enter highly specialized, niche businesses. Designers are being asked to provide more designs with fewer resources. Meanwhile, economic uncertainty is making inventory management a risky business.

The Web plays a supporting role in all of these areas, but it is not the main player. Here's how the Web affects these aspects of the supply chain:

- **Suppliers.** Vendors can communicate a lot of information over the Internet, such as datasheets, schematics, and benchmarks. Most suppliers, however, also provide call-in centers to help engineers work out a problem.
- **Designers.** Engineers cull a lot of information up front and use the Web to compare a variety of components. There are also numerous design tools available online. Distributors, however, have hired more engineers to support customers who don't get direct help from suppliers. And the increased complexity of designs and devices has increased demand for person-to-person assistance.
- **Inventory management.** The Web provides a window into inventory prices and availability. OEMs, however, need to forecast demand as far out as possible; they can't rely on a last-minute order for 10,000 components. Many have preferred-pricing relationships. Long-term contracts and preferred pricing are still negotiated face to face.

Buyers are using the Web more extensively for a lot of things, but the Web-based activity is supplementary to most existing models, not a direct replacement. The Internet has changed the way the supply chain conducts business, but not in the way most pundits expected.

—by Barbara Jorgensen, *EBN* community editor

This story was originally posted by EBN: http://bit.ly/UfAm4z.

OUTLOOK

iPHONE 5 TO SPUR RECORD Q4 APPLE PHONE SHIPMENTS

The iPhone 5 will help to drive Apple's smartphone shipments in 2012 to 149 million units, up 60% from 93 million in 2011, according to IHS iSuppli. Most of the iPhone 5 sales bump will be seen in the final quarter, when it will combine with normal seasonality to yield what IHS predicts will be Apple's biggest quarter ever for iPhone sales.

"[The] iPhone 5 announcement comes as a significant departure from previous models," says Daniel Gleeson, mobile analyst for IHS. "The addition of a new, larger screen is a fundamental change in product design. Furthermore, the iPhone 5 is the first member of Apple's smartphone line to feature 4G [LTE] long-term evolution connectivity, accelerating data speeds dramatically."

The iPhone 5's support of global 4G LTE frequencies will help 4G get off the ground in many markets where uptake has been muted so far. Even in areas with poor 4G coverage, the iPhone 5 is expected to cause a spike in the usage of compatible devices, which should also be an incentive for wireless operators to build their networks faster.

—by Amy Norcross

productroundup

POWER SOURCES

On Semi Li-ion battery charger meets next-gen power-efficiency needs

On Semiconductor's NCP1851 fully programmable lithium-ion switching battery charger reduces charge time, increases battery life, and includes advanced startup features for optimized power efficiency in smartphones, tablets, and other handheld devices. With 1.6A charging capability, the device is sized at 2.2×2.55 mm for the latest USB-compliant input supplies and large battery capacities. It can complete a full charge cycle of a 1650-mAhr, 4.2V Li-ion battery in 90 minutes. Integrated dynamic power-path management enables instant system turn-on in case of a weak battery and helps replenish a deeply discharged battery. The NCP1851 is priced at $1.25 per unit (3000).

On Semiconductor, www.onsemi.com

Vicor offers integrated ZVS buck regulators in system-in-package

The high-efficiency, wide-input-range dc/dc ZVS (zero voltage switching) buck regulators in Vicor Corp's Picor PI33XX Cool-Power series integrate a controller, power switches, and associated support components in a high-density, low-profile system-in-package. The PI33XX requires only an external inductor and minimal capacitors to form a complete dc/dc soft-switching-mode buck regulator. The ZVS architecture enables high-frequency operation while minimizing switching losses and maximizing efficiency. Picor PI33XX-00-LGIZ Cool-Power ZVS buck regulators sell for $12.85 (1000).

Vicor, www.vicorpower.com

Linear Tech step-down dc/dc converter delivers 100% duty-cycle operation

The LT3504, a quad 1A-output, 40V step-down switching regulator with 100% duty-cycle operation, targets automotive and industrial applications requiring multiple outputs. It features a 3.2 to 40V input voltage range and has internal 1.5A switches that deliver up to 1A of continuous output current per channel to voltages down to 0.8V. The device minimizes the external-component count and delivers efficiencies of up to 88% over a wide input voltage range. Its current-mode topology enables fast transient response. Anti-phase switching reduces input ripple. The LT3504EUFD, in a QFN-28, sells for $3.50 each (1000); the LT3504IUFD sells for $3.85 each (1000).

Linear Technology, www.linear.com

iWatt 800V primary-side switcher adds accuracy to ac/dc power control

The iW1816 digital PWM driver, the latest in the iWatt AccuSwitch primary-side driver family, has an internal power switch rated to 800V for universal ac input and supports high-capacitance loads to 6,000 µF at up to 5W. The driver features adaptively controlled soft-start to support quick start-up at output voltages from 5 to more than 12V when driving a large capacitive load. It enables less than 100-mW system standby power, with close to

productroundup

50 mW at light load. The iW1816 targets smart meters, industrial-control applications, microwave ovens, and household appliances. The device is available in production quantities in a standard, low-cost seven-lead SOIC package. Samples are available. The price is 38 cents (1000).

iWatt, www.iwatt.com

TDK-Lambda touts power density of dc programmable supplies

TDK-Lambda's Z+ programmable dc power supplies are high-density, high-efficiency, 2U-format, benchtop and rack-mountable power supplies that target ATE, lab, and OEM applications.

The power supplies provide 400W of output power with an output-voltage range from 0 to 100V dc and output currents up to 40A. The Z+400 is 33% smaller and 40% lighter than the previous-generation ZUP series and similar products, thus providing a 49% increase in power density. Later this year, 200, 600, and 800W models will be added to the Z+ series. Pricing starts at $1460 each.

TDK-Lambda, www.tdk-lambda.com

Power Integrations switcher ICs deliver up to 90W

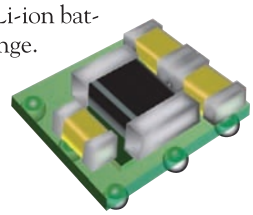
LinkSwitch-HP energy-efficient, off-line switcher ICs from Power Integrations can deliver up to 90W with accurate primary-side regulation. The ICs reduce component count by using innovative control algorithms and the

properties of the main power transformer and output diode—instead of optocouplers and related feedback circuitry—to determine the amount of power to deliver from the primary to the isolated secondary side. LinkSwitch-HP devices automatically select their control mode according to prevailing line and load conditions to optimize conversion efficiency and response to transient-load demands, while minimizing output ripple and audible noise. The devices come in eSIP-7C and eDIP-12B package options, starting at 42 cents each (10,000). Two supporting evaluation demo boards are available.

Power Integrations, www.powerint.com

TI dc/dc boost power module cuts board space requirements

The TPS81256 ultrasmall boost power module, integrating an inductor and I/O capacitors, measures less than 9 mm^2 and less than 1 mm in height, saving up to 50% more board space over competing solutions, according to Texas Instruments. The power module addresses the needs of smartphone and tablet designers for smaller point-of-load converters with long battery runtimes and high power-conversion efficiency. The 4-MHz, 600-mA module supports a 5V output with a power density of 400 mW/mm^2. It reduces supply current to 43 µA during light-load operation and achieves power efficiency of more than 90% from an input voltage of 2.5V, efficiently managing 3W over a full Li-ion battery voltage range. Pricing is $1.70 each (1000).



Texas Instruments, www.ti.com

Traco fields high-power, ultracompact dc/dc converter modules

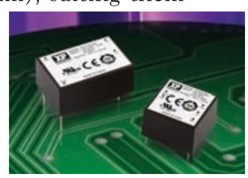
The high-power dc/dc modules in Traco Power's TEP 75-200 series offer output power from 75 to 240W. The modules are packaged in a

sealed metal case with an aluminum baseplate and an optional heat sink that allows full load operation up to 60°C with convection cooling. The products feature 2:1 or 4:1 wide input-voltage ranges, efficiency up to 93%, undervoltage lockout, and reverse-input-voltage protection. Delivery times range from stock to 10 weeks; prices range from less than $100 to $315 in OEM quantities, depending on the wattage and options chosen.

Traco Power, www.tracopower.com

XP Power adds mini 5 and 10W power supplies

The miniature, encapsulated, board-mount 5W single-output ac/dc power supplies in XP Power's ECE05 series measure 1×1×0.6 in. (25.4×25.4×15.24 mm), suiting them for end-product designs in which available board space is at a premium. Complementing the ECE05 series,



the ECE10 series provides 10W output from an encapsulated package measuring 1.5×1×0.6 in. (38.1×25.4×15.24 mm). Both series comprise seven models covering nominal output voltages from 3.3 to 48V dc, from a universal input of 85 to 264V ac with Class II construction, meaning no earth or ground connection is required. The ECE05 is priced at $14.82 (500) and the ECE10 is priced at $21.06 (500).

XP Power, www.xppower.com

CUI digital POL modules set optimum stability in real time

The NDM2P series from CUI Inc is the company's second generation of digital point-of-load dc/dc modules for distributed-power-architecture applications. The modules offer true cycle-by-cycle compensation, autonomously balancing the trade-offs between dynamic performance and system stability in real time as conditions change. Offering efficiencies above 93% at half load, the NDM2P series is initially available in three compact DIP configurations: the 12A NDM2P-12, priced at $9.98; the 25A NDM2P-25, priced at $14.20; and the 50A NDM2P-50, priced at $19.80 (OEM quantities). **CUI, www.cui.com**

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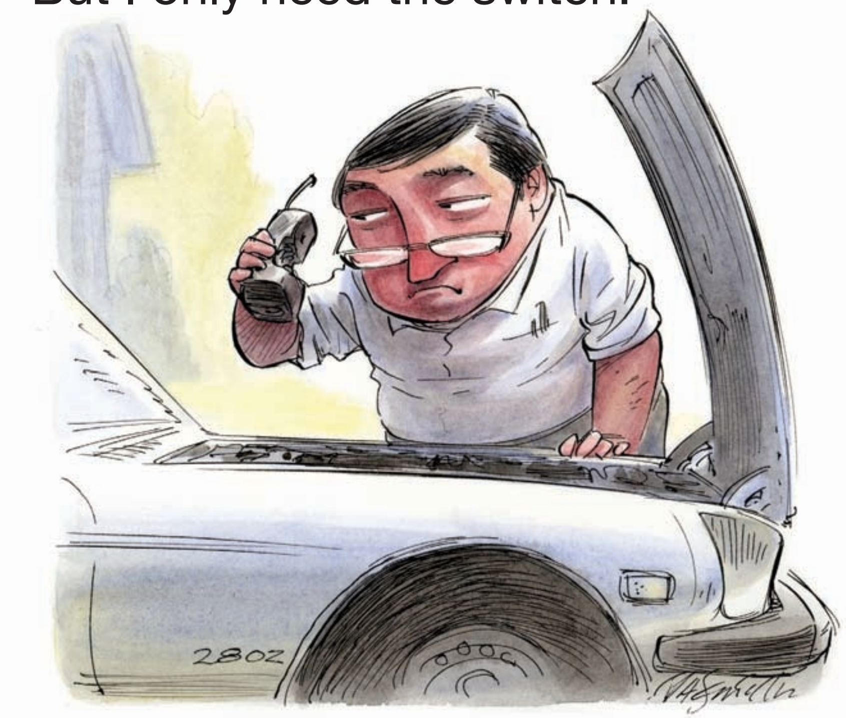

Not all engineering challenges occur at work; often, an engineer needs to bring his troubleshooting skills home with him. I learned that lesson firsthand when, during the late 1970s or the early 1980s, my wife's automobile started acting up.

The car was a Datsun (now Nissan) 280Z. It had been very reliable and well maintained, but it had started to act up intermittently—and as any engineer will tell you, intermittent problems are the hardest to diagnose.

The first time the problem occurred, the car stalled as if it had run out of gas. My wife turned the ignition switch off and then back on to restart the car; it restarted fine, and she was able to get home. I took a look at the car but couldn't find anything wrong. I thought the fuel filter might be dirty, so I changed it to eliminate that as a possible cause.

After that, my wife drove the car for many weeks without a recurrence of the problem; but then out of the blue, just as it had done the first time, the engine stopped as if it had run out of gas and then restarted just fine. Again, I checked the car but found nothing suspicious.

My wife drove the car without incident for a few more weeks before the car stalled again. It became clear that an apparently random event had a real root cause; I just hadn't found it yet.

My wife and I traded cars, and I drove hers for a few weeks before I stalled just as she had. I got out the auto manual. After studying the wiring diagram, I connected a voltmeter to some points under the dash and sat the voltmeter on the console so I could keep an eye on it.

I drove that car for months, monitoring and recording the voltages. Periodically, I would switch the voltmeter to a different point to collect more data. I drove with no problems through the winter and spring; then one hot summer day, the engine suddenly stalled, and I noticed that the voltage was only 6V on one of the relay coils. Finally, I was getting somewhere. Consulting the wiring diagram and all the data I had collected, I determined that the voltage loss was through switch contacts in an airflow meter.

The airflow meter was simply a spring-loaded flap connected to the switch contacts and mounted in the air-intake path. With the engine running and air flowing into the intake manifold, the flap is open and the switch contacts are closed; if the driver gets into an accident and the engine stalls, the airflow will stop, the spring will close the flap, and the switch contacts will open. The switch provides the voltage to a relay, which in turn controls the fuel pump. When the airflow stops, the switch will open, the relay will open, and the fuel pump will stop, causing the engine to "run out of gas." This safety feature ensures that fuel will not be sprayed onto a hot engine in the case of an accident.

The switch in our car dropped enough voltage to barely pull in the relay, and in the heat of summer the relay had an even harder time pulling in. Since all the wiring looked OK, I concluded that the switch contacts had to be dirty or corroded. I temporarily wired in an external toggle switch to bypass the airflow-meter switch; this applied the full 12V to the fuel-pump relay coil and kept the car running, and confirmed that the airflow-meter switch was the problem.

When I called the Datsun dealership to buy a replacement switch, the dealer told me I would have to replace the entire airflow-meter assembly, as it was a sealed unit and not repairable. The cost was about $500 just for the assembly. But I only needed the switch!

Never tell an engineer that something cannot be repaired. I got my utility knife, slit the cover seal, and removed the cover. There was the switch, with its dirty, pitted contacts. I cleaned the contacts, put the cover back on, and sealed the assembly with RTV. I then measured the full 12V on the relay coil. Intermittent problem solved. EDN

Walter Sjursen is a research engineer at Bose Corp (Framingham, MA). He holds a master of science degree in engineering science from The Pennsylvania State University.

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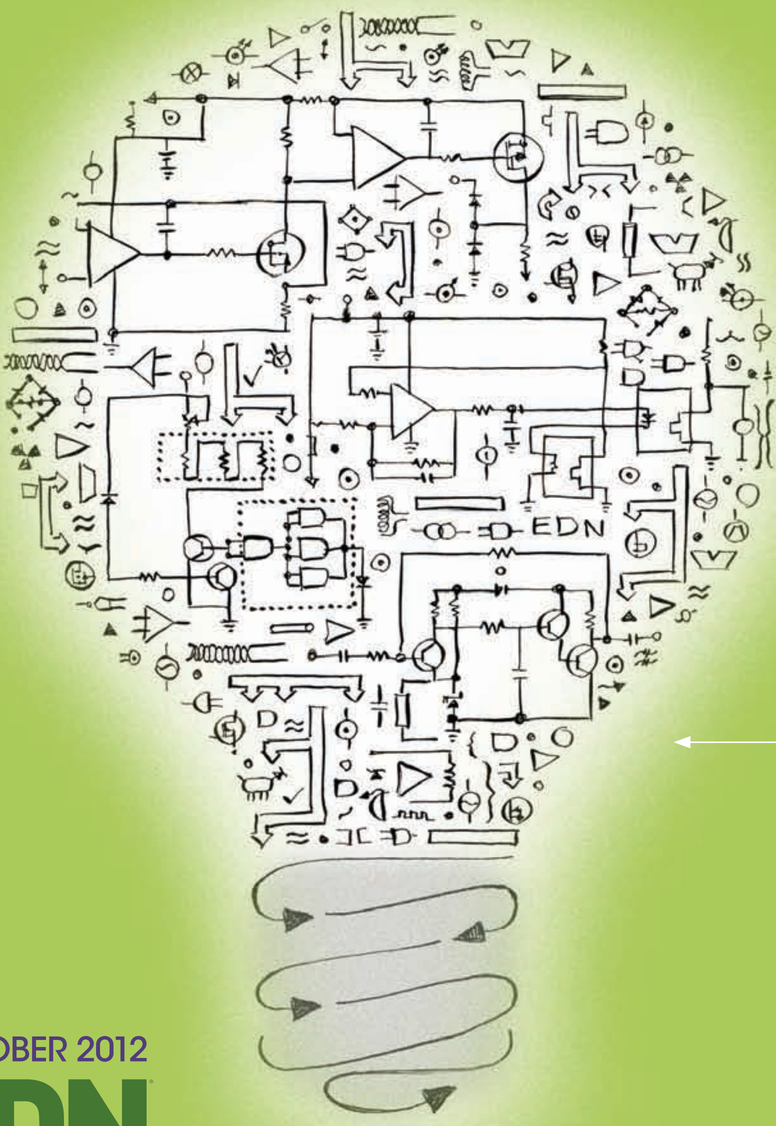

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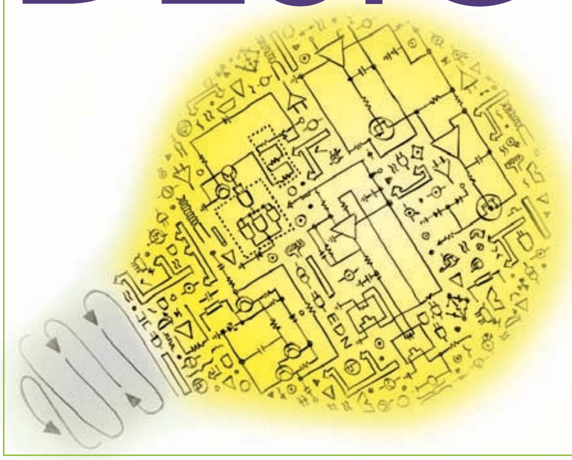

A SPECIAL SUPPLEMENT TO *EDN*

COVER IMAGE: DANIEL VASCONCELLOS

the best of DESIGN IDEAS

"IDEAS ARE WHAT EVERY ENGINEERING ORGANIZATION HAS IN COMMON," OUR FIRST EDITOR, MILTON SOL KIVER, WROTE BACK IN 1956. HOW INTERESTING THAT, 56 YEARS LATER, ENGINEERS STILL HAVE THE SAME HUNGER FOR DESIGN IDEAS.

I recently had the opportunity to see *EDN*'s print archives. The vault area, housed in our Bedford, MA, office, stores original copies that date back to issue No. 1, published as *Electrical Design News* on May 8, 1956. I was six years old when *EDN* debuted.

As I sat down and leafed through the 122-page first edition, the first piece that caught my eye was the editorial by Milton Sol Kiver, the publication's first editor and the author of *Transistors in Radio, Television, and Electronics*, published by McGraw-Hill in 1959.

"We are beginning what we believe will be a helpful service to electrical design engineers," Kiver wrote. " 'What,' we asked, 'would you desire most to see in an electrical publication?' The response was as direct as it was unanimous … a magazine of design ideas."

The editorial continues: "No engineer, we found, can ever get enough good ideas. Ideas represent the most important piece of property in every engineering department, whether it be concerned with the evolution of fantastically complex and intricate computers or merely a simple, two-piece widget that sells for 18 cents. Ideas are what every engineering organization has in common—and will continue to have in common for as long as they remain in business."

The aim of *Electrical Design News*, Kiver wrote, was "to provide you with a maximum of ideas which will help you solve present or future problems or perhaps suggest methods of approach that were never even considered."

How interesting that, 56 years later, engineers still have the same need and hunger for Design Ideas. As the new Design Ideas editor, as well as a longtime *EDN* reader, I truly value their content. Ever since I graduated from New York University's School of Engineering in 1972, I have been tearing out Design Ideas and putting them in folders for near- or far-term use as references for my designs.

Design Ideas—community driven, and offering inspired, hands-on, practical, useful circuit-design contributions—have always resonated deeply with *EDN*'s audience. To highlight those contributions, and the engineers behind them, we collected the most popular Design Ideas published since January 2011 in six categories—Analog, Components and Packaging, LEDs, Power, Systems, and Test and Measurement—and in late August asked our online readers to vote for their favorites. You responded in force. The pages that follow include our Readers' Choice in each category, as well as a collection of other popular Design Ideas.

As always, you can find many more Design Ideas online at www.edn.com/designideas. You might even want to share a Design Idea of your own with the *EDN* community. For information on that process, take a look at page 26 of this supplement, or go to www.edn.com/4394666.

Steve Taranovich,
Senior Technical Editor, **EDN**

READERS' CHOICE

How to recover a pulse signal with a large capacitance load

Chenan Tong, Texas Instruments

In some applications, it is necessary to transmit square waves across a long cable. Long cables, however, typically have high capacitance, which can significantly affect the signal's wave shape. As such, the signal's frequency and duty cycle need to be maintained if the signal is to remain free from distortion. This Design Idea discusses this phenomenon and offers a simple solution.

Figure 1 illustrates a common solution used to reconstruct a square wave at the end of a long cable (47-pF cable capacitance). V_{IN0} is the signal to be transmitted. The signal at V_{IN1} represents the signal at the end of the cable. You can see that this signal is distorted by the charge and discharge of the parasitic capacitance of the cable. Furthermore, the gate (IC_2) sees the rising and falling edges differently, so the reconstructed output signal will not be an accurate representation of the original digital signal.

The results in **Figure 2** show that you cannot recover input pulse with a simple logic gate. You need to find a different method to detect the rising and falling edges of the digital circuits. A differentiator can be used to detect the square-wave edges because the output of the RC circuit rises after the rising edge and falls after the falling edge of the square wave. Remember that the differentiator output is proportionate to the rate of change of the output signal, so it moves positively for increasing signals and negatively for decreasing signals.

The design in **Figure 3** uses a differentiator. **Figure 3** also shows the simple gate solution (IC_2) for comparison. In this example circuit, you can see how the simple gate solution does not effectively solve the problem. Note that the signal at V_{IN1} is from the charging and discharging of C_2 times R_6. In this

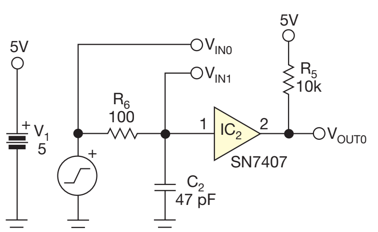

Figure 1 Shown is a common pulse-reconstruction solution.

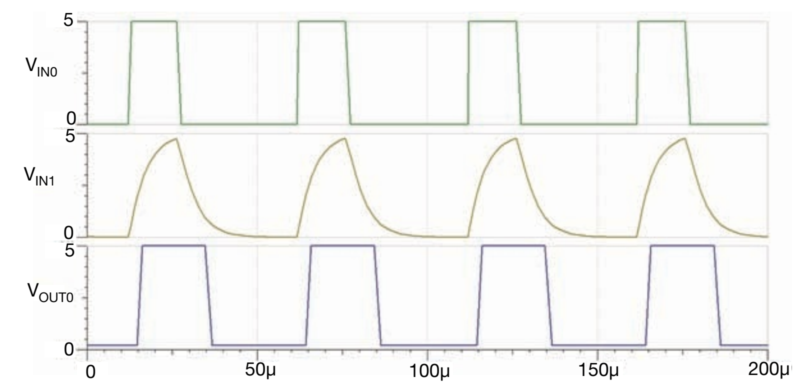

Figure 2 Simulation results for the common pulse reconstruction show that you cannot recover the input pulse with a simple logic gate.

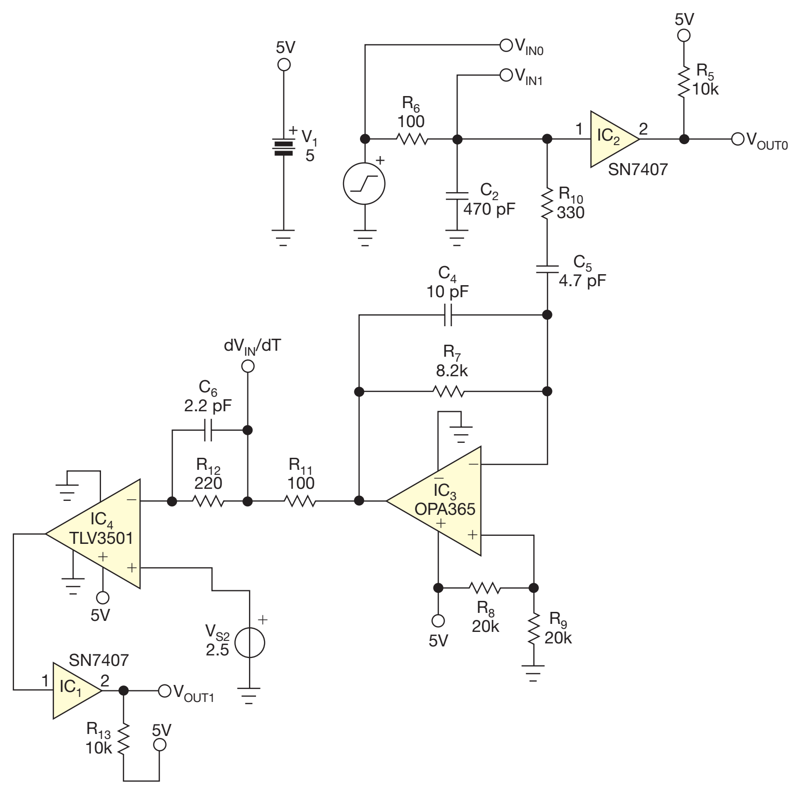

Figure 3 By differentiating the RC signal, you can reconstruct a signal that more closely resembles the original square wave.

example, C_2 is 470 pF, or 10 times larger than the example in **Figure 1**. When the input pulse is high (after the rising edge), the capacitor voltage increases. The differentiator output is negative for increasing capacitor voltage. When the input pulse is low (after the falling edge), the capacitor voltage decreases. The differentiator output is positive for increasing capacitor voltage.

Thus, by differentiating the RC signal you can reconstruct a signal that more closely resembles the original square wave. A comparator follows the differentiator output to create a sharp square-wave output.

Figure 4 shows the simulation results for the circuit in **Figure 3**. The input signal is a 20-kHz square wave with a duty cycle of 20%. The output of IC_2 clearly does not reproduce the original signal. In fact, IC_2 does not even detect most of the pulses. The differentiator's output looks like a smoothed inversion of the original digital signal. The comparator converts the differentiator output to a sharp square wave that accurately matches the frequency and duty cycle of the original signal. Specifically, the overall error in the duty cycle for this example is approximately 10%.

With this circuit, you can easily implement pulse recognition after a long cable and heavy capacitance load. This method produces pulse transmission with low distortion so that the frequency and duty cycle of the original signal are preserved. EDN

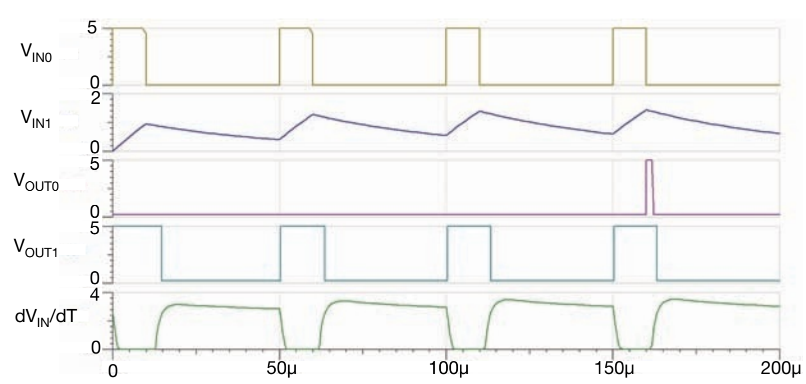

Figure 4 In these simulation results for differentiator-plus-comparator reconstruction, the differentiator output looks like a smoothed inversion of the original digital signal.

ACKNOWLEDGMENT

Special thanks to Arthur Kay and Matthew Hann of Texas Instruments for contributing their technical expertise in this subject area.

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Simple reverse-polarity-protection circuit has no voltage drop

Aruna Prabath Rubasinghe, University of Moratuwa, Moratuwa, Sri Lanka

Common methods of reverse-voltage protection employ diodes to prevent damage to a circuit. In one approach, a series diode allows current to flow only if the correct polarity is applied (**Figure 1**). You can also use a diode bridge to rectify the input so that your circuit always receives the correct polarity (**Figure 2**). The drawback of these approaches is that they waste power in the voltage drop across the diodes. With an input current of 1A, the circuit in **Figure 1** wastes 0.7W, and the circuit in **Figure 2** wastes 1.4W.

This Design Idea suggests a simple method that has no voltage drop or wasted power (**Figure 3**).

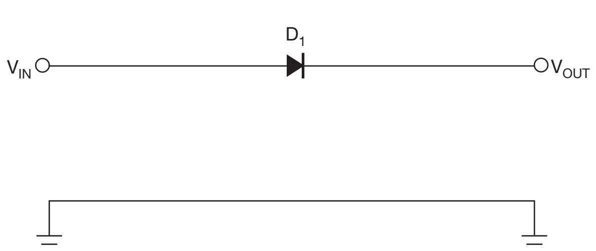

Figure 1 A series diode protects systems from reverse polarity but wastes power in diode losses.

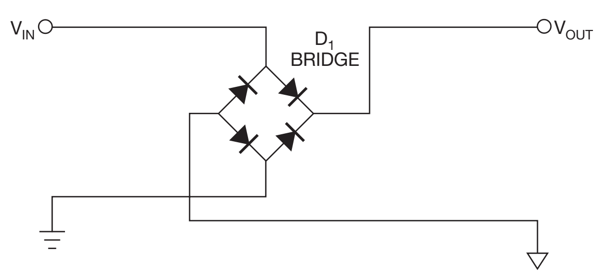

Figure 2 You can use a bridge rectifier so that your system works no matter what the input polarity is. This circuit wastes twice the power, in diode losses, of the circuit in Figure 1.

Select a relay to operate with the reverse-polarity voltage. For example, use a 12V relay for a 12V supply system. When you apply correct polarity to the circuit, D_1 becomes reverse-biased, and the S_1 relay remains off. Then connect the input- and output-power lines to the normally connected pins of the relay, so current flows to the end circuit. Diode D_1 blocks power to the relay, and the protection circuit dissipates no power.

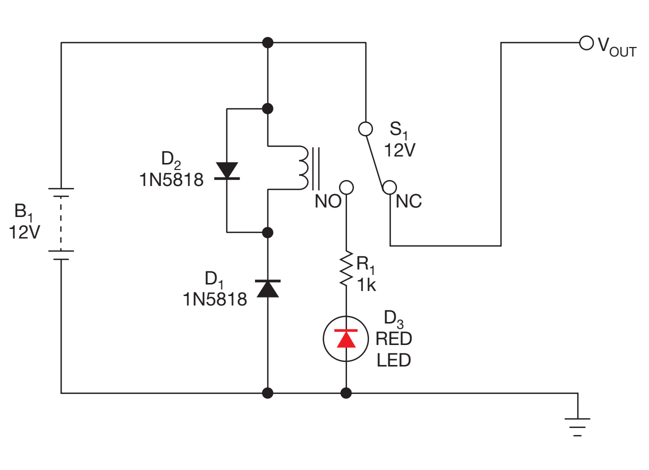

Figure 3 You can wire a relay switch to pass power to your system with no power loss. D_2 clamps inductive kicks from the relay coil.

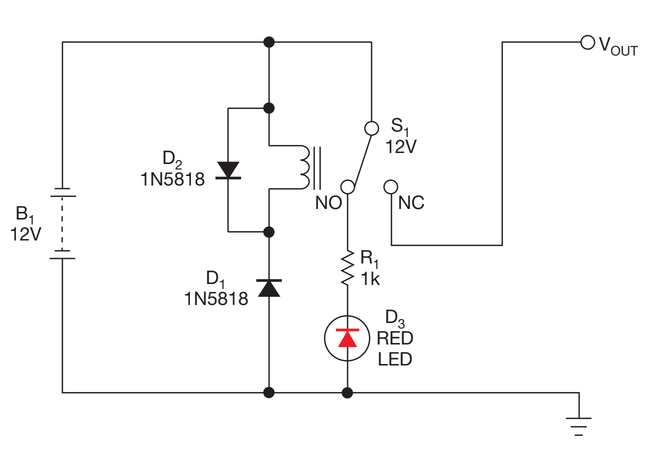

Figure 4 With reversed input voltage, the relay switch engages, interrupting power to the system, and the LED lights.

When you apply incorrect reversed polarity, diode D_1 becomes forward-biased, turning on the relay (**Figure 4**). Turning on the relay cuts the power supply to the end circuit, and red LED D_3 turns on, indicating a reverse voltage. The circuit consumes power only if reverse polarity is applied. Unlike FETs or semiconductor switches, relay contact switches have low on-resistance, meaning that they cause no voltage drop between the input supply and the circuit requiring protection. Thus, the design is suitable for systems with tight voltage margins. EDN

Obtain a gain of 450 from one vacuum tube

Lyle Russell Williams, St Charles, MO

A direct-conversion radio receiver required an audio gain of 450 from a pentode vacuum tube. A pentode has a high transconductance—that is, the ratio of the change in plate current to the change of the control grid voltage that caused it. To get high gain, however, it needs a high load impedance. RF applications with pentodes often used LC-tuned circuits in their plate loads in which the impedance at resonance and, therefore, the gain is high. It is typically impossible to implement a high load impedance using an untuned circuit because of the dc requirements of the tube.

RF APPLICATIONS WITH PENTODES OFTEN USED LC-TUNED CIRCUITS IN THEIR PLATE LOADS.

For instance, a 6AU6 pentode vacuum tube needs a quiescent plate current of approximately 5 mA (**Figure 1**). If the quiescent dc plate voltage is to be 60V, the load resistance must be no more than 12 kΩ. The 0.5-MΩ plate resistance of the tube and the 1-MΩ load of the next stage are negligible with respect to the 12-kΩ load. With a transconductance of 3900 microsiemens, those requirements demand an audio gain of 45. You can easily achieve this gain with a triode tube.

To get a high load impedance with an untuned plate circuit, you can use a transistor current source for the tube (**Figure 2**). The transistor has no gain but functions as an active load for the tube and supplies the 5-mA plate current. You adjust the 500Ω potentiometer to obtain 60V dc at the plate. The gain of the circuit is approximately 450. This gain implies a 150-kΩ load impedance that the transistor supplies in parallel with the plate resistance and the resistance of the next stage. Alternatively, you can use two triode tube circuits in series, each having a gain of 21. EDN

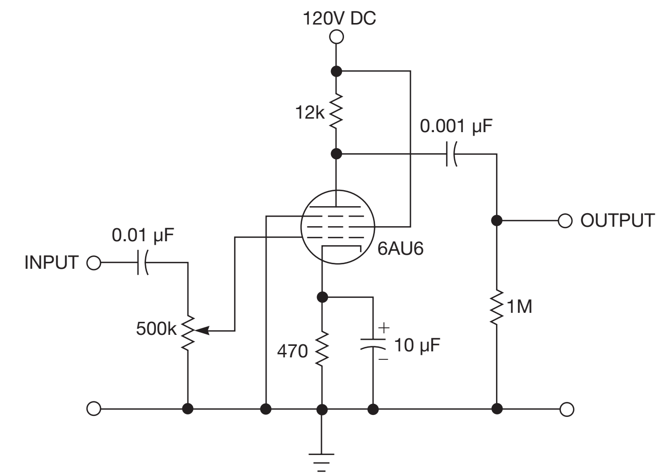

Figure 1 A 6AU6 pentode vacuum tube needs a quiescent plate current of approximately 5 mA.

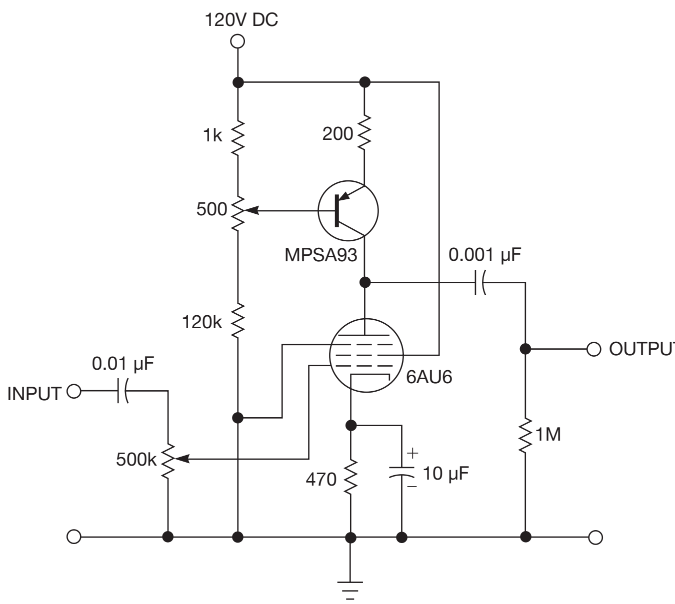

Figure 2 To get a high load impedance with an untuned plate circuit, you can use a transistor current source for the tube.

READERS' CHOICE

Build an op amp with three discrete transistors

Lyle Russell Williams, St Charles, MO

You can use three discrete transistors to build an operational amplifier with an open-loop gain greater than 1 million (**Figure 1**). You bias the output at approximately one-half the supply voltage using the combined voltage drops across zener diode D_1, the emitter-base voltage of input transistor Q_1, and the 1V drop across 1-MΩ feedback resistor R_2.

Resistor R_3 and capacitor C_1 form a compensation network that prevents the circuit from oscillating. The values in the **figure** still provide a good square-wave response. The ratio of R_2 to R_1 determines the inverting gain, which is –10 in this example.

You can configure this op amp as an active filter or as an oscillator. It drives a load of 1 kΩ. The square-wave response is good at 10 kHz, and the output reduces by 3 dB at 50 kHz. Set the 50-Hz low-frequency response with the values of the input and the output capacitors. You can raise the high-frequency response by using faster transistors and doing careful layout. EDN

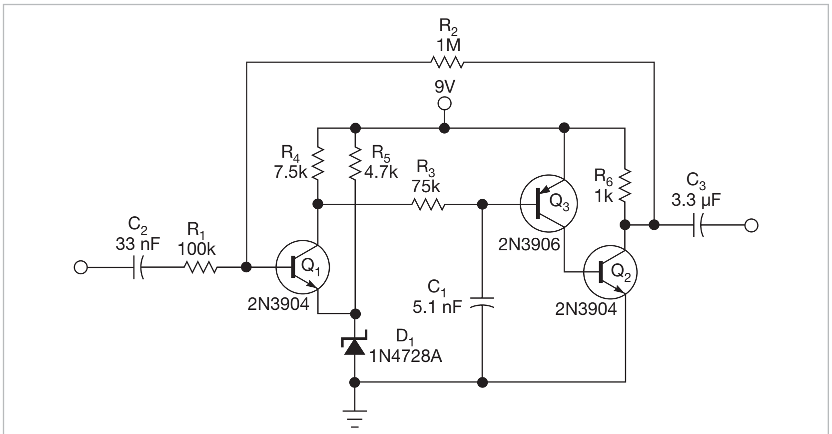

Figure 1 This ac-coupled inverting op amp has an open-loop gain of 1 million. R_1 and R_2 set a closed-loop gain of –10.

Automatic night-light feeds directly from the ac line

Abel Raynus, Armatron International Inc, Malden, MA

There are many approaches to the problem of activating a light when it becomes dark, and a recent Design Idea covers this topic (**Reference 1**). Some approaches require a dc power supply and an electromechanical relay, but a better approach involves feeding the device directly from the ac line, minimizing the number of components (**Figure 1**).

The heart of the device is a light-sensitive cadmium-sulphide resistor, P_R, with a resistance of approximately 200 kΩ in the dark, decreasing to a few kilohms in the light. P_R and capacitor C_1 form an ac-voltage divider. In daylight, the voltage across P_R is too low to generate the required gate-trigger current to turn on bidirectional ac switch Q_1, thus keeping the load—usually a lamp—off. When it becomes dark, P_R's resistance rises, resulting in an increase in the TRIAC's gate current that triggers the TRIAC and lights the lamp.

The circuit uses inexpensive, off-the-shelf components, including the VT90N1 photoresistor; a 0.1-µF, 275V capacitor; and an L2004F61 TRIAC with a load current of 4A rms, a peak blocking voltage of 200V, and a gate-trigger current of 5 mA. The exact specifications of these components are not critical; you could use others instead.

Editor's note: Attributes worth mentioning include the fact that the capacitor introduces a phase shift, which places the peak of the gate voltage close to the zero crossing of the load's sine wave for optimum turn-on timing. Another benefit is thermal hysteresis, which occurs due to the reduction of the required triggering voltage and current as the TRIAC warms up after the initial turn-on. EDN

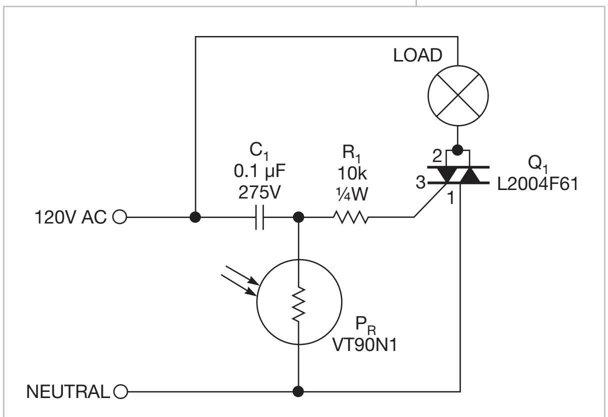

Figure 1 The photoresistor activates the TRIAC and the load when darkness falls.

REFERENCE

1 Tran, Chau, "Simple night-light uses a photoresistor to detect dusk," *EDN*, Dec 15, 2011, pg 49, http://bit.ly/HPi1GG.

Use a transistor as a heater

REC Johnson, B Lora Narayana, and Devender Sundi,
Center for Cellular and Molecular Biology, Hyderabad, India

It is common to use transistors for driving resistive heating elements. However, you can use the heat that a power transistor dissipates to advantage in several situations, eliminating the need for a separate heating element because most transistors can safely operate at temperatures as high as 100°C.

A typical example is in a biological laboratory, in which maintaining the temperature of samples in microliter-sized cuvettes is a common requirement. The space/geometry constraint and the <100°C upper-temperature limit are the basic factors of the idea.

You can use an N-channel IRF540 MOSFET to directly heat and control the temperature of a biological sample from ambient to 45°C. **Figure 1** shows a simple on/off-type control circuit in which an LM35, IC_1, is the temperature sensor, whose output a DPM (digital panel meter) can display. IC_2 compares the voltage that VR_1 sets with the output of the LM35 to turn on Q_2 accordingly, with the positive feedback through R_9 providing a small amount of hysteresis. S_1 switches the DPM between a set value and the actual temperature readout. You derive the reference voltage from a TL431 shunt regulator (not shown). The LED lights up when Q_2 is on.

IC_1 and Q_2 thermally mount on the metal block that forms the sample holder; use thermal grease on both components for maximum heat transfer. Note that the mounting tab of the TO-220 package electrically connects to the drain, and you may need to insulate it from the cuvette with a thermal pad. Setting bias control VR_3 for a Q_2 current of 270 mA is sufficient to hold the cuvette at 45°C.

Be sure to set VR_3 to minimum power during initial power-up; if you set it for maximum power, you could apply 24V to Q_2's gate-to-source voltage, which is rated for a maximum of only 20V. You can extend the temperature range by changing the voltage divider comprising R_1, R_2, and VR_1. The design includes a safety cutoff circuit (not shown) in case the temperature gets too high.

YOU CAN USE THE HEAT THAT A POWER TRANSISTOR DISSIPATES TO ELIMINATE THE NEED FOR A SEPARATE HEATING ELEMENT.

Various other options are also possible applications for this circuit. These applications include linear control, pulse-width modulation, and the use of a PID (proportional-integral-derivative) controller, to name a few. EDN

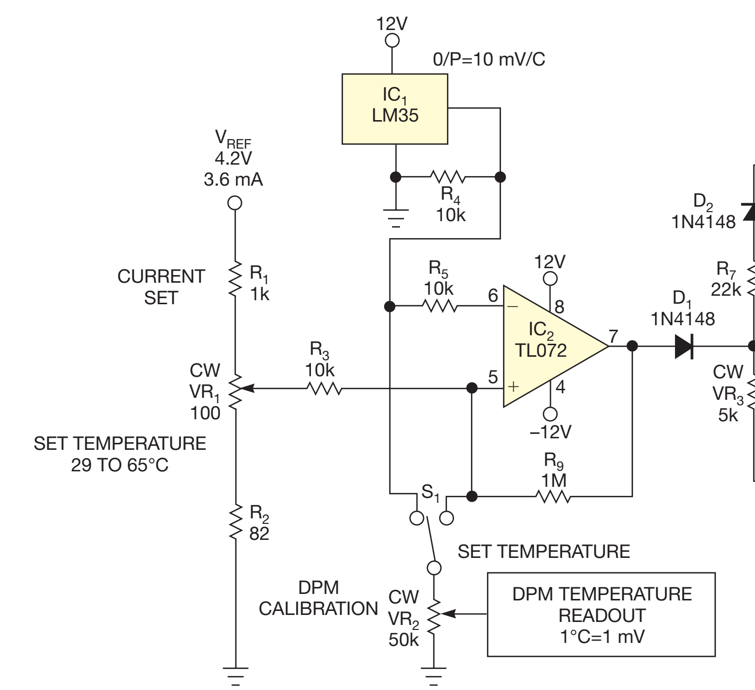

Figure 1 IC_1 senses the temperature of the item that Q_2 heats, and the temperature remains at the level that VR_1 sets.

Adjust power-efficient LED switch to any light intensity

Raju Baddi, Tata Institute of Fundamental Research, Pune, India

You can use an LED as a photoelectric sensor. A previous Design Idea shows that such a switch is highly power-efficient, consuming almost no power (**Reference 1**). You cannot, however, adjust that configuration to switch at the desired light intensity. You can adjust the circuit in this Design Idea to any threshold level of light intensity necessary to maintain the on state of the photoelectric switch while retaining almost the same power efficiency of the original circuit (**Figure 1**).

Illuminating the reverse-biased green LED with ambient light causes the small current that flows through the LED to form the base current of the BC549 NPN transistor, which is amplified and passed on to the base of the BC177 PNP transistor. A magnified version of this current flows through the emitter of the BC177. The voltage drop across the emitter resistor depends on its value and the current flowing through it, which in turn determines the voltage drop across the CE terminals of the BC549.

By adjusting the value of the series emitter resistor, you can set a voltage corresponding to logic zero of a CMOS gate for any desired intensity of light falling on the green LED. This intensity depends heavily on the response of the green LED and the current gains of the two transistors, so you select the resistor value by shorting out combinations of the series string of resistors and use the 10-MΩ potentiometer as a fine adjustment. Once you find a suitable value, you can remove the unused resistors from your circuit.

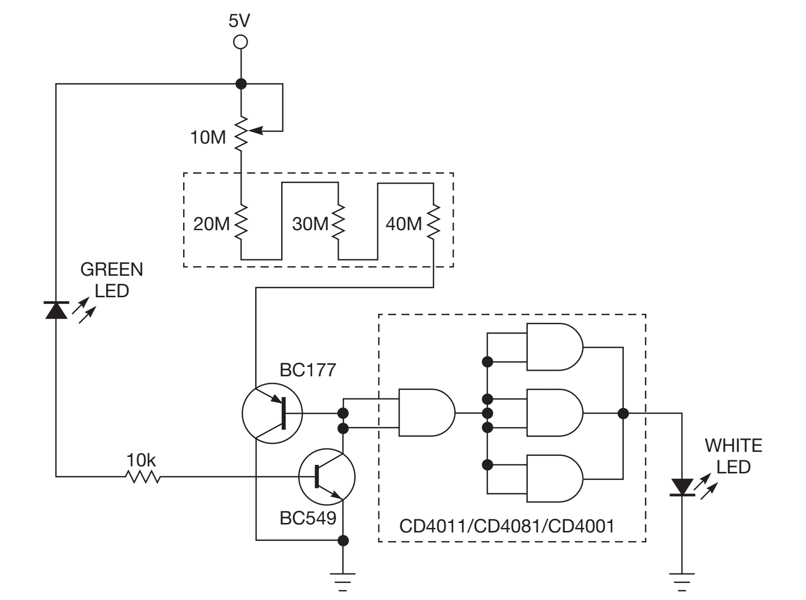

Figure 1 The photocurrent through the green LED amplifies to CMOS-logic levels to turn on the white LED when ambient light falls.

When the ambient-light intensity falls below this level, both the base current of the BC549 and the current through the emitter series resistors decrease. This decrease raises the input voltage at the CD4011 logic gate higher than the CMOS switching threshold. The typical gate sourcing current at a 3V output is approximately 3 to 4 mA per gate; running three gates in parallel delivers approximately 10 mA to the white LED. You can use inverting or noninverting gates for the same result. The circuit still retains its power efficiency because the required series-resistor values normally exceed 10 MΩ.

You can check a green LED's suitability for use as a photodiode by measuring the voltage drop across the LED with a 200-mV digital multimeter. If the LED is suitable as a photoelectric sensor, you will see a voltage of 0.3 to 1 mV across it, and this voltage changes with the intensity of light falling on the LED. **EDN**

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Drive 16 LEDs with one I/O line

Zoran Mijanovic and Nedjeljko Lekic,
University of Montenegro, Podgorica, Montenegro

Over the last few years, several Design Ideas have described how to use just a few microcontroller I/O pins to drive many LEDs (**references 1 through 7**). The circuit in **Figure 1** can drive 16 LEDs with just one pin and two shift registers. You can use the circuit to drive long-dot-bar or two seven-segment-digit displays. Adding multiplexing to the same circuit enables it to drive eight seven-segment LED digits.

The microcontroller drives the shift registers' clock inputs. That signal also passes through an RC filter and drives data inputs A and B. A 100-kΩ resistor, R, and the A and B input pins' capacitances form the RC filter (**Figure 2**), producing time delay of approximately R×C×ln2=100 kΩ×(5 pF+5 pF)×0.7=0.7 μsec.

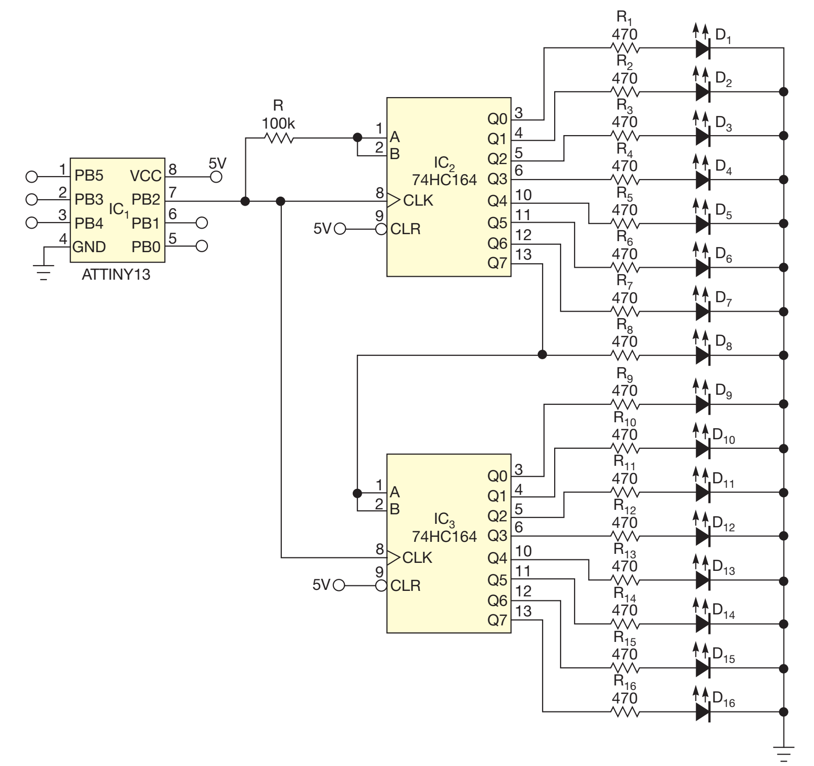

Figure 1 A 16-LED dot-bar/bar-graph display uses two 8-bit serial-input/parallel-output shift registers.

To write a logic zero to the shift register, the microcontroller holds a low level for approximately 2 μsec, which is longer than the time delay. It then sets the signal to a logic one, or high, level. To write a logic one, the microcontroller holds the high level for longer than the time delay. The MCU then makes negative pulses of approximately 0.25 μsec, or two CPU cycles, which is shorter than the time delay and which doesn't change the logic level at the data inputs.

Figure 3 shows the clock signal in Channel 1 (yellow) and the data signal in Channel 2 (blue). The oscilloscope is a Tektronix (www.tektronix.com) DPO4034 with TPP0850 high-voltage probes. These probes have 40-MΩ input resistance and only 1.5-pF input capacitance, minimizing distortion.

A rising edge on the clock signal clocks the shift registers. This edge corresponds to the data signal's local minimum. **Figure 3** also shows that the minimum data-signal voltages for logic zero and logic one are 1.3 and 3.1V, respectively. The shift register's logical threshold is 2.5V.

These voltages guarantee sufficient voltage margins. If your design requires higher margins, vary the signal timing and use a higher resistance for R in **Figure 1**. This circuit stores 16 bits in shift registers in approximately 35 μsec.

You can view a short video of the circuit in operation and download a code listing, in C, at the online version of this Design Idea at www.edn.com/4368093. The software turns on the LEDs one by one every 500 msec until all LEDs are on. It then turns off all the LEDs and repeats the cycle. **EDN**

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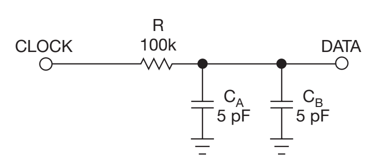

Figure 2 An RC filter provides a 0.7-μsec delay.

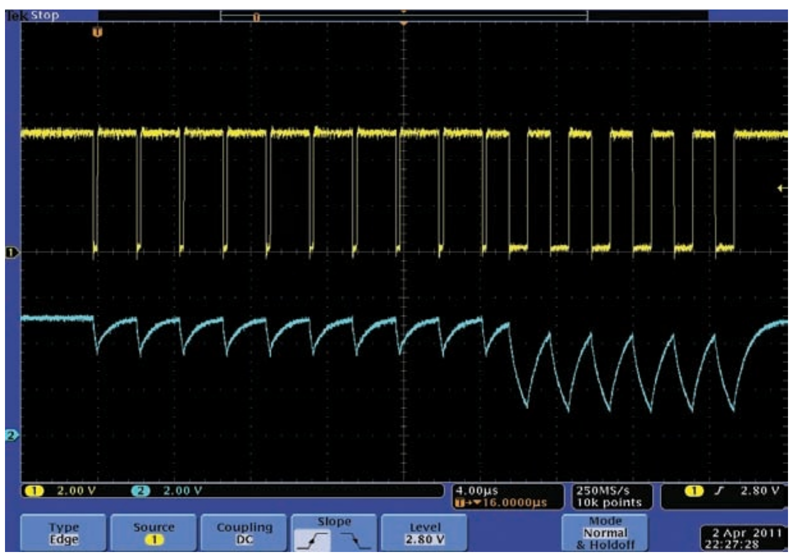

Figure 3 The waveform shows the circuit writing the pattern 1111111111000000 for the display. The upper, yellow trace is the clock signal, and the lower, blue trace is the data signal.

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Offline supply drives LEDs

TA Babu, Chennai, India

LEDs need power when rectified ac-mains voltage drops during its cycle. The circuit in **Figure 1** lets you use an inductorless, switching, offline power supply as an LED driver for emergency-exit signs and neon-light replacements. The design uses off-the-shelf components, offers efficient operation without an inductor in the dc side of the circuit, has no high-voltage capacitors, operates directly from either 120 or 230V ac, has minimal power dissipation, and has adjustable output voltage.

The circuit operates by controlling the conduction angle of MOSFET Q_2. When the rectified ac voltage is below the high-voltage threshold, V_{TH}, which D_1 sets, the series pass transistor turns on. The series pass transistor turns off when the output storage capacitor, C_2, charges up to the regulation point.

THE DESIGN DOES NOT REQUIRE AN INDUCTOR IN THE DC SIDE OF THE CIRCUIT.

The circuit's output voltage decays when Q_2 is off and when the rectified ac is below the output voltage (**Figure 2**). The load and the value of C_2 determine the amount of decay. The switch conducts only when it has low voltages across it, minimizing power dissipation. The output capacitor charges on the rising edge of a sine wave, which achieves reasonable efficiencies. Fusible resistor R_1 provides catastrophic-failure protection and limits input inrush when you first apply ac power. A 15V diode, D_2, limits the voltage to the gate of Q_2 and limits the voltage across transistor Q_1.

The current interruption in the MOSFET causes ringing on the drain-to-source voltage of Q_2, creating conducted EMI (electromagnetic interference). The 2.2-mH choke, L_1, and capacitor C_1 suppress EMI. This design maintains a fairly constant illumination over a wide voltage variation in the input. If necessary, you can add a few more such strings to suit your requirements.

Note that this circuit does not provide galvanic isolation. Touching any part of the circuit during operation can give you an electric shock. EDN

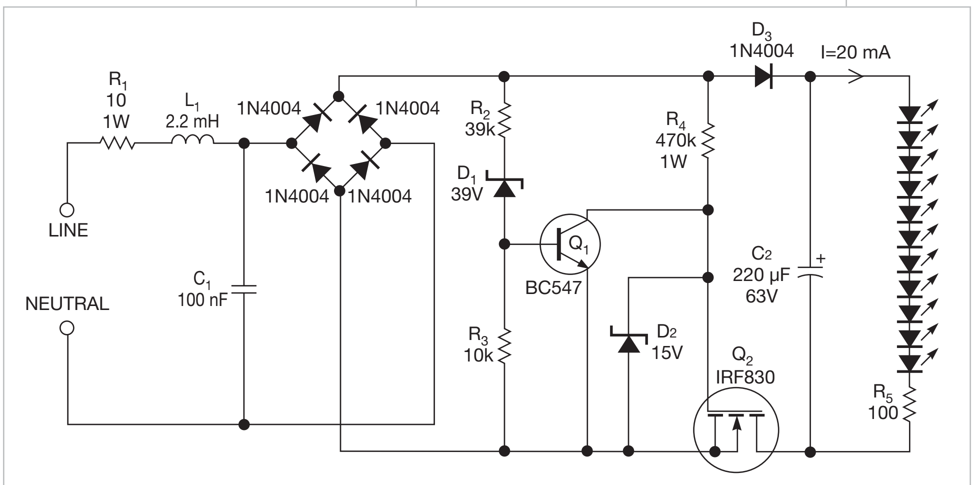

Figure 1 The transistor and MOSFET provide current to keep the LEDs lit.

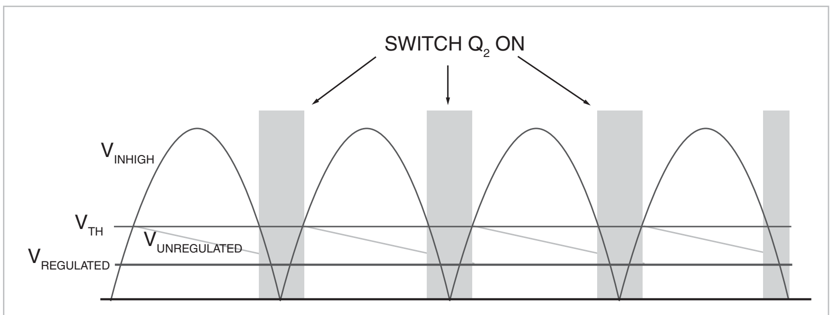

Figure 2 Switch Q_2 turns on when the rectified ac input voltage drops below a threshold.

Convert 1 to 5V signal to 4- to 20-mA output

Thomas Mosteller, Linear Technology Corp

Despite the long-predicted demise of the 4- to 20-mA current loop, this analog interface is still the most common method of connecting current-loop sources to a sensing circuit. This interface requires the conversion of a voltage signal—typically, 1 to 5V—to a 4- to 20-mA output. Stringent accuracy requirements dictate the use of either expensive precision resistors or a trimming potentiometer to calibrate out the initial error of less precise devices to meet the design goals.

Neither technique is optimal in today's surface-mounted, automatic-test-equipment-driven production environment. It's difficult to get precise resistors in surface-mount packages, and trimming potentiometers require human intervention, a requirement that is incompatible with production goals.

The Linear Technology LT5400 quad matched resistor network helps to solve these issues in a simple circuit that requires no trim adjustments but achieves a total error of less than 0.2% (**Figure 1**). The circuit uses two amplifier stages to exploit the unique matching characteristics of the LT5400. The first stage applies a 1 to 5V output—typically, from a DAC—to the noninverting input of op amp IC_{1A}. This voltage sets the current through R_1 to exactly V_{IN}/R_1 through FET Q_2. The same current is pulled down through R_2, so the voltage at the bottom of R_2 is the 24V loop supply minus the input voltage.

This portion of the circuit has three main error sources: the matching of R_1 and R_2, IC_{1A}'s offset voltage, and Q_2's leakage. The exact values of R_1 and R_2 are not critical, but they must exactly match each other. The LT5400A grade achieves this goal with ±0.01% error. The LT1490A has <700-µV offset voltage over 0°C to 70°C. This voltage contributes 0.07% error at an input voltage of 1V. The NDS7002A has a leakage current of 10 nA, although it is usually much less. This leakage current represents an error of 0.001%.

The second stage holds the voltage on R_3 equal to the voltage on R_2 by pulling current through Q_1. Because the voltage across R_2 equals the input voltage, the current through Q_1 is exactly the input voltage divided by R_3. By using a precision 250Ω current shunt for R_3, the current accurately tracks the input voltage.

The error sources for the second stage are R_3's value, IC_{1B}'s offset voltage, and Q_1's leakage current. Resistor R_3 directly sets the output current, so its value is crucial to the precision of the circuit. This circuit takes advantage of the commonly used 250Ω current-loop-completion shunt resistor. The Riedon SF-2 part in the **figure** has 0.1% initial accuracy and low temperature drift. As in the first stage, offset voltage contributes no more than 0.07% error. Q_1 has less than 100-nA leakage, yielding a maximum error of 0.0025%.

Total output error is better than 0.2% without any trimming. Current-sensing resistor R_3 is the dominant source of error. If you use a higher-quality device, such as the Vishay PLT series, you can achieve an accuracy of 0.1%. Current-loop outputs are subject to considerable stresses in use. Diodes D_1 and D_2 from the output to the 24V loop supply and ground help protect Q_1; R_6 provides some isolation. You can achieve more isolation by increasing the value of R_6, with the trade-off of some compliance voltage at the output. If the maximum output-voltage requirement is less than 10V, you can increase R_6's value to 100Ω, affording

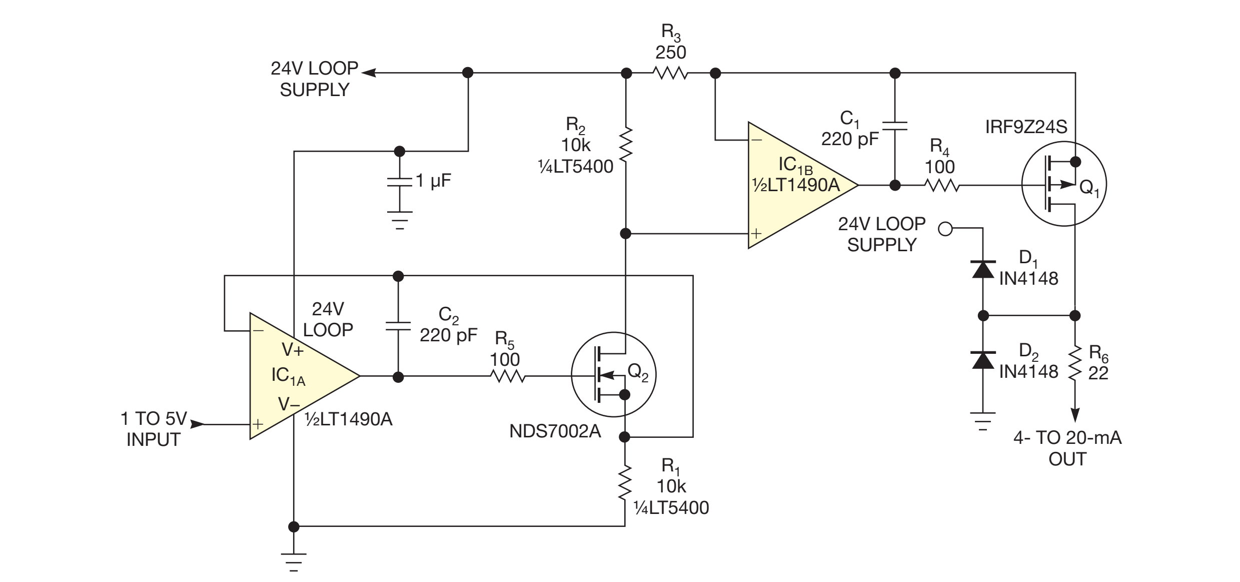

Figure 1 Precision matched resistors provide accurate voltage-to-current conversion.

even more isolation from output stress. If your design requires increased protection, you can fit a transient-voltage suppressor to the output with some loss of accuracy due to leakage current.

This design uses only two of the four matched resistors in the LT5400 package. You can use the other two for other circuit functions, such as a precision inverter, or another 4- to 20-mA converter. Alternatively, you can place the other resistors in parallel with R_1 and R_2. This approach lowers the resistor's statistical-error contribution by the square root of two. EDN

Inverting level-shift circuit has negative potential

Chun-Fu Lin and Shir-Kuan Lin, National Chiao Tung University, Hsinchu, Taiwan; and Hui-Shun Huang, Jyi-Jinn Chang, and Tai-Shan Liao, National Applied Research Laboratories, Hsinchu

Digital-system designs require you to consider many core voltages. Memory operates at 1.8V, I²C and FPGA devices operate at 3.3V, microcontrollers operate at 5V, and charge-coupled-device image sensors operate at –9 to 8V. Clocks for each device must suit their operating voltages.

You can use the level-shift circuit in **Figure 1** to adjust an input clock signal to the proper logic-high and logic-low voltage levels, including negative voltages. This property is handy for devices that need a negative voltage, such as a charge-coupled-device sensor. Although the circuit's output clock is 180°-inverted relative to the input clock, that inversion does not affect the function of the device.

The level-shift circuit comprises fast-switching transistors Q_1 and Q_2. The user chooses level-shift high and level-shift low, which are dc-bias voltages and which connect to the transistor emitters, to match the desired output high- and low-logic levels. C_1, R_1, D_1, C_2, R_2, and D_2 keep the base voltages of Q_1 and Q_2 close to that of their emitters.

Because memory and charge-coupled-device sensors usually have high-frequency clocks, you can choose C_1 and C_2 to prevent low-frequency-noise pass-through. The circuit in **Figure 1** uses a 20-MHz signal for measurements (**Table 1**) and thus uses a value of 100 pF for C_1 and C_2. When the input voltage's clock is low, Q_1 turns on and Q_2 turns off, driving the output voltage's clock to the level shift's high potential. When the input voltage's clock is high, Q_1 turns off and Q_2 turns on, driving the output voltage's clock to the level shift's low potential, even when that potential is negative relative to ground.

Because of the circuit's high switching speeds, keep component leads as short as possible to minimize inductance. This caveat is especially true for C_3 through C_6's leads to their respective transistor emitters and to the ground plane or the output ground return. EDN

TABLE 1 INPUT AND OUTPUT CLOCKS

High/low level shift (V)	Input clock (V)	Output clock (V)
3.3/0	0/5	3.3/0
20/10	0/5	20/10
–5/–10	0/5	–5/–10
2/–4	0/5	2/–4

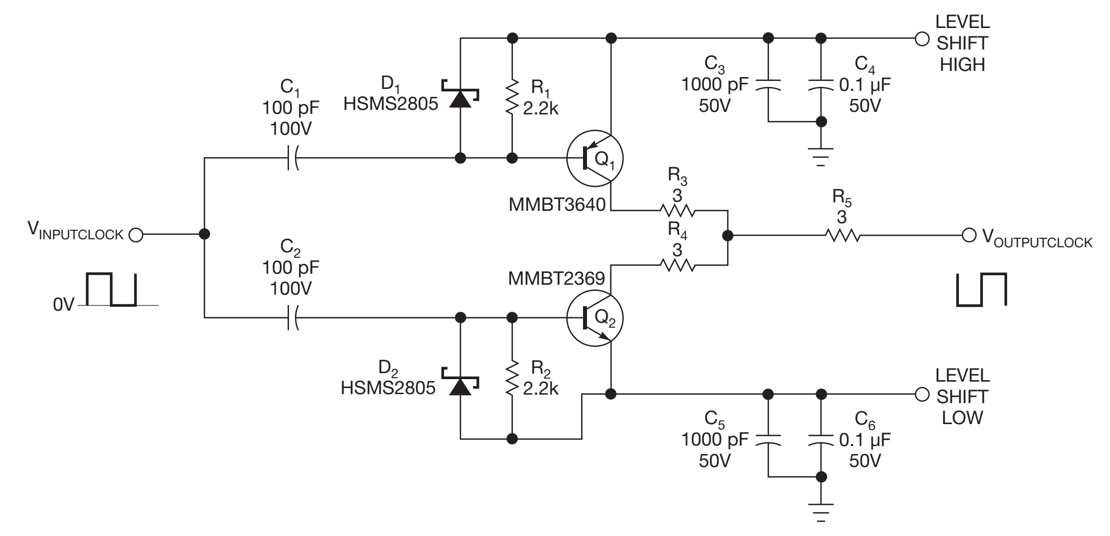

Figure 1 This simple and fast level-shift circuit can adjust an input clock to both positive and negative voltage levels.

Complementary-pair dc/dc converter simultaneously doubles, inverts supply voltage

Ajoy Raman, Bangalore, India

The circuit in this Design Idea uses an intrinsic property of collector voltages in one-transformer push-pull dc/dc converters: They have a swing of twice the supply voltage. When you implement these circuits with an NPN device, the collector swings from 0V to twice the supply-rail voltage. When you use PNP devices, the collector voltage swings from V_{CC} to an equal amplitude but negative V_{CC} (**Reference 1**). In this circuit, a complementary pair of transistors, simultaneously implementing a voltage doubler and a negative-voltage source, drives the two windings of the transformer.

One of the windings of transformer T_1 connects to ground, driven by PNP transistor Q_1 from V_{CC} (**Figure 1**). The other winding of T_1 connects to V_{CC}, and NPN transistor Q_3 drives the lower end to ground. Q_2 and Q_4 drive Q_1 and Q_3, respectively. The collectors of Q_3 and Q_1 through resistors R_4 and R_3 provide cross-coupled drives to Q_2 and Q_4. R_1 and R_2 form the collector loads for Q_2 and Q_4. D_1 and D_4 prevent the reverse breakdown of Q_1 and Q_3. The drive configuration and the transformer's winding polarity provide regenerative feedback and self-oscillation so that the transformer alternates between positive and negative saturation, inducing voltages to drive transistors Q_1 and Q_3 alternately on and off.

A square wave with an amplitude twice V_{CC} is generated at the collector of Q_1, which swings nominally from V_{CC} to the equal but negative output voltage. Simultaneously, a square wave with an amplitude twice the supply-rail voltage is generated at the collector of Q_3, which swings nominally from 0V to twice the supply-rail voltage.

D_2 and C_2 provide half-wave rectification and filtering of the Q_1 collector waveform generating the negative voltage output. Half-wave rectification and filtering of the Q_3 collector waveform using D_3 and C_3 generate the doubler's output.

T_1 is 200 turns of bifilar AWG 37 enameled wire wound 1-to-1 on a ferrite toroid core (**references 2** and **3**). **Table 1** shows the experimental results with the voltage doubler and negative-voltage-generation circuit operating over an input voltage of 5 to 30V, demonstrating operation over a wide input voltage range and providing power at both outputs simultaneously at moderate efficiency. EDN

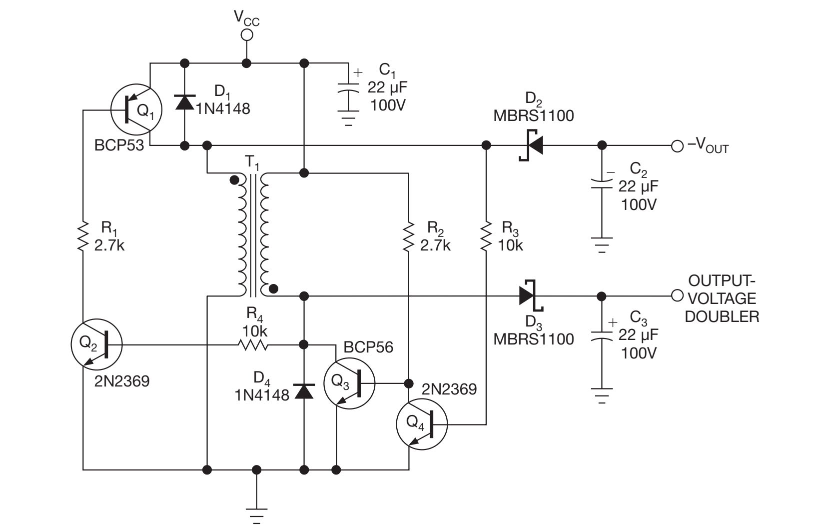

Figure 1 Cross-coupled regeneration drives switching transistors Q_1 and Q_3 and the windings of the transformer. The resulting voltage swings at their collectors are rectified to twice the positive and the negative power-supply rails.

REFERENCES

1 Raman, Ajoy, "Voltage doubler uses inherent features of push-pull dc/dc converter," *EDN*, Aug 16, 2007, pg 72, http://bit.ly/GTlveF.
2 "T503125," Ceramic Magnetics Inc, http://bit.ly/L3FzeW.
3 MN60 manganese-zinc material specs, Ceramic Magnetics Inc, http://bit.ly/KoyO4Y.

TABLE 1 EXPERIMENTAL RESULTS

Input voltage (V)	Input current (mA)	Frequency (kHz)	Voltage doubler (V)	Current doubler (mA)	Negative voltage (V)	Negative current (mA)	Input power (W)	Output power (W)	Efficiency (%)
5	253	2.1	7.68	81.7	−3.41	−72.5	1.27	0.87	69
9.97	360	4.05	17.33	115.5	−8.65	−86.5	3.59	2.75	76.6
15	420	6.02	27.2	136	−13.58	−90.5	6.3	4.93	78.2
19.4	400	7.37	34.9	145.4	−18.33	−61.1	7.76	6.19	79.8
25	340	10.47	48.5	97	−23.8	−79.3	8.5	6.59	77.5
30	410	12.07	56.5	113	−27.6	−92	12.3	8.92	72.5

READERS' CHOICE

Wireless temperature monitor has data-logging capabilities

Tom Au-Yeung and Wilson Tang, Maxim Integrated Products, Sunnyvale, CA

You can use a local temperature sensor and an ASK (amplitude-shift-keying) transmitter/receiver pair to design a simple wireless temperature-monitoring system with data-logging capabilities. A microcontroller processes and displays the temperature reading to the user. The microcontroller's onboard UART (universal asynchronous receiver/transmitter) also allows for data-logging applications.

Local-temperature sensor IC_1 detects the ambient temperature at the device (**Figure 1**). The output of IC_1 is a square wave with a frequency proportional to temperature in kelvins. ASK transmitter IC_2 modulates the signal onto the carrier frequency of 315 MHz. You measure the output signal's frequency with a frequency counter. The configured scalar multiplier is 1K/Hz when the TS1 pin connects to ground and the TS0 pin connects to V_{DD}. This scalar multiplier is configurable with pins TS1 and TS0. ASK receiver IC_3 demodulates the signal at the corresponding carrier frequency (**Figure 2**).

Comparator IC_4 connects to IC_3's RSSI

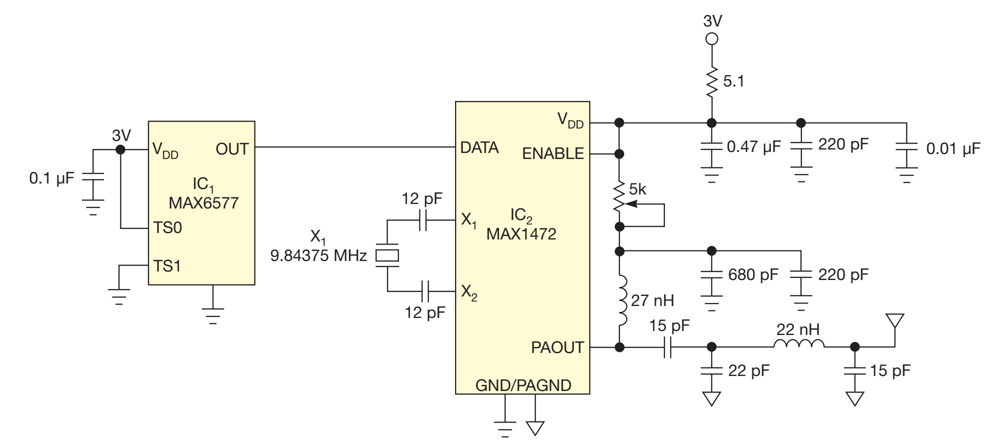

Figure 1 The MAX6577 temperature sensor and 315-MHz MAX1472 ASK transmitter form a wireless temperature-monitoring system.

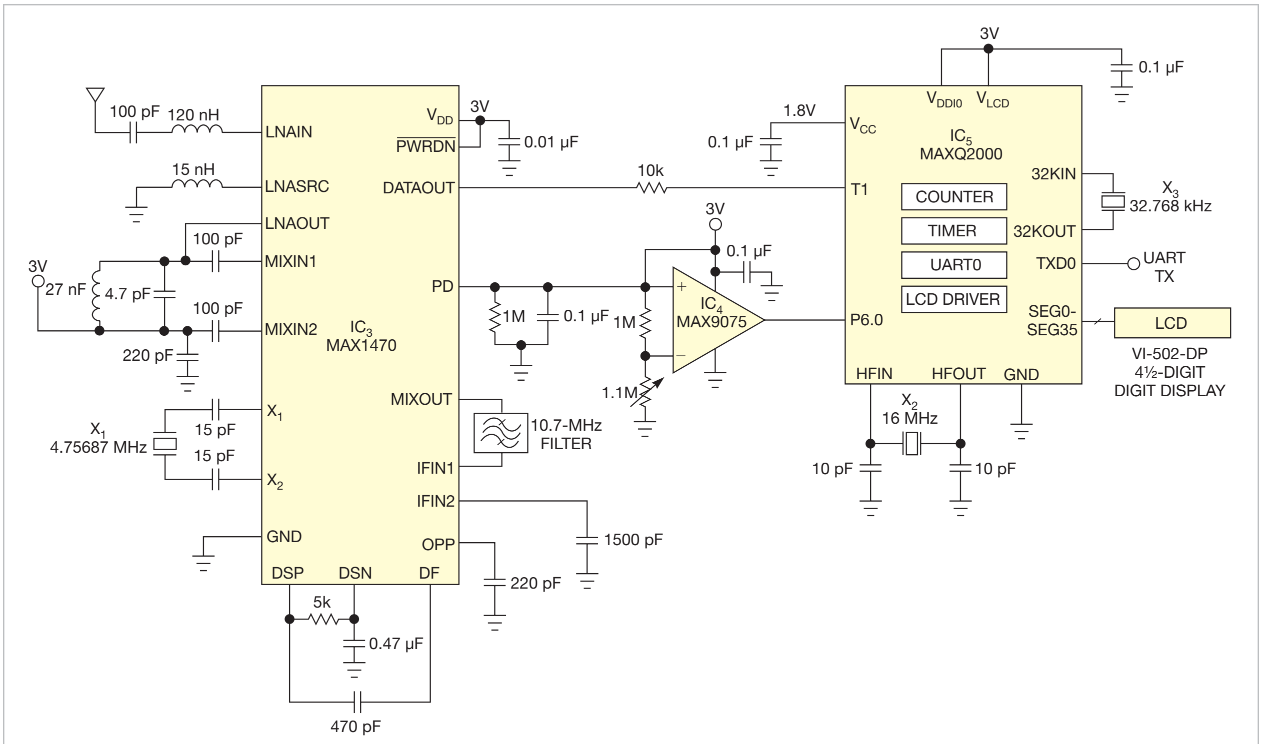

Figure 2 An ASK receiver with a microcontroller processes and displays temperature data.

(received-signal-strength indicator) with an internal peak detector. The external RC follows the peak power of the received signal and compares it with a predetermined, resistor-voltage-divider-generated voltage level. Lab experiments show that a threshold of approximately 1.57V generates a valid output on the data-out pin without receiving false readings. Adjust this threshold to the proper level for optimal performance. The comparator's output is low when the received signal is weak or invalid and high when the received signal is adequate.

Microcontroller IC_5 then measures and displays the value of the signal frequency using its integrated timer/counters and LCD-driver peripherals. A counter tracks the number of rising-edge transitions on the input temperature signal, and a timer tracks the elapsed time. After the timer's 1-sec period elapses, an interrupt occurs. At that moment, the circuit reads the counter value, converts it to Celsius, and displays it on the LCD. The counter then resets to zero to restart the process. The timer automatically reloads once the timer interrupt occurs. UART0 also outputs the resulting temperature. A handheld frequency counter verifies the temperature reading.

The microcontroller monitors the signal power through P6.0, a general-purpose input pin. When the input is logic low, the LCD and UART output "no RF" to alert users of possible transmitter issues when the transmitter and receiver are too far apart from each other. The LCD connection follows the design in the IC's evaluation kit. Using a look-up table in the data segment of the assembly code enables you to preserve the internal mapping of the display's A through G segments. This preservation ensures that the display enables the correct segments. Using an RS-232 level converter, the UART output sends data to a data-logging device, such as a computer.

Use the MAX-IDE assembler software to program the device during assembly. The MAXQJTAG board operates with the MAX-IDE to load the code onto the device. You can download the project files at www.edn.com/4368878. This design provides for a 1-sec temperature-refresh rate in 1°C increments, which is within the accuracy of IC_1. EDN

Microcontroller drives piezoelectric buzzer at high voltage through one pin

Mehmet Efe Ozbek, PhD, Atilim University, Ankara, Turkey

A previous Design Idea demonstrates how you can use a microcontroller to drive a piezoelectric buzzer at a high alternating voltage through a four-MOSFET circuit that interfaces to two of its I/O pins (**Reference 1**). This expanded Design Idea provides a modification of the previous circuit to save one of the I/O pins of the microcontroller. Q_4's gate connects to Q_2's drain rather than a second I/O pin (**Figure 1**). The microcontroller turns on Q_2 by applying a high logic level to the I/O pin, pulling Node A down to a low logic level. This action turns on Q_3 and turns off Q_4. The voltage on Node B becomes 15V, and Q_1 turns off. The voltage across the piezoelectric element is now 15V.

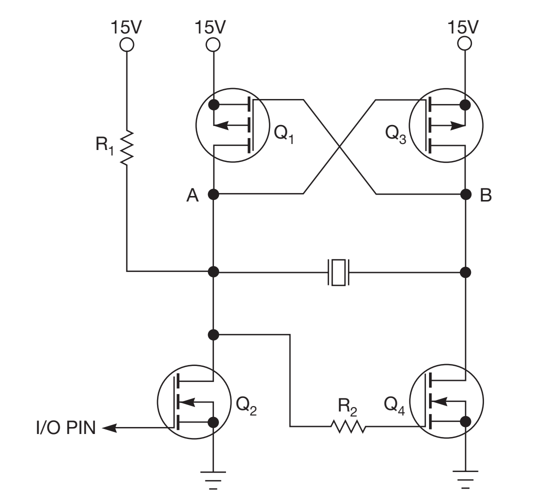

Figure 1 One microprocessor I/O pin drives this circuit to generate an alternating voltage across the piezoelectric buzzer.

The microcontroller then toggles the I/O pin low, turning off Q_2. Q_1 is also off, so Node A slowly rises to a high logic level through pullup resistor R_1. When the voltage on Node A reaches the switching threshold of the inverter comprising the Q_3 and Q_4 pair, Q_3 quickly turns off and Q_4 quickly turns on. The consequently low logic level on Node B turns on Q_1 and speeds the increase of Node A's voltage. The 15V across the piezoelectric buzzer is now of the opposite polarity.

R_2 weakens the coupling between the output and the input of Q_4 due to the presence of the piezoelectric element. A value of 330Ω for R_2 is usually sufficient to suppress high-frequency oscillations that the feedback causes. The drained power from the supply increases if you use low values for R_1. Using excessively large values for R_1 also increases power dissipation by prolonging the switching of the transistors and associated shoot-through currents. The optimum value for R_1 is approximately 1 kΩ.

Saving an I/O pin with this design involves the trade-off of increased power consumption. The circuit's power consumption is thus one order of magnitude greater than the circuit described in the previous Design Idea. EDN

REFERENCE

1 Ozbek, Mehmet Efe, "Microcontroller drives piezoelectric buzzer at high voltage," *EDN*, March 1, 2012, pg 44, http://bit.ly/JyzLpz.

Logic gates form high-impedance voltmeter

Raju Baddi, Tata Institute of Fundamental Research, Pune, India

You can use the circuit described in this Design Idea to estimate voltages across 10- to 100-MΩ resistances. It also works for reverse-biased diodes.

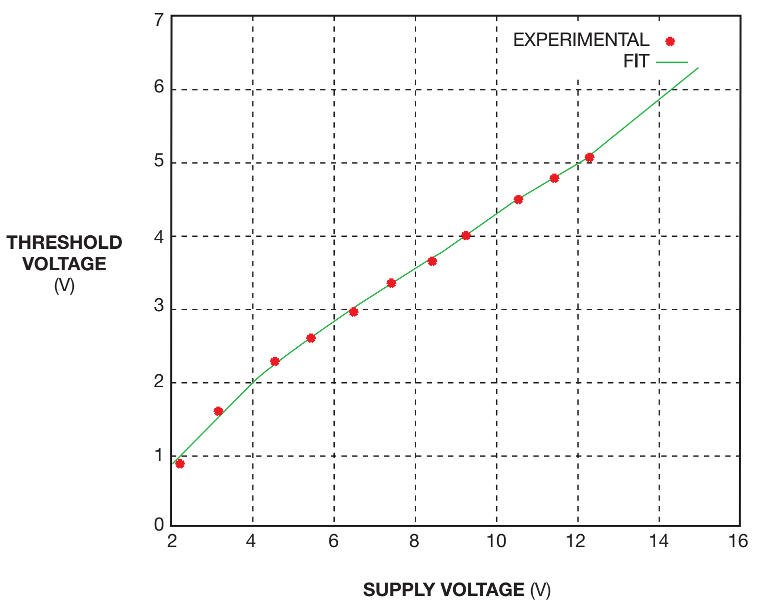

Figure 2 The gate's threshold voltage is nearly linear respective to the power-supply voltage. Download this plot from the online Design Idea at www.edn.com/4368072.

ESTIMATE THE UNKNOWN VOLTAGE USING A GRAPH OF THRESHOLD VERSUS SUPPLY VOLTAGE.

The common CMOS gates in **Figure 1** have an input threshold voltage in which the output swings from logic zero to logic one, and vice versa. The threshold voltage depends on the supply voltage (**Figure 2**). Because of each CMOS gate's high input impedance, input currents are approximately 0.01 nA. If you apply 5V to 100 MΩ, you get 50 nA. Thus, you can connect the gate input at a point at which it draws a negligible amount of current.

You can vary the CMOS gate's supply voltage to attain the desired threshold voltage for the gate input. If you apply the unknown voltage to one of the gate's inputs and then connect the other input to the positive-voltage supply, you can vary the supply voltage, V_S, until you reach a point at which the threshold voltage at the input becomes equal to the unknown voltage.

At this point, the output of the sense gate, IC_{1A}, changes from logic zero to logic one. When this event happens, the threshold of the gate passes the unknown voltage. You can estimate the unknown voltage using a graph of threshold voltage versus supply voltage, such as the one in **Figure 2**. By fitting a parabola or a polynomial to the experimentally obtained points—say, some 20 points lying in the supply-voltage range of 2 to 15V—you can estimate the threshold voltage, V_T, for any supply voltage.

This circuit has been built and tested. The online version of this Design Idea includes Octave/Matlab code that you can view at www.edn.com/4368072. **EDN**

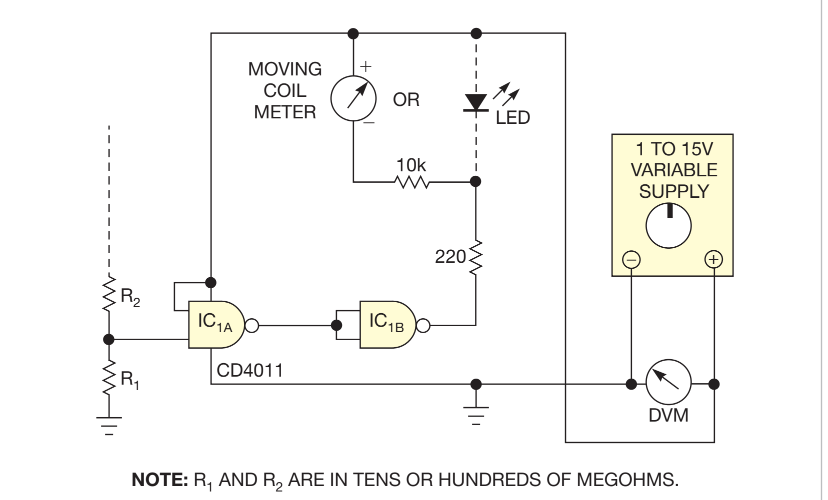

Figure 1 Use CMOS gates and a variable power supply to find an unknown voltage.

READERS' CHOICE

Use a photoelectric-FET optocoupler as a linear voltage-controlled potentiometer

Sajjad Haidar, University of British Columbia, Vancouver, BC

You can use a photoelectric FET as a variable resistor or a potentiometer in combination with a fixed resistor. The H11F3M photoelectric FET has an isolation voltage of 7.5 kV, enabling you to safely control high-voltage circuit parameters. The nonlinear-transfer characteristics of these devices are problematic, however (**Figure 1**). To correct the nonlinearity, using a simple feedback mechanism as a potentiometer yields a linear response (**Figure 2**). This circuit uses two photoelectric FETs: one for feedback and the other for applications requiring an isolated potentiometer. You connect the inputs of the two photoelectric FETs in series to ensure the same amount of current for the input LEDs.

Place 50-kΩ resistors at the FET outputs to mimic the response of a potentiometer. The circuit amplifies the difference between the set input voltage, which you adjust using potentiometer R_7, and the feedback from photoelectric FET 1. The resulting output controls the current in the

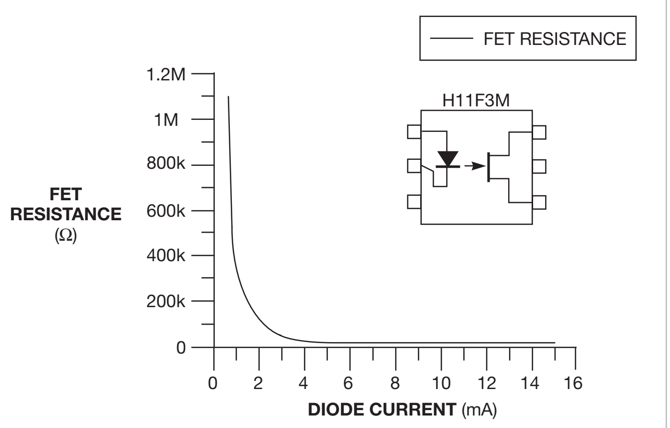

Figure 1 The output resistance of a photoelectric FET is nonlinear with respect to the input-LED current.

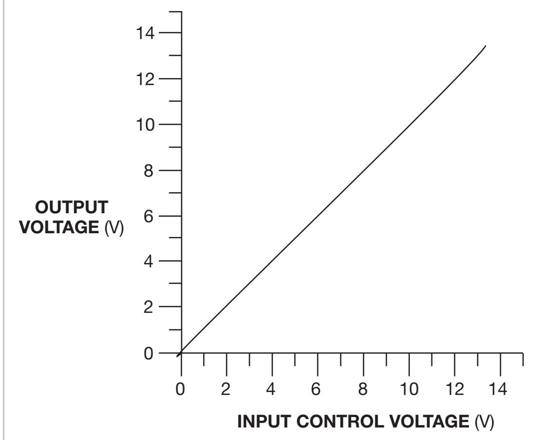

Figure 3 The feedback circuit greatly improves output linearity.

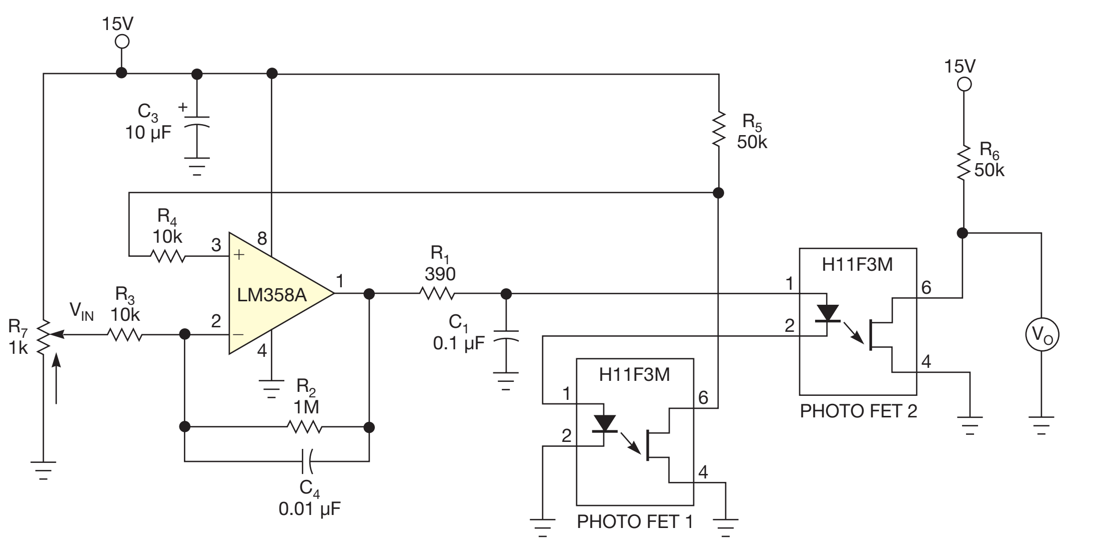

Figure 2 This circuit feeds back the response of an identical photoelectric FET to linearize the response.

photoelectric-FET LEDs until the feedback voltage equals the input voltage. The output voltage follows linearly with the input voltage (**Figure 3**). You might think that photoelectric FETs bearing the same part number are identical, but small manufacturing discrepancies can be present. Five H11F3M parts have offsets within 3%. **EDN**

Minimize noise in power-supply measurements

John Lo Giudice, STMicroelectronics, Schaumburg, IL

You must minimize noise when measuring ripple in power rails because the ripple's amplitude can be low. Oscilloscope probes are essential measurement tools, but they can introduce noise and errors. Ground leads, such as those that attach to standard oscilloscope probes, can add noise that's not present in your circuit to an oscilloscope's trace. The wire loop acts as an antenna that picks up stray magnetic fields. The larger the loop area, the more noise it picks up.

To prove this theory, connect the oscilloscope ground lead to the probe tip and move it around. The oscilloscope will show the noise increasing and decreasing with the ground-lead movement. You can use an oscilloscope probe with its ground lead and sockets to build a simple interconnect board (**Figure 1**).

Start by removing the probe's cover, which reveals the probe tip. There is a short distance between the tip and the ground ring. You need one of two sockets: a right-angle, or horizontal, socket or a vertical socket, similar to those in **Figure 1**.

Solder the center leg of the socket to the output of the power supply, and solder the other leg to the power-supply return. Connect a 0.1-μF surface-mount, stacked ceramic capacitor between the two sockets. This step limits the probe bandwidth to approximately 5 MHz, which further reduces high-frequency noise and lets the lower-frequency ripple pass through. **Figure 2** shows the completed interconnect board; **Figure 3** shows a schematic of the board.

Insert the probe tip into the socket to measure ripple. You will get a ripple measurement without spikes or other noise.

You should use a multilayer stacked ceramic capacitor because it's better at decoupling high-frequency noise. Electrolytic, paper, and plastic-film capacitors comprise two sheets of metal foil with a sheet of dielectric separating the metal sheets, and these three components form a roll. Such a structure has self-inductance; thus, the capacitor acts more like an inductor than a capacitor at frequencies higher than a few megahertz.

Figure 4 shows the impedance to the power supply for various stacked-ceramic-capacitor values. **EDN**

Figure 1 A standard oscilloscope probe has a ground lead that can pick up noise.

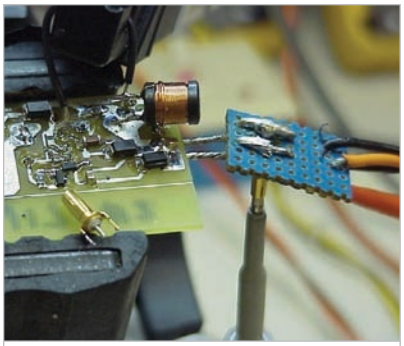

Figure 2 Solder wires from the power supply under test to an interconnect board reduce ground-lead length.

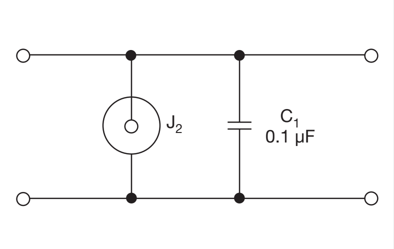

Figure 3 A ceramic capacitor further reduces high-frequency noise.

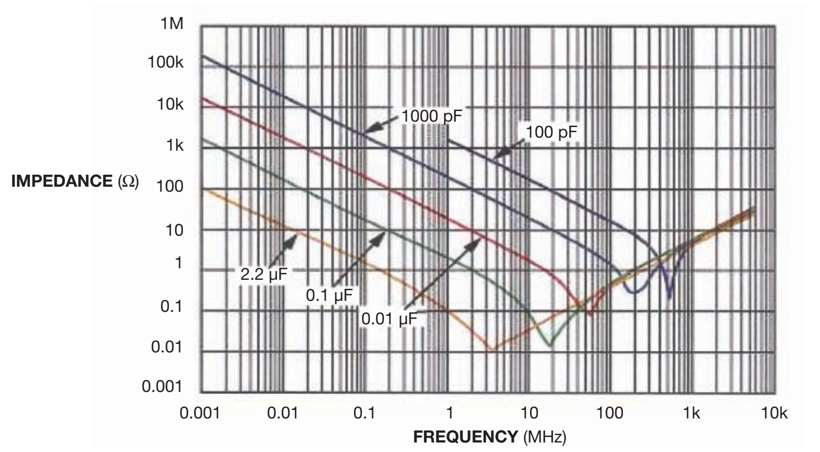

Figure 4 Probe impedance varies with capacitor value.

Probing system lets you test digital ICs

Raju Baddi, Tata Institute of Fundamental Research, Pune, India

This Design Idea describes a simple yet powerful handheld probe that you can use as both a logic probe and a pulse generator either individually or simultaneously. This feature makes the probe useful for testing DIP digital ICs, such as gates, flip-flops, and counters, using a socketed fixture with three-post jumpers to connect each pin to logic high or logic low or to 5V or ground.

Three pushbutton switches, two dual-color LEDs, and two probe tips are built into a plastic cylinder, such as an empty, 20g or larger glue-stick tube. The generator's probe tip hooks to fit onto the test fixture's jumper pins and mounts onto a spring—such as those in retractable ball-point pens—for flexibility, and it allows the logic-probe tip to move to the output under test. Two of the pushbutton switches set the generator's quiescent state for a high or low output. The third switch briefly single-pulses the output to the opposite state. If the switch is pressed for longer than 2 seconds, the output produces a pulse train.

IC_{1A}, an NE556, is a 2-sec monostable circuit, which triggers a 1-msec-pulse generator circuit employing gate G_1, resistor R_1, and capacitor C_1 (**Figure 1a**). G_4 buffers the circuit. The output of the monostable circuit also passes through G_2 and G_3 to mask the output of the astable component, IC_{1B}, an NE556 that provides the pulse train. To prevent any spurious pulse from reaching output Probe A when switch S_1 is not depressed, keep IC_{1B} deactivated by applying a low voltage to its reset pin 4 through transistor Q_1, whose biasing is further guarded by a 0.68-μF capacitor.

When you press switch S_1 for a short

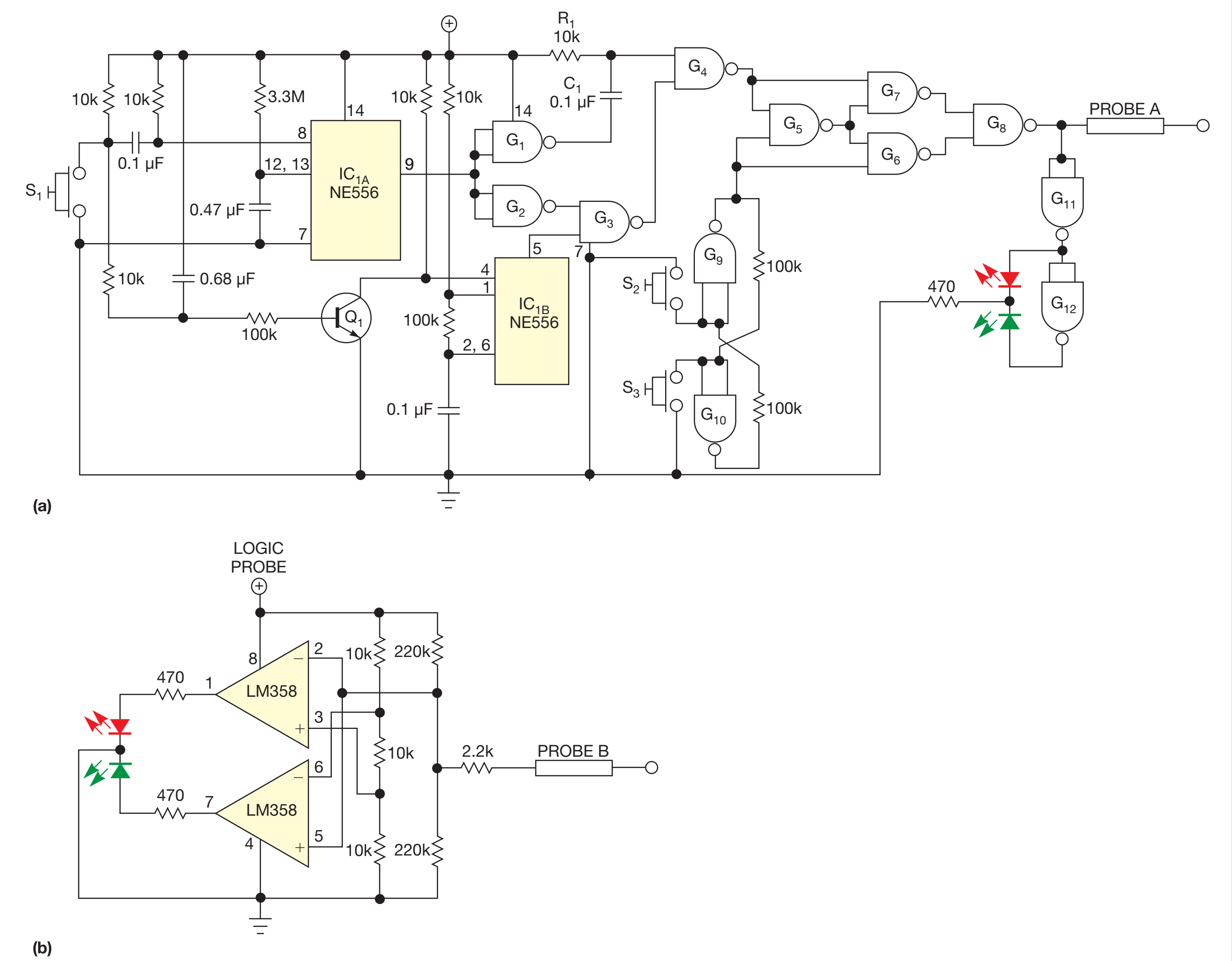

Figure 1 This circuit combines analog and digital functions. Probe A is the pulse-generator probe, and Probe B is the logic probe (a). Although not shown, a 100-μF capacitor should be connected between the supply and ground. Red LEDs indicate logic zero, and green LEDs display logic one (b).

time, IC_{1A} fires and produces a high output for approximately 2 sec. The 1-msec pulse from G_1, R_1, C_1, and G_4 reaches the pulse Probe A through the XOR function comprising G_5 through G_8, and the output of the astable IC_{1B} is masked at G_3 from reaching the XOR. If you depress switch S_1 for longer than 2 sec, the monostable IC_{1A} times out. This action unmasks G_3 and allows the 70-Hz oscillation from IC_{1B} to reach the XOR.

G_9 and G_{10} form a bistable circuit, which "remembers" the most recently pressed S_2 or S_3 switch and controls the inverting and noninverting operation of the XOR function. G_{11} and G_{12} together drive the dual-color LED to indicate the pulse generator's polarity. Red indicates that Probe A's output is mainly logic zero, with the single 1-msec pulse a logic high. Green indicates the opposite.

The LM358 acts as a window-detector logic probe (**Figure 1b**). With the values in the **figure**, the red LED lights at Probe B voltages of less than 35% of the supply voltage, and the green LED lights at voltages greater than 65% of the supply voltage. Neither LED lights between these voltages. You may wish to adjust the resistor network to reduce the lower threshold to include the transistor-transistor-logic zero of less than 0.8V.

If you use CD4011 quad NAND gates, you can externally power the probe at 4.5 to 15V. Using a CD4093 Schmitt-trigger quad NAND for G_1 through G_4 ensures no spurious oscillations as a result of the slow voltage rise at timing capacitor C_1. If your design requires a higher-current generator drive, you can add a pair of NPN and PNP boost transistors to the output.

Figure 2 shows a jig for testing the digital ICs. Configure the 16-pin DIP socket for the device under test with an array of triple-post headers and push-on jumpers. You can connect any pin directly or through a resistor to power or ground to configure power or logic levels. The resistors can be any suitable value; approximately 2 kΩ is appropriate.

To set a TTL low, the pin must connect directly to ground. To inject a signal, hook the flexible spring-mounted generator, Probe A (**Figure 3**), onto the appropriate input post and move logic Probe B to the corresponding output post or pin. See a suggested perf-board layout at www.edn.com/4374947.EDN

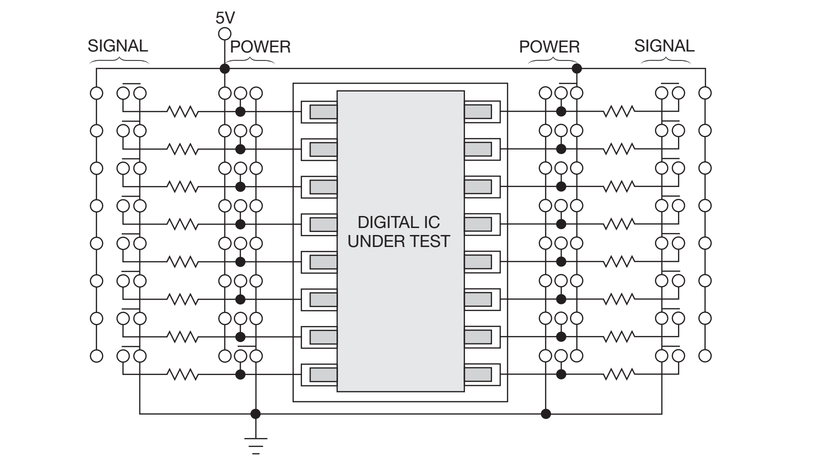

Figure 2 Program this test jig with header posts and jumpers for the IC under test.

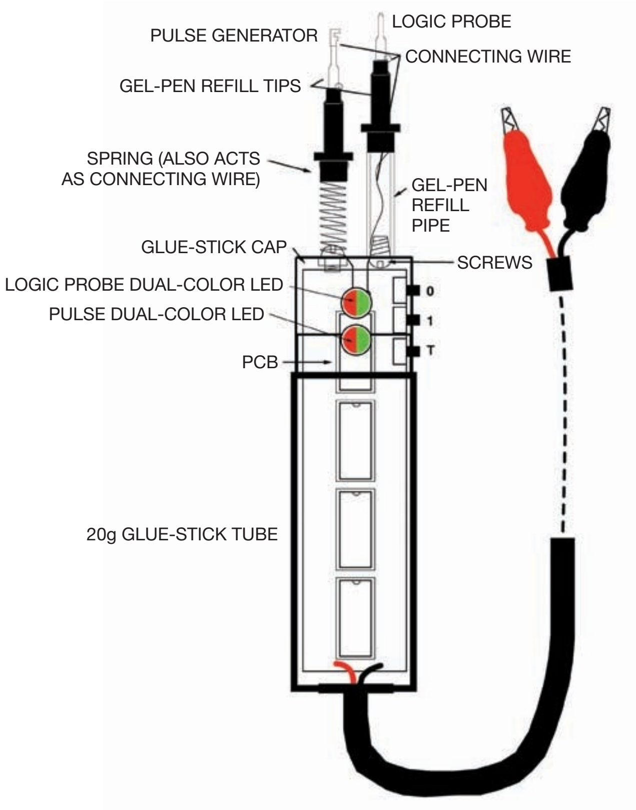

Figure 3 To inject a signal, hook the flexible spring-mounted generator, Probe A, onto the appropriate input post and then move logic Probe B to the corresponding output post or pin.

REFERENCES

1 Baddi, Raju, "Logic probe uses six transistors," *EDN*, Dec 15, 2010, pg 46, http://bit.ly/n24oau.

2 Rentyuk, Vladimir, "Logic probe uses two comparators," *EDN*, Aug 25, 2011, pg 54, http://bit.ly/wtuKgi.

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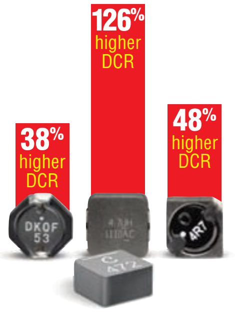

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