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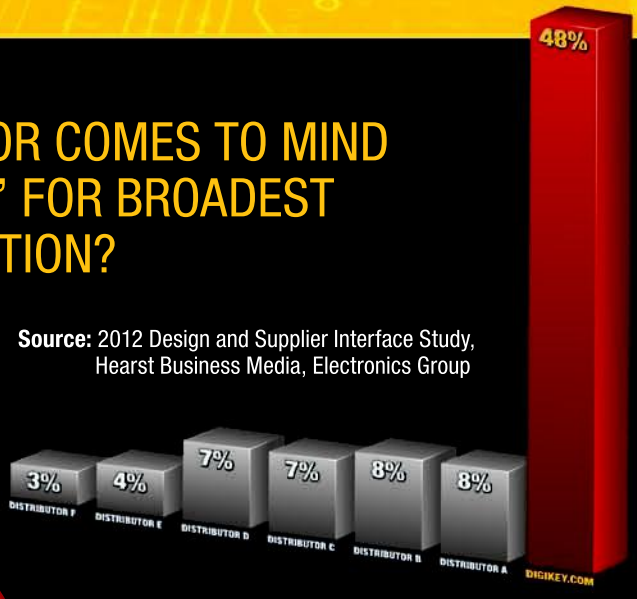

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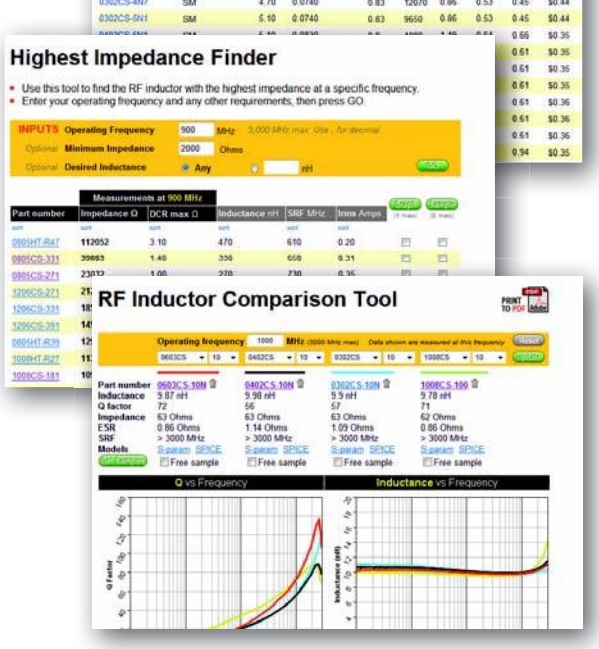

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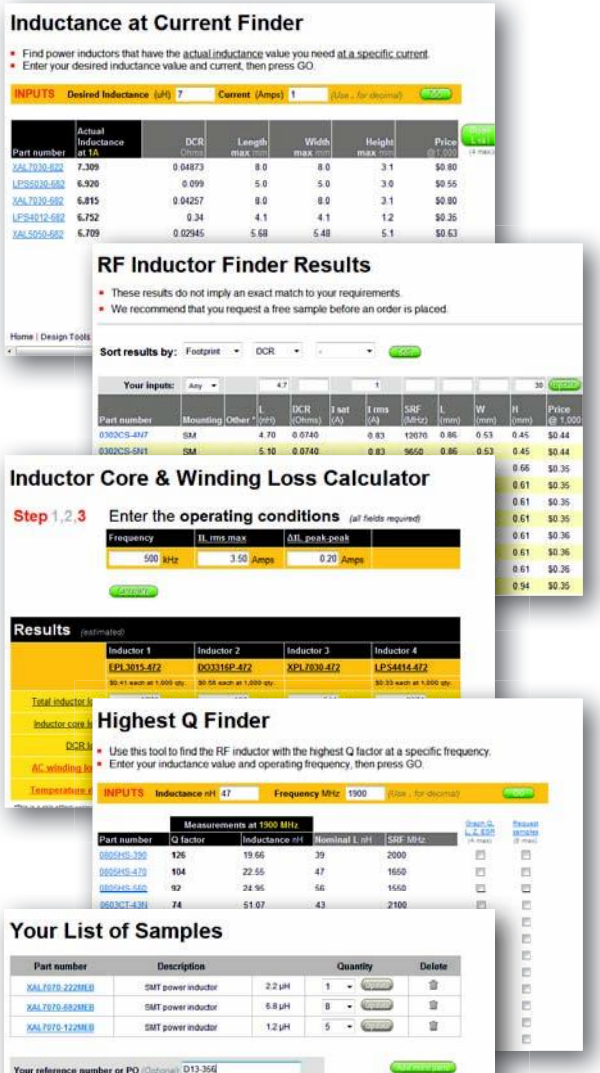

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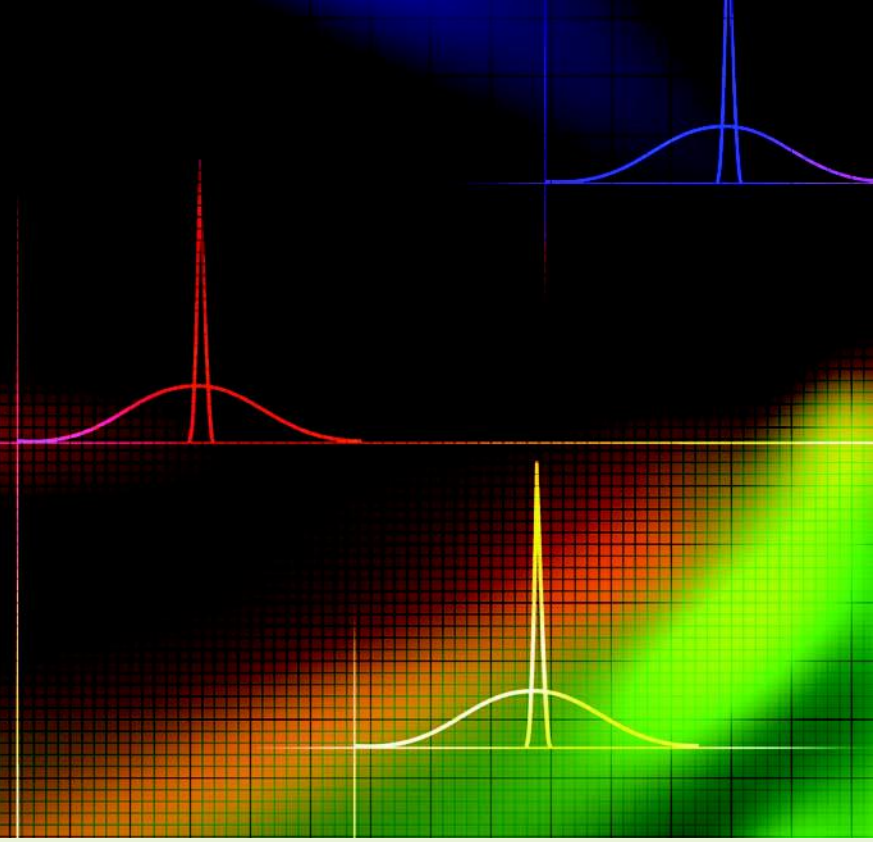

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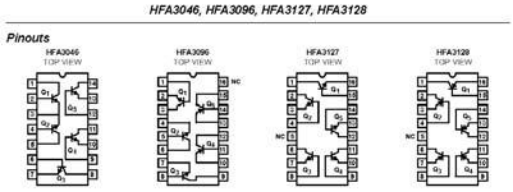
Spread spectrum: safe haven for wireless

Characterizing mixed-signal ICs for production

Forgotten circuits (that should be brought back)



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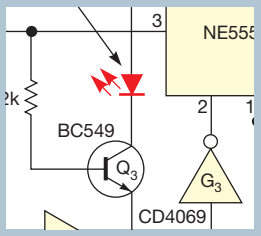

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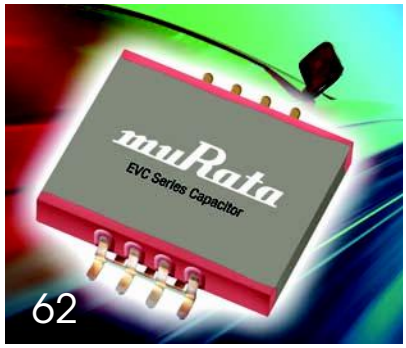
DEPARTMENTS & COLUMNS



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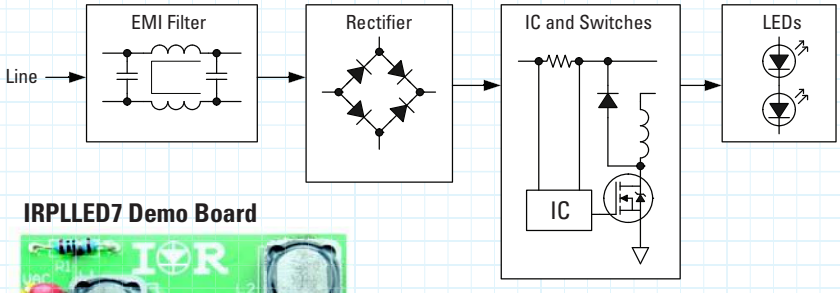
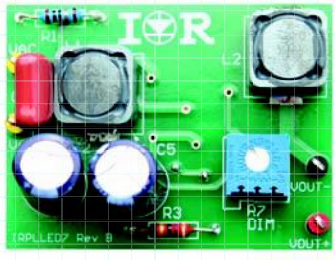
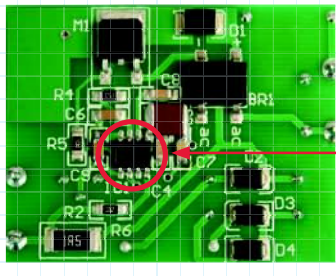
High-Voltage Buck Control ICs for Constant LED Current Regulation



IRPLLED7 Demo Board





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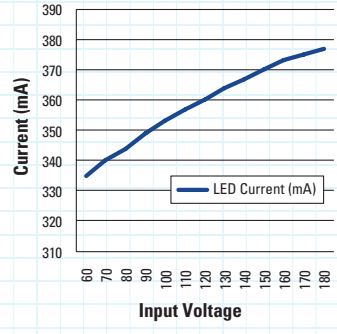
IRS2980

IRPLLED7 Demo Board
LED Current vs Input Voltage



IRS2980 Features

- Internal high voltage regulator
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- PWM dimming with analog or PWM control input
- Free running frequency with maximum limiting (150kHz)

IRS2980 Benefits

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- Off-line operation
- Very simple design
- Inherent stability
- Inherent short circuit protection

Demo Board Specifications

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- Output Voltage 0V to 50V (DC)
- Regulated Output Current: 350mA
- Power Factor > 0.9
- Low component count
- Dimmable 0 to 100%
- Non-isolated Buck regulator

Part Number	Package	Voltage	Gate Drive Current	Startup Current	Frequency
IRS2980S	SO-8	450V	+180 / -260 mA	<250 µA	<150 kHz
IRS25401S	SO-8	200V	+500 / -700 mA	<500 µA	<500 kHz
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JOIN THE CONVERSATION

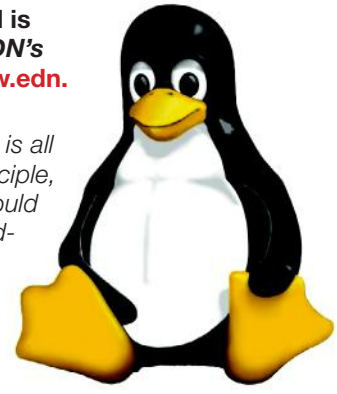
Comments, thoughts, and opinions shared by *EDN*'s community

In response to Bill Schweber's Power Points blog post "Wi-Fi appliance power control: Easy, but is it good?" at www.edn.com/4405262, David Sherman commented:

"The one mandatory requirement I'd like to impose on any engineer designing any such thing is that it have a mechanical 'disable' switch. In the case of fancy appliances that need software to operate, the switch would just disable the Web interface. This would be helpful for troubleshooting, as well as for security."

In response to "'Linux is obsolete' thread is started, January 29, 1992," an entry in *EDN's* tech-history blog, *EDN* Moments, at www.edn.com/4405860, przemek commented:

"This whole story illustrates why engineering is all about trade-offs and good judgment. In principle, microkernels have many advantages, and could be easily ported, but in actuality it was 'good-enough' Linux that _would_ get ported everywhere. It reached a commodity status: I have it on all our smartphones, and it is running on my TV, DVD player, and all wireless routers."

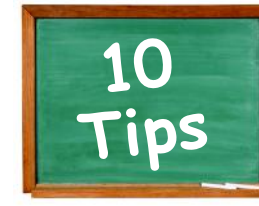


EDN *invites all of its readers to constructively and creatively comment on our content. You'll find the opportunity to do so at the bottom of each article and blog post.*

CONTENT

Can't-miss content on EDN.com

10 SOFTWARE TIPS FOR HARDWARE ENGINEERS



When transitioning from hardware design to include software design, here are 10 software tips that hardware engineers should keep in mind when they start developing software.

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ULTRA HDTV: A COMPLETE WASTE OF CONSUMERS' MONEY

There have been a lot of comparisons and contrasts between this year's "Ultra HDTV" hype and the "3-D TV" promotion of the not-too-distant past. But Ultra HDTV won't mean a darn thing once you get out of the electronics superstore and your nose is no longer pressed up against the display.

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FAMOUS PEOPLE YOU MAY NOT KNOW ARE ENGINEERS

We all have talents, and some of those talents outshine others. In late January, *EDN* took a look at six well-known, even famous, people who have an engineer's mind and skills but who have been acclaimed for talents other than engineering. Those six individuals—including rockers, starlets, and presidents—sparked conversation among the post's readers, who were eager to share in the comments section the names and bios of other "hidden" engineers. Are you aware of any others with engineering gifts who have been acclaimed for other achievements? Join the conversation and let us know. www.edn.com/4405678

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BY SUZANNE DEFFREE, EXECUTIVE EDITOR

Why your company's competitor won't hire you

Recent news from Silicon Valley courtrooms brings to mind the hit song "Hotel California," released in 1977 by American rock band the Eagles. Lead singer Don Henley has said that the song is about excess, but its famed "you can check out any time you'd like, but you can never leave" lyric is ringing true this month when it comes to employment in tech.

By now you've likely heard about the emails and documents brought to light by a recent case that alleges several technology companies—including Apple, Google, and Intel—violated antitrust laws by entering into formal or informal agreements to not recruit each other's employees (read.bi/W9j6B5).

In short, emails such as one from the late Steve Jobs to Google's Eric Schmidt, in which Jobs tells Schmidt that Google should stop recruiting in Apple's iPod group, are being produced as evidence that some companies adopted "no hire" policies. Under these policies, companies agreed not to hire one another's top talent, in some cases even if the employee was not being poached and was actively seeking new employment.

The case comes after a separate 2010 settlement in which the Department of Justice said some tech companies kept do-not-call lists to avoid competitive recruiting, and that such agreements restrained competition and hurt employees.

And it's reminiscent of a case that revolved around Mark Papermaster, an engineer who in 2008 was taken to court by his former employer, IBM, when he moved to Apple. IBM claimed Papermaster violated "noncompete" agreements he signed 26 years prior when accepting the IBM job that said he would not work for a Big Blue competitor for a year after leaving the company.

In the end, a ruling came down that stated IBM and Apple were competitors, even if their products played in entirely different fields, because both companies worked on devices that incorporated MPUs. In 2009, Papermaster was allowed to work at Apple, but not until six months after his IBM resignation and with a ball of additional strings attached.

All of these noncompete dealings, be they behind-the-curtain handshakes or legal documents engineers are forced to sign for mere employment, hark back to some pre-union work era when you signed up at a company to make enough to feed the family and stayed there until you retired (or died, whichever came first).

You can almost picture a sinister-looking character from HR, twirling his handlebar mustache with one hand and holding a noncompete agreement in the other, saying, "You can check out of the company anytime you like, but you can never leave for other employment at a company we see as a rival." And if IBM, focused on large-scale electronics, got away with claiming consumer-oriented Apple was a rival, any tech company could be considered another's competitor. Cue the guitar solo.

What makes these courtroom unveilings even more disturbing is that Apple and Google, the two biggest names in the case, are among the most pioneering and powerful companies in California, if not the world.

Allowing for different surroundings and environments can inspire new ideas and innovations. Hindering employees' abilities to move to the best positions for their skills will impede their growth, not to mention make for a slew of bitter employees.

How much more innovation would occur if employees and their ideas could move more fluidly from company to company, from industry pillar to start-up, from competitor to competitor? The argument Apple and the like will surely make is that keeping top talent in-house allowed them to create a steady stream of innovation while maintaining shareholder growth and overall value.

Such agreements instead force stagnancy upon companies looking to bring in new blood and cause employees locked into their present companies to mentally "check out," sticking around only for the paycheck. Any ethical HR person will tell you a dead-weight employee is not great for business, or coworker morale. Those who do manage to make it to the door, like Papermaster, remain weighed down by their former shackles for some time.

Extinction of noncompete and no-hire policies may be considered bad for business, but it could do wonders for engineering—not to mention for engineers looking to climb the career and salary ladder. And, while this is an oversimplification, when engineers and innovation grow, so does business.

What do you think? Share your thoughts on such agreements online at www.edn.com/4405856.EDN

Contact me at suzanne.deffree@ubm.com.

IMAGE: THINKSTOCK

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INNOVATIONS & INNOVATORS

Python speeds up GaN models

Anyone following developments in high-power RF knows that GaN is hot (pun intended). According to research firm Yole Développement, there is a great deal of R&D activity in this market. In March 2012, the company projected the power GaN market would grow to nearly $10 million in 2012 and $500 million in 2016—up from less than $2.5 million in 2010.

When new semiconductor processes are introduced, they are usually slowly integrated into device modeling and characterization tools. If a process takes off, however, the capabilities of the device modeling and characterization tools must keep pace, or even anticipate the needs of the new market. Agilent Technologies, for example, recently announced a new version of its Integrated Circuit Characterization and Analysis Program (IC-CAP) for high-frequency device characterization and modeling, offering parameter extraction, data analysis, instrument control, and interface responsiveness. It also now includes Angelov-GaN modeling and Python scripting. This announcement actually includes two noteworthy topics: GaN and Python.

Angelov-GaN is an industry-standard compact device model for GaN semiconductor devices. Since GaN devices typically operate at high power, it is important to be able to model thermal issues and their impacts on device characteristics. Designers working with GaN quickly realized that GaAs models were not good enough. Fortunately, Professor Iltcho Angelov at Chalmers University of Technology (Gothenburg, Sweden) developed his Angelov-GaN model as an alternative.

In IC-CAP 2013.01, Agilent has embraced the Angelov model with the W8533 Angelov-GaN extraction package. An interface lets users execute a step-by-step extraction flow to obtain model parameters. A turnkey flow aims to provide quick-start modeling of GaN devices.

The Agilent product uses Python scripting. Why Python? The Python program may soon lay claim to the title of most used interpreter language. Roberto Tinti, device modeling product manager with Agilent EEsof EDA, thinks an advantage of Python is the support of a large, open-source community. "Some of our major customers have started to use Python for their projects," says Tinti, "and we decided to support it natively in our platform in addition to our own native language, called PEL." Python is 100× faster than Agilent's Programming Extraction Language, the language that IC-CAP users have been using to customize their applications.

The new IC-CAP release includes support for Smartspice simulations, as well as support for gain compression and two-tone intermodulation distortion measurements with Agilent's PNA-X network analyzer. The software is available for download at http://bit.ly/YIRSFV.

—by Janine Love

▷**Agilent Technologies**, www.agilent.com

In Agilent's Angelov-GaN extraction package, an interface lets users execute a step-by-step extraction flow to obtain model parameters.

TALKBACK

"I'm all for making things better and utilizing technology to do so, but what parts of our soul do we lose in the process?"

—Commenter Calibrator, in response to Pallab Chatterjee's blog post "What will be in the auto black box?" at www.edn.com/4404670. Join the conversation and add your own comment.

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Dreamlining Boeing and batteries

You've undoubtedly seen the news that various fleets of Boeing's 787 Dreamliner, which recently went into service, have been temporarily grounded while an apparent problem with some of its battery sets is checked out. (There have also been some fuel leaks, but that's another story.) Among the battery issues was a smoke-filled locker and fire damage that occurred when a plane was parked on the runway.

> Any engineer knows that what appears to be 'the problem' often is just a misleading manifestation of the real problem elsewhere.

I'm not going to jump to conclusions about the problem or the cause. Any engineer with any experience knows that what appears to be "the problem" often is just a misleading manifestation of the real problem elsewhere, while the actual root cause (or causes) is frequently buried somewhere down the line in a long chain of events. Just because you see smoke doesn't mean that there's a fire where you think it is, so to speak.

There's no doubt that a lot of advanced battery technology can be found in the 787. An excellent article from *The Wall Street Journal*, "Dreamliner-like batteries raised concerns" (on.wsj.com/U9xwV9), and its associated graphic show how the Dreamliner 787 uses lots of electrical power for actuators and more, compared with earlier aircraft.

Why? That question is easy to answer: In order to reduce weight and get the benefits of electronics and advanced algorithms, much of the conventional hydraulic power and control of the aircraft has been replaced by electrically based power and control—and with advanced electronics and software, of course. (Plus, the airframe is also largely made up of composites, instead of conventional aluminum, for reduced weight.)

These electrical systems require lots of batteries for start-up, backup, and even operation. The preferred rechargeable energy-storage technology for the batteries utilizes lithium-based chemistry. This makes sense, since lithium offers much, much higher energy density (by weight and volume) than any other available battery chemistry.

But much more so than with older chemistries such as nickel cadmium, lithium cells also need lots of careful attention when charging and discharging. In addition, their energy density is so high that there's a lot of stored energy in that small volume, and a failure such as an internal short can result in huge current flows and subsequent fires or even explosions. (Note several well-documented instances of laptops catching fire even though they were "off" and not even plugged into their ac-line chargers.)

So we have the typical engineering situation of a tricky trade-off. We want the benefits of lower weight, greater efficiency, higher energy density, and so on, but we also have to accommodate and anticipate all of the implications of the technology that makes these benefits possible. And as all engineers know, you can't plan for everything, so you also have to have some independent, overall watchdogs in case something happens that you didn't think of, or didn't plan for.

It's also true that while lithium chemistry has such high density and subsequent danger, just remember that hydrocarbons such as gasoline have far greater energy density than the best batteries, yet we have managed to make that explosive technology into a safe energy-storage medium and power source.

Of course, the same politicians and activists who want engineers to perform miracles and deliver it all—better efficiency, lower weight, better products—will also be the first to scream and point fingers (and maybe lawsuits) when they don't get everything they wanted, and perhaps were promised. Once again, no good deed goes unpunished.

—by Bill Schweber

▷**Power Points blog**, www.edn.com/4405458

DILBERT By Scott Adams

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Anticipate — Accelerate — Achieve

Agilent Technologies

TI claims industry's lowest-phase-noise frequency synthesizer

Texas Instruments has introduced a wideband frequency synthesizer with integrated voltage-controlled oscillator (VCO) that delivers what the company claims is the industry's lowest phase noise. The LMX2581 allows designers to use one frequency synthesizer to support a variety of demanding applications in wireless infrastructure, radar, medical imaging, defense and aerospace, and test and measurement.

A phase-detector frequency of 200 MHz and an ultralow phase-locked-loop (PLL) normalized phase noise of –229 dBc/Hz provide a precision local oscillator to an RF front end for better receiver sensitivity. Integrated VCOs allow the device to output frequencies from 50 to 3760 MHz, eliminating the multiple VCO/PLL combinations typically required to support a broad range of applications. The LMX2581 also gives designers the option to bypass its internal multicore VCO in favor of an external VCO.

The ultralow-noise, wideband frequency synthesizer integrates a delta-sigma fractional-N PLL; a multicore VCO with tank circuit; an optional frequency divider; two differential RF output buffers that can deliver 10 dBm single-ended on each side; and several low-noise, high-precision low-dropout regulators. This integration reduces BOM costs.

A phase-detector frequency of 200 MHz and a PLL normalized phase noise of –229 dBc/Hz in TI's LMX2581 frequency synthesizer provide a precision local oscillator to an RF front end for better receiver sensitivity.

> Integrated VCOs allow the device to output frequencies from 50 to 3760 MHz.

The LMX2581EVAL evaluation module can be purchased for $175. The synthesizer's companion Clock Design Tool and CodeLoader software help speed system design by aiding engineers with product selection, loop filter design, and simulation of timing solutions.

The LMX2581 is available now in a 32-pin, 5×5-mm QFN package for a suggested retail price of $7 (1,000).

—by Steve Taranovich

▷**Texas Instruments**, www.ti.com

02.13

Peel-and-stick solar cells circumvent several fabrication challenges

Researchers at Stanford University, the National Renewable Energy Laboratory, and Hanyang University claim to have developed the world's first peel-and-stick thin-film solar cells that don't require any modification of existing processes or materials. The new process would allow the creation of decal-like solar panels that could be applied to virtually any surface.

Unlike with standard thin-film solar cells, the new process doesn't require direct fabrication on a final carrier substrate. Instead, a 300-nm film of nickel (Ni) is deposited on a silicon/silicon dioxide (Si/SiO_2) wafer, on which thin-film solar cells are then deposited using standard fabrication techniques and covered with a layer of protective polymer. A thermal-release tape is then attached to the top of the thin-film solar cells as a temporary transfer holder.

Peeling the cells from the wafer involves soaking the structure in a water bath, during which the thermal-release tape is slightly peeled back, allowing water penetration into the Ni and SiO_2 interface, which results in its separation and the peeling off of the thin-film solar cells from the Si/SiO_2 wafer. When the solar cells are ready to be applied to a surface, the thermal-release tape holding them is heated at 90°C for a few seconds to weaken its adhesion, allowing the cells to be removed. The cells can then be applied to various surfaces—including plastics, paper, glass, metal foils, and textiles—using common adhesives.

Tests have shown that the peel-and-stick thin-film cells remain completely intact and functional, with no loss of the original cell efficiency. Looking beyond solar cells, the researchers believe the process could also be applied to thin-film electronics, including printed circuits, ultrathin transistors, and LCDs. For more information, see the original paper, published in *Scientific Reports,* "Peel-and-Stick: Fabricating Thin Film Solar Cell on Universal Substrates" (bit.ly/XNRZcA).

—by Rich Pell

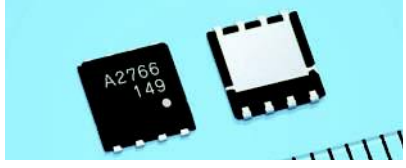
▶**Stanford University**, www.stanford.edu
▶**National Renewable Energy Laboratory**, www.nrel.gov
▶**Hanyang University**, www.hanyang.ac.kr

Renesas power MOSFETs deliver 50% lower on-resistance

Renesas Electronics has started to sample three new low-on-state-resistance MOSFET products, including the µPA2766T1A, optimized for use as ORing FETs in power-supply units for network servers and storage systems.

Featuring ultralow on-state resistance of 0.72 mΩ (typical) for 30V—about 50% lower resistance compared with the company's earlier products—and a high-efficiency, small-surface-mount package (8-pin HVSON), the products enable high-current control, contributing to power savings and miniaturization of the power units used for comparably large-scale server storage systems.

For mission-critical systems, it is common to provide redundant power delivery, for example, by ORing FETs with multiple power units that maintain high reliability. These ORing FETs are connected to the power output lines of each of the power-supply units. They remain in the on state during normal operation, but if one of the power-supply units fails, the ORing FETs of that unit switch to the off state to isolate them from the other power-supply units and ensure that system power is not disrupted.



Three new power MOSFETs from Renesas feature on-state resistance of 0.72 mΩ (typical) for 30V.

During normal operation, the power output lines handle large currents of several tens to several hundreds of amperes. The ORing FETs must have low on-state-resistance characteristics to prevent an increase in conduction loss or a drop in the power-supply voltage.

Sample pricing is $1.20, $1, and $1.80 per unit for the µPA2764T1A, µPA2765T1A, and µPA2766T1A, respectively. Mass production was scheduled to begin this month. **—by Ismini Scouras**

▷**Renesas Electronics Corp**, am.renesas.com

Microsemi expands SiC power-module product family

Microsemi has started to sample a new generation of industrial-temperature, silicon-carbide (SiC) standard power modules aimed at high-power switch-mode power supplies, motor drives, uninterruptible power supplies, solar inverters, oil exploration, and other high-power, high-voltage industrial applications requiring high performance and reliability. The power-module family is also offered with extended temperature ranges to meet next-generation power-conversion system requirements for higher power densities, operating frequencies, and efficiencies.

SiC technology delivers higher breakdown field strength and improved thermal conductivity compared with silicon material. The result is improved performance characteristics, including zero reverse recovery, temperature-independent behavior, higher voltage capability, and higher-temperature operation.

Microsemi's new SiC power modules feature multiple circuit topologies and are integrated into low-profile packages. The majority of the new module product family uses aluminum-nitride substrates to enable isolation from the heat sink, which improves heat transfer to the cooling system. Additional features include high-speed switching, low switching losses, low input capacitance, low drive requirements, a low profile, and minimum parasitic inductance, which enable high-frequency, high-performance, high-density, and energy-saving power systems.

The company's SiC product portfolio includes Schottky diodes in both discrete and module packages, and power modules with a mix of SiC Schottky diodes and IGBT or MOSFET transistors in both standard and custom configurations.

—by Ismini Scouras

▷**Microsemi Corp**, www.microsemi.com

02.13

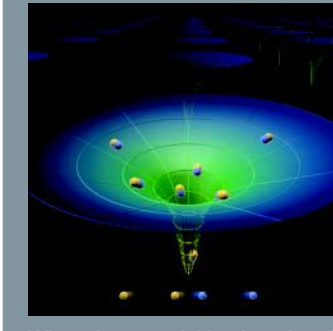
CAPTURING MORE OF THE SUN'S ENERGY

Researchers at the Massachusetts Institute of Technology have proposed a more efficient way of capturing photons for electricity. Their concept, the solar energy funnel, is based on manipulating elastic strain in new "ultrastrength" optoelectronic materials so that the materials can capture and more efficiently collect a broader range of the solar spectrum.

The researchers used computer modeling to determine the effects of strain on molybdenum disulfide (MoS_2), a material that is capable of forming a layer just a single molecule thick. When the material is placed under strain in the solar energy funnel configuration—using a microscopic needle to poke it down at the center—its bandgap varies across the surface so that different parts of it respond to different colors of light, and the resulting photoexcited charge carriers are conveyed and concentrated in the center for collection.

The researchers hope to be able to carry out laboratory experiments at some point to confirm the effect.—by Rich Pell

▶**MIT,** www.mit.edu



When the material is placed under strain in the solar energy funnel configuration, its bandgap varies across the surface, and the resulting photoexcited charge carriers are conveyed and concentrated in the center for collection (courtesy MIT).

BY HOWARD JOHNSON, PhD

Make it better

The circuit in **Figure 1** includes a plethora of termination options. The **figure** shows four results using various combinations of component values, each observed at the point indicated by the purple arrow.

In the first three results, resistor R_2 is replaced with a 0Ω short, and resistor R_3 is not installed. This is a classic series-terminated approach using only resistor R_1, having values of 33, 18, and 4.7Ω, respectively.

Looking at the rising edges, the signal in each case fails to achieve full strength on the first stroke, as indicated by the "plateau" marking on each waveform. In each case, subsequent reflections at 2-nsec intervals push the signal voltage up toward its 3.3V limit. As the value of R_1 is successively reduced, the first stroke becomes more powerful, climbing higher toward the goal of first-incident-wave perfection but never quite achieving it. Even with R_1 set to 0Ω, this driver will never achieve perfection when driving a 50Ω line, because the effective driver output resistance, R_S, is greater than 50Ω.

The falling edges tell a different story. With R_1 set to 33Ω, the initial drop in the falling waveform is 2.7V—a larger step than the first step in the rising waveform. That clue tells us the driver output resistance in the falling direction must be *less than* the output resistance in the rising direction, a common situation in CMOS totem-pole drivers. In the third waveform, by the time R_1 is set to 4.7Ω, the signal undershoots significantly. The driver in this case is too powerful.

If your driver output resistance varies between its rising and falling edges, as it often does, then no value of series-terminating impedance can possibly make both edges perfect—but perhaps you can make it better.

A higher value of line impedance helps. To see why, suppose that your driver has output resistances of 60 and 37Ω in the rising and falling directions, respectively, as in this example. Mate that to a transmission line with a characteristic impedance of 10,000Ω using a series resistor of 9,951Ω. The effective impedances in the two driving directions are now 10,011 and 9,988Ω, respectively—very close matches to the line impedance.

Of course, you can't make such a circuit, but even raising your transmission-line impedance to 65Ω permits a higher value of R_1, making R_1 a more significant part of the circuit and thus reducing the impact of variations in the natural output resistance of your driver.

A slower edge helps. The signal rise and fall time now is about 1 nsec. Some FPGA drivers have a facility for slowing the edge-transition time, which would be ideal. If you don't have that, try inserting R_2=50Ω or more in series with the receiver (fourth waveform). That additional resistance, working into the 9-pF capacitance of the receiver, forms a lowpass filter that can lengthen the edge-transition times, reducing the amount of undershoot in the falling direction and making the waveform less sensitive to natural variations in the driver's output impedance. EDN

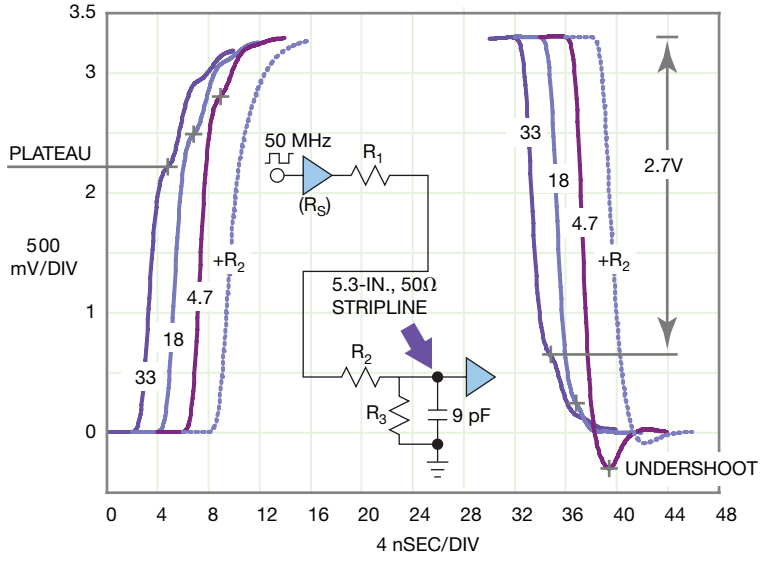


Figure 1 With R_1=4.7Ω, adding R_2=50Ω lengthens the signal-transition times, smoothing the signal and limiting the undershoot.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his website at www.sigcon.com.

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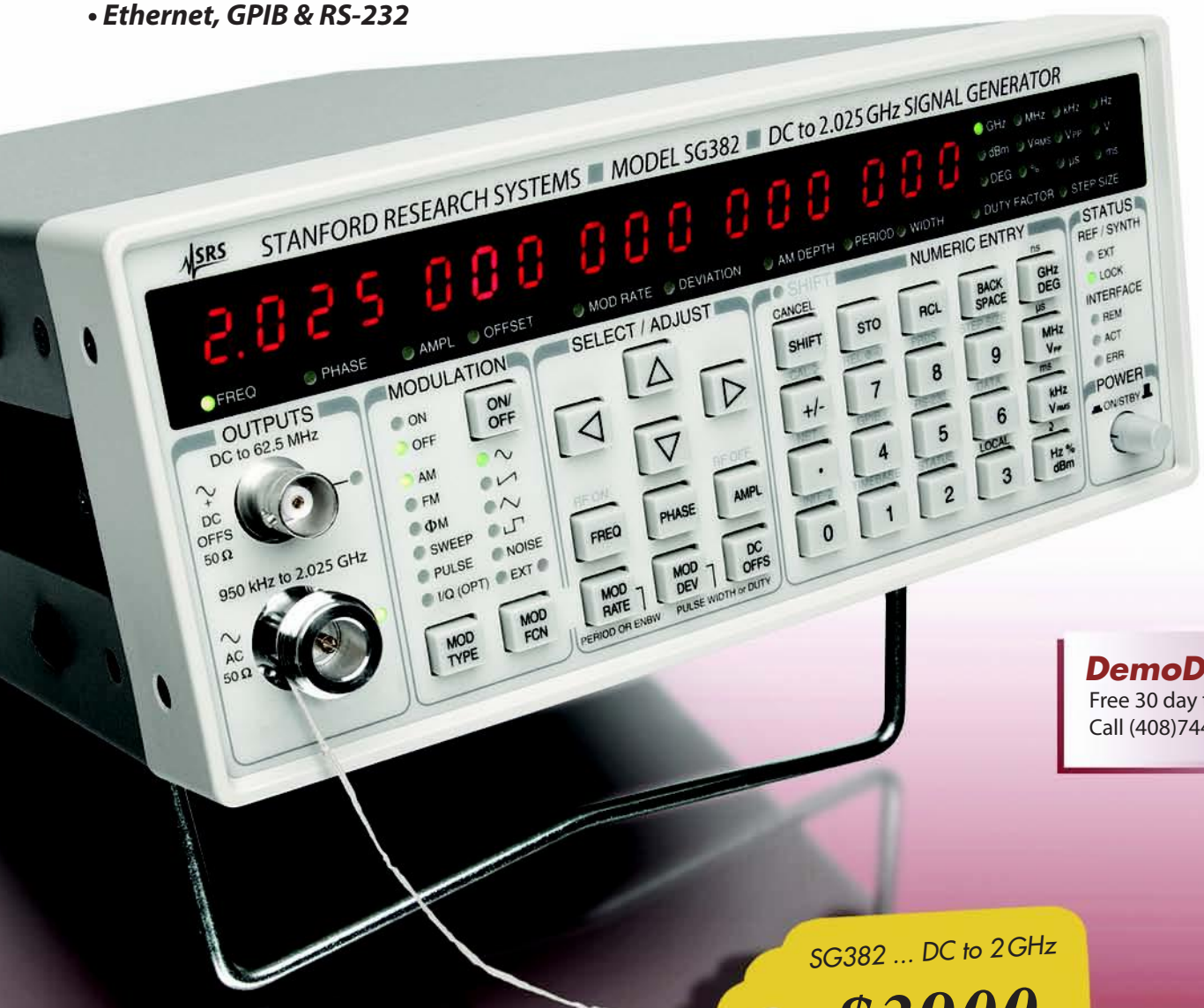

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BY BONNIE BAKER

Take advantage of an online design tool's extended transimpedance features

Companies are cutting engineering resources while still expecting teams to meet tightened product-development deadlines. Designers need to organize their thoughts and approach this problem aggressively with an arsenal of design weapons. Worthy design tools can encompass the analog/digital simulation models, such as SPICE and IBIS, along with higher-level tools that offer comprehensive circuit-design solutions.

For example, a common but not-so-simple design of a photodiode circuit[1] is available online for your use.[2] This tool provides a complete solution (**Figure 1**), including a bill of materials and a protoboard that you can order.

The solution shown in the **figure** is great if you're designing a complete system, but if you are looking for just a transimpedance-amplifier solution, I suggest that you look a little closer at the website tool. The software user can elect to use only the transimpedance-amplifier circuitry in the final design.

As a first step, evoke the software on the Web and create a full photodetector system. The circuit's complete system-specification page is embedded in the *Operating Values, Performance* view. (From the front page, select *Photodiode*, then click *Start Design* → *Start Design* → *Operating Values, Performance*.) This page includes the system SNR, total output noise, and analog-signal and system bandwidths. Note the analog-signal bandwidth of 330 kHz for this first design.

You are now ready to design your own transimpedance-amplifier circuit with a higher analog-signal bandwidth. You can access the list of amplifiers by clicking on *View Design Summary* → *Schematic* → *Change Op Amp A1*. In this view, you have a list of amplifiers with the lowest gain-bandwidth product (GBWP) at the top. Choose any operation amplifier from this list. If you select the OPA354, with a GBWP of 250 MHz, the analog-signal bandwidth in the *Operating Values, Performance* view will be 3.859 MHz. This new analog-signal bandwidth opens the door for higher-speed systems, higher-resolution systems, or both.

This type of application site is indicative of what is in store for the analog hardware designer now and in the future. The Webench pages available now are not just ordinary text pages, as they provide a library of common-sense design equations, rules, and tips, along with robust, up-to-date product-selection lists. The interactive Webench algorithms tap the expertise of numerous analog experts around the world. These design tools can provide intuitive evaluations for constraints such as power dissipation versus BOM costs versus the footprint size of your circuit.

This type of application site is indicative of what is in store for the analog hardware designer.

The most valuable part of this type of Webench page is that it is there for the long term. This "workforce" does not retire, move to another job, or go home in the evening. It is at your beck and call 24/7. EDN

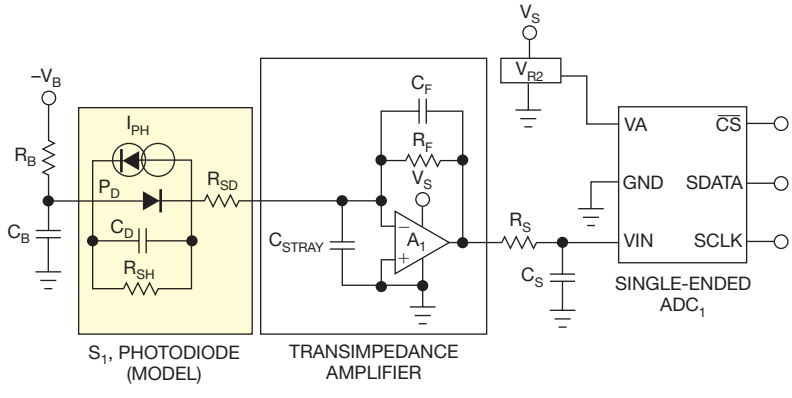


Figure 1 This reference solution for a complete photodetector-system signal path uses a photodiode, transimpedance amplifier, and successive-approximation-register ADC; but what if you need just a transimpedance-amp solution?

REFERENCES

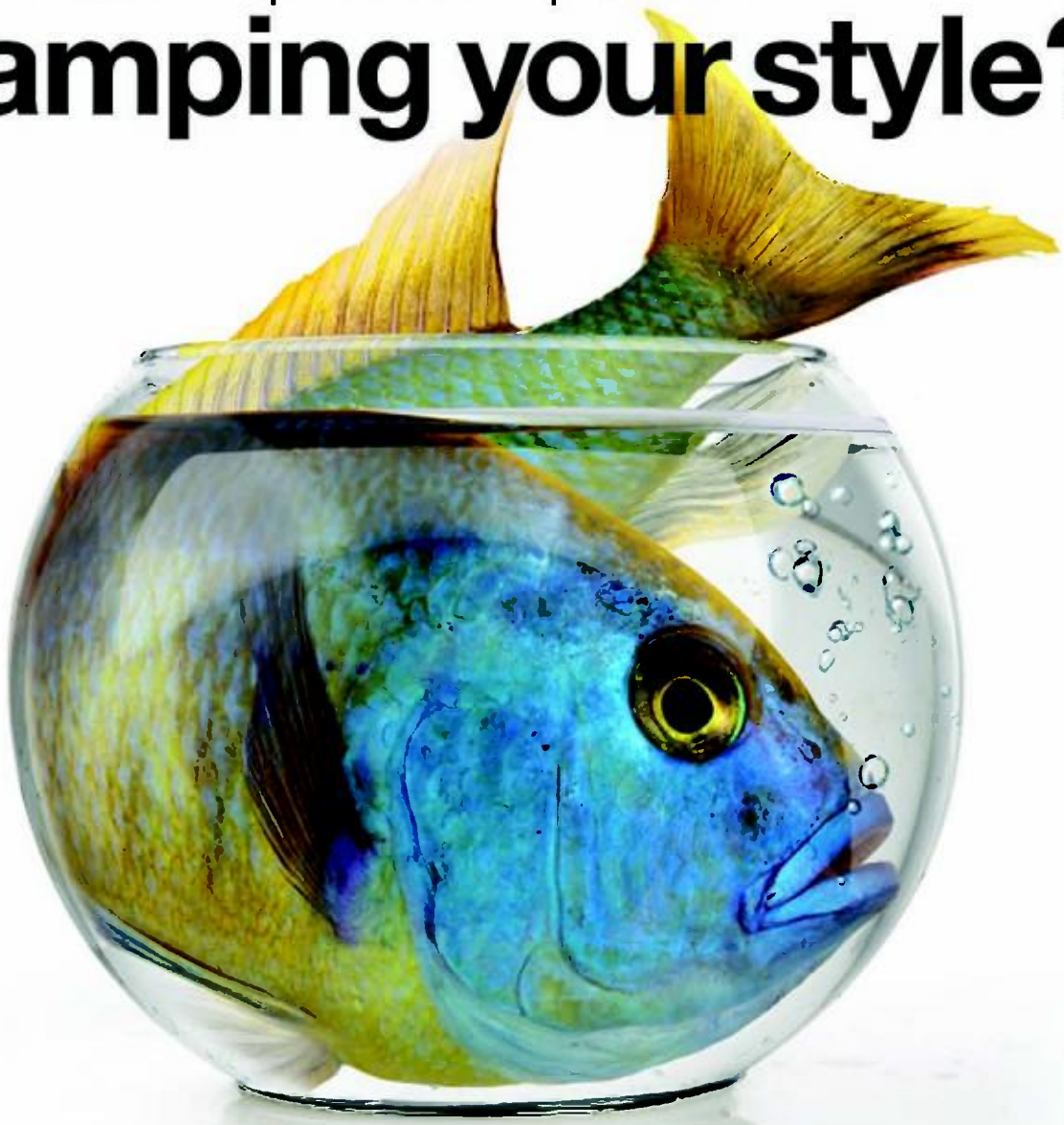
1 Ramus, Xavier, "Transimpedance Considerations for High-Speed Operational Amplifiers," Texas Instruments, Nov 2009, http://bit.ly/XyxmDK.
2 Webench Sensor Designer tool, Texas Instruments, http://bit.ly/V66Rsv.

Bonnie C Baker is a senior applications engineer at Texas Instruments.

TDK

Are limited capacitor options

cramping your style?



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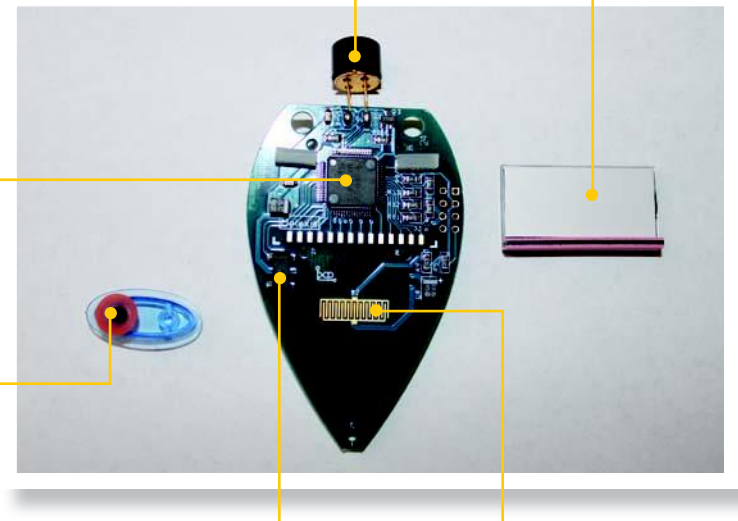
Thermometer measures temperature without contact

The Melexis infrared (IR) thermometer makes it safe to measure the surface temperatures of hot, hazardous, or hard-to-reach objects without having to physically touch them. (Omega Engineering's website provides an introduction to IR thermometers: http://bit.ly/VlTS0B.) Simply aim and push the front-panel button to display the remote temperature (in your choice of °C or °F) in less than a second. Pressing the button a second time will freeze the measured value on the display. The value will continue to flash until the button is again depressed, making the device ready for another temperature measurement. Aside from a few minor issues with the front-panel button, I found the device fairly easy to use.

The MLX90614 IR sensor is built from two chips developed and manufactured by Melexis: the MLX81101 IR thermopile detector and the MLX90302 signal-conditioning ASSP, which is specially designed to process the output of the IR sensor. The sensor is housed in a TO-39 can, which also comprises an integrated low-noise amplifier, 17-bit ADC, and DSP. The IC's digital 10-bit PWM is configured with a digital SMBus output to continuously transmit the measured temperature. The sensor is precalibrated for an object emissivity of 0.95.

LCD removed from the circuit board.

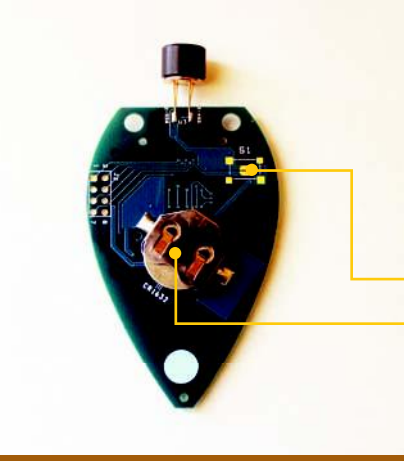
The MSP430F413 16-bit ultralow-power microcontroller has 8 kbytes of flash, 256 bytes of RAM, a comparator, and a 96-segment LCD driver to drive the display. The microcontroller takes the IR sensor's DSP PWM signal and converts it to degrees Celsius or degrees Fahrenheit when the front-panel switch signal is sensed.



A rear view of the front-panel switch cap with conductive elastomer to activate the resistor array.

32,768-Hz oscillator for the MSP430.

Switch resistive array.



A rear view of the circuit board shows the 3V, CR1632 replaceable coin-cell battery in its holder, as well as the reset-switch circuitry.

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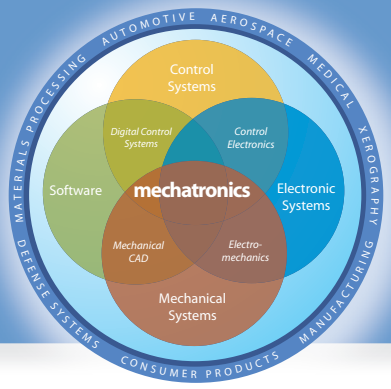

Inertia mismatch: fact or fiction?

Is this often-quoted concept an excuse for inadequate system modeling?

By Kevin C Craig, PhD

Servo systems may be direct drive or geared. For geared systems, the motor selection also involves a choice of gear ratio. **Figure 1** shows a motor connected to a load through an ideal (that is, no friction, no backlash, and no compliance) gear train with gear ratio N. The equation of motion for this one-degree-of-freedom system is shown in terms of the load angular velocity, ω_L.

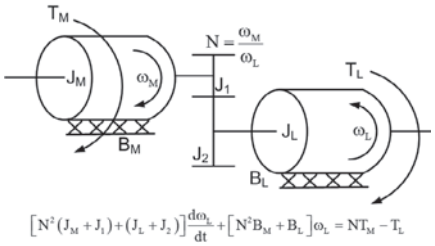

Figure 1 A motor is connected to a load by an ideal gear train.

The inertia ratio is the ratio of the load inertia to the motor inertia, J_L/J_M. What is the optimum value of this ratio for a particular value of N? If you ignore the motor and load damping, B_M and B_L, respectively, and the load torque, T_L, the inertia ratio that maximizes the power transferred from motor to load is N^2—that is, the reflected motor inertia equals the load inertia.

When friction and load torques and system compliance (for example, coupling or timing-belt compliance) are significant, the selection of an optimum inertia ratio is less straightforward. **Figure 2** shows this more general case.

Why do deviations from the so-called ideal inertia ratio of N^2, called inertia mismatch, often cause servo-system stability problems, particularly in compliantly coupled systems? This is a system question, and to answer it you must examine the frequency-response plot for a compliantly coupled motor and load, as shown in **Figure 3** (N=1, B_M=0, B_L=0).

The anti-resonance frequency, ω_{AR}, always occurs before the resonance frequency, ω_R. At a low J_L/J_M ratio, the resonance and anti-resonance frequencies are close to each other at a high frequency. As J_L/J_M increases, both the anti-resonance and resonance frequencies decrease, with the anti-resonance frequency decreasing at a faster rate. For a given J_L, to increase the resonance frequency, you need to either increase the shaft stiffness, K_S, or decrease the motor inertia. As K_S increases, both ω_R and ω_{AR} increase. The smaller the inertia ratio, the less the compliance will affect the system.

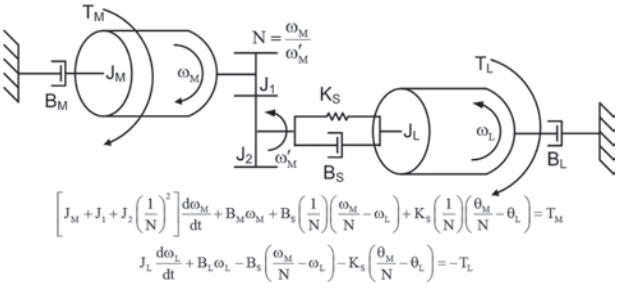

Figure 2 A motor is connected to a load by an ideal gear train with compliance.

All mechanical systems have compliance. You should base your choice of inertia ratio and transmission ratio (for example, gear, belt, or lead screw), as well as the design of the feedback-control system, on a system analysis and not on poorly defined rules of thumb. EDN

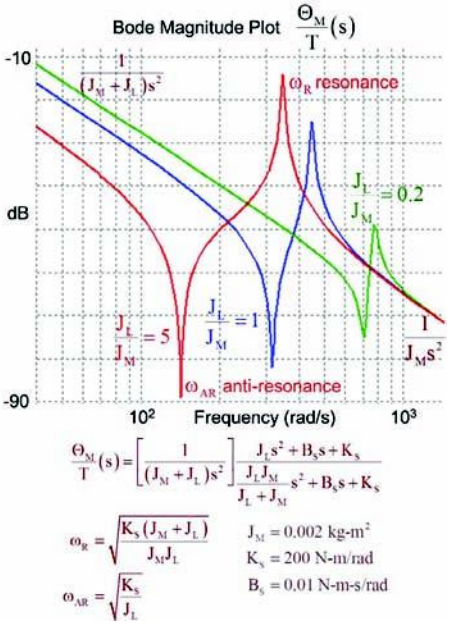

Figure 3 In a compliantly coupled motor and load, the anti-resonance frequency, ω_{AR}, always occurs before the resonance frequency, ω_R.

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CHARACTERIZING MIXED-SIGNAL ICs FOR PRODUCTION

WHAT YOU DON'T TEST CAN HURT YOU.

BY ROBERT SEITZ • AMS AG

IMAGE: SHUTTERSTOCK

An integrated circuit entering production must be available in high volume to meet the potential demand. Even though bench testing may show good results, in production the device must be tested with automated test equipment (ATE). What's more, before the design's release to production, it must undergo thorough characterization to verify that every tested device will fully meet its electrical specifications, as well as to uncover any process defects that could appear during the fabrication process. Here, we focus on mixed-signal device characterization, examining statistical techniques that ensure repeatability of test results, including testing over an IC's rated temperature extremes.

REPEATABILITY

Before releasing a device and its test solution to production, you must verify that the test solution itself is both accurate and repeatable. Gauge repeatability and reproducibility (GR&R) is a measure of the capability of a gauge or tester to obtain the same measurement reading every time the measurement is taken, and thus indicates the consistency and stability of the measuring equipment. Mathematically, it is a measure of the variation of a gauge's measurement. Engineers must try to minimize the GR&R numbers of the measuring equipment, since a high GR&R number indicates instability and is thus unwanted. Reduced GR&R is a means of checking the repeatability of the test program.

Part of the procedure is to test multiple sites on a wafer and to do so multiple times. It's important to note that only the actual active site should be powered. This avoids possible influence from other sites, such as crosstalk or interference from RF signals that could adversely affect test results.

Let's assume you will test each site 50 times. With this approach, a 16-site test solution produces 800 (16×50) test results. The overall results can show a possible discrepancy between sites. You can then calculate the standard deviation and process capability index (Cpk) across all sites. The goal is to ensure a good, repeatable test program.

AT A GLANCE

- Gauge repeatability and reproducibility, or GR&R, is a measure of the capability of a gauge or tester to obtain the same measurement reading every time the measurement is taken.
- Testing at room temperature is necessary and important, but it's even more important to test key parameters over a device's fully specified operating temperature range.
- In addition to testing at the wafer level, you also have to test packaged parts to determine that no damage has occurred during the packaging process.

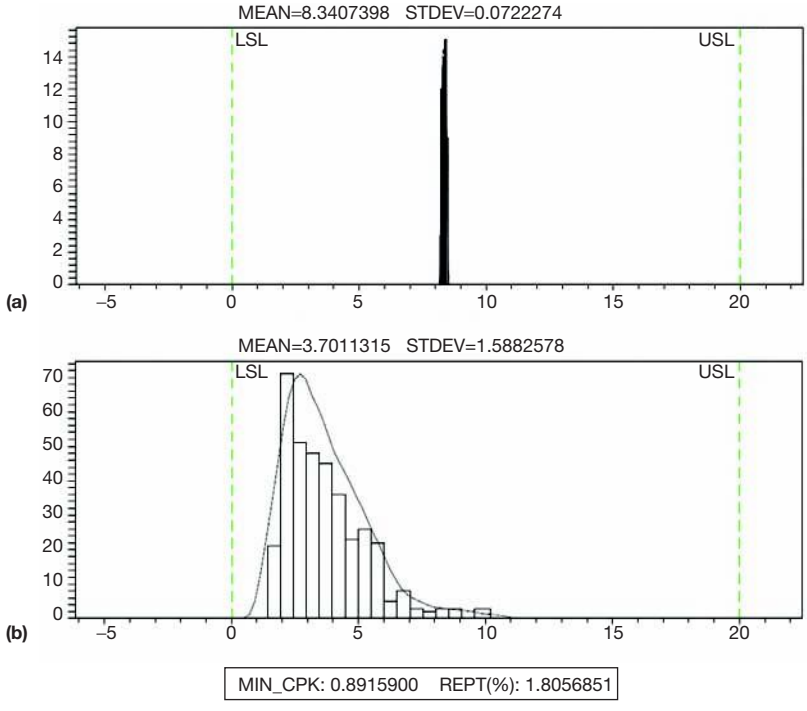


Figure 1 A reduced-repeatability-and-reproducibility report such as this one can provide the data to judge a measurement's accuracy and stability. Here, one part is tested 100 times on ATE (a), and 300 parts are tested one time on ATE (b). LSL is the lower spec limit; USL is the upper spec limit.

Figure 1 shows a comparison between one part tested 100 times on ATE and 300 parts tested one time on ATE. A reduced-repeatability-and-reproducibility report such as the one shown in the **figure** can provide you with the data to judge a measurement's accuracy (of the measurement range, for example) and stability.

To summarize the test sequence:

- One site is tested 50 times. All other sites are disabled (not powered) during test.
- Approximately 300 parts are tested with ATE to provide a comparison of lot variance with device repeatability.
- Statistical tools are used to analyze the data.

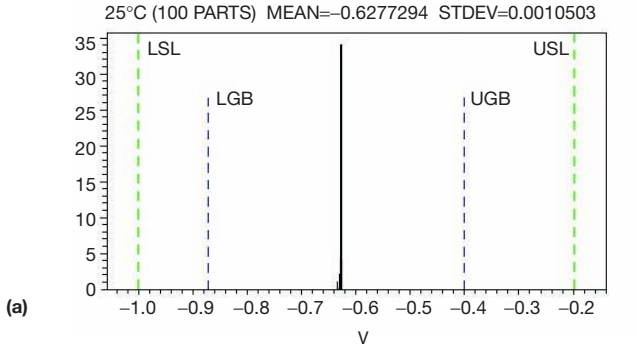
The measurements on the tester must correlate with the measurement results in the lab. In each situation, the project team must define the number of correlation devices and the parameters to be tested. This correlation can be started as soon as the test program is debugged and stable. At least 10 devices should be tested to guarantee that the data is correlating.

CPK CALCULATION

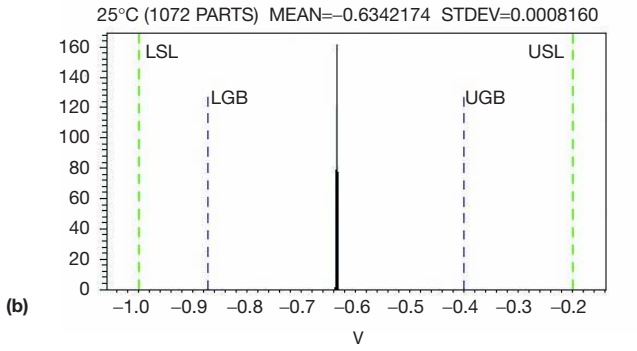
The process-capability-index value—defined from the mean value, the standard deviation (sigma), and the upper and lower specification limit—is an indication of how well the test parameter is under control with respect to its limits. For many devices, a desirable Cpk value would be 1.33, which would indicate a repeatability value of three times sigma. For automotive devices, however, a Cpk value of 2.00 would be preferable because of the Six Sigma rule.

TEMPERATURE TESTING

Testing at room temperature is necessary and important, but it's even more important to test key parameters over a device's fully specified operating temperature range. Temperature characterization shows the stability of the device over the specified operating temperature range. You should test approximately 300 parts at three previously defined temperatures; in addition, one part must be tested 100 times at three temperatures in order to calculate drift over temperature. You can use the resultant data to calculate temperature guard bands.



(a)



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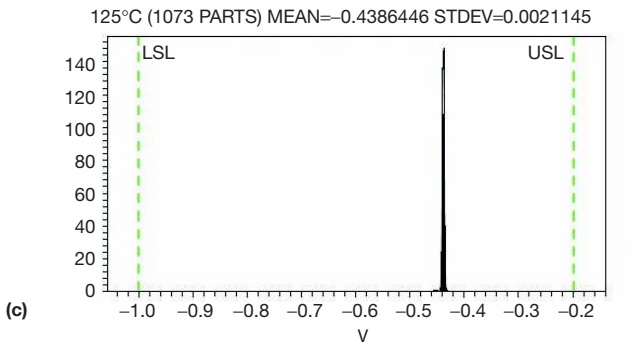

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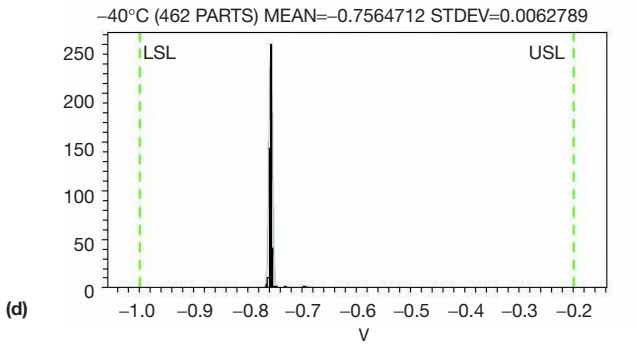

(d)

Figure 2 This sample temperature-characterization report includes guard bands. The Y axis represents the number of parts; the X axis shows the measured value. Characterization is shown for 100 parts tested at +25°C (a), 1072 parts tested at +25°C (b), 1073 parts tested at +125°C (c), and 462 parts tested at –40°C (d).

MORE ON GUARD BANDS

In general, test engineering uses two kinds of guard banding: one for repeatability and one for temperature. There are both pros and cons to their use.

Engineers turn to repeatability guard bands to deal with the uncertainty of each measurement. The following example looks at drive current:

Segment drive source current:
37 mA (min), 47 mA (max)
LGB limit = lower spec limit + ε
=> 37.37 mA
UGB limit = upper spec limit – ε
=> 46.53 mA

Here, LGB is the lower guard band, UGB is the upper guard band, and ε is the uncertainty of the measurement.

The disadvantage of using repeatability guard bands is that a good device can be rejected as a bad device because of the uncertainty that the example demonstrates. The ideal case would be to use a guard-band limit of zero so that no good parts would be rejected. To reduce the impact of the guard band, you can improve the stability if the resulting measurement is a smaller repeatability guard band. The disadvantage would be a much longer test time due to device-settling time, an inherent issue with analog and mixed-signal ICs.

Every device, meanwhile, has a specified drift over temperature, which may be a typical or a guaranteed minimum/maximum specification. Temperature guard bands have tighter test limits than the IC's data-sheet specifications and need to be calculated based on the drift of the measurement over temperature. The advantage of using temperature guard bands is that you can skip test stages at other temperatures and instead calculate, based on the test results seen at room temperature, whether a device would fail at temperature extremes.

Figure 2 shows a temperature-characterization report with guard bands included. The plots demonstrate that there is drift over temperature. From this data, you must be able to predict that when testing production parts at +25°C, the drift at the temperature extremes will be within specification limits. That is the point of temperature guard bands for production testing.

Silver samples are often used to show the stability of the test solution over temperature. They also can be stored for use as reference parts for later verification of the test solution. The testing procedure for these devices is to test three parts at three temperatures, hundreds of times each.

Using the gathered data, you can prove the stability of every device with the help of a statistical report tool. For example, a double distribution or instability can be seen immediately. You can keep the test results for later reference, comparing future measurements with the stored data.

Assume the device to be tested has the following operating conditions: a minimum operating temperature of –40°C, a typical operating temperature of +25°C, and a maximum operating temperature of +125°C. The black bar in the graph in **Figure 3** is the value at room temperature. The green bar shows the value at high temperature (+125°C); the blue bar shows the value at cold temperature (–40°C). The data clearly shows an increase and decrease of the value at high and low temperatures, respectively.

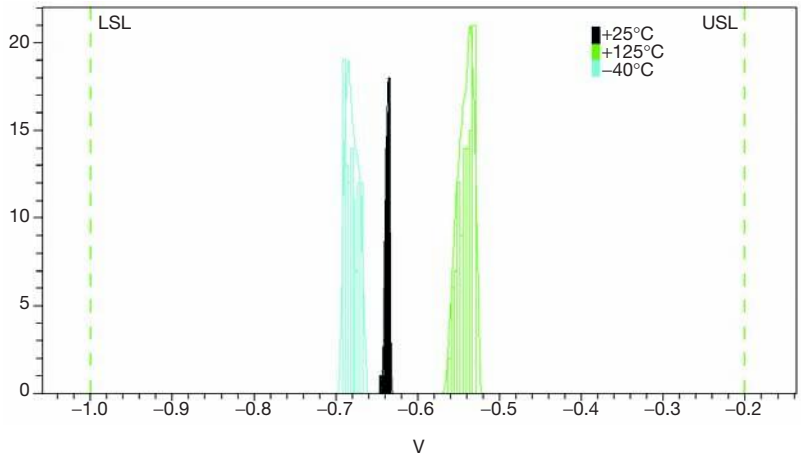

Figure 3 This silver-sample report shows the drift between temperatures. The data clearly shows an increase and decrease of the value at high and low temperatures, respectively.

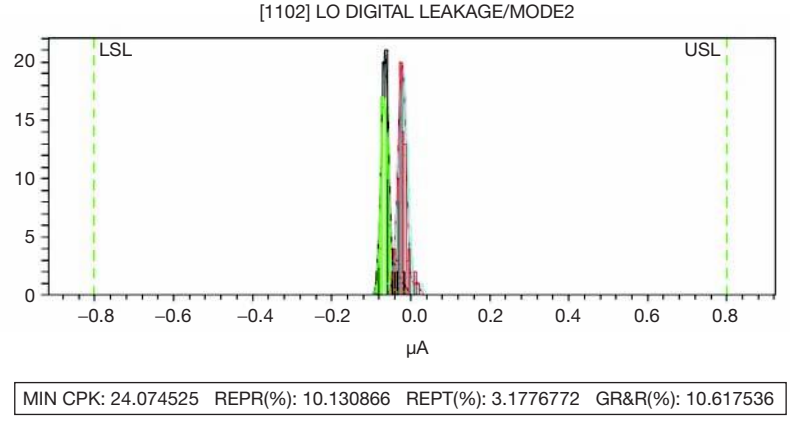

Figure 4 This tester-to-tester comparison shows a drift between the testers for which the root cause must be determined.

GR&R FOR PLASTIC PARTS

In addition to testing at the wafer level, engineers must test packaged parts to determine that no damage has occurred during the packaging process. To verify the repeatability and reproducibility on different testers, test a minimum of 50 plastic packaged parts on one tester twice in the same order, then repeat the procedure on another tester and compare the test results obtained using

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the different testers. An optimal result would be a 100% overlay of both sets of data. If you discover that the results are not closely matched, you must find the root cause for the discrepancy.

The tester-to-tester comparison in **Figure 4** shows a shift between two testers of the same type. The test results are not entirely consistent, and the results between testers need to be very close. The difference is usually traceable to something simple, such as the range of the instrument used. Though the two testers used for this example are the same type, the GR&R process can be used for tester transfers; that is, between two different tester types.

GR&R FOR WAFER SORT

An alternative to testing GR&R is to implement a bin-flip wafer technique (**Figure 5**). Rather than test plastic parts, the technique tests a complete wafer on tester 1 and then on tester 2. The bin results—that is, bin 1 to bin 7—should not exceed a predefined limit. If the measurement result is not repeatable on the other tester, review the failing tests to determine the problem.

BOARD VERSUS BOARD

To ensure multiple test boards have the same electrical characteristics, a measurement-system-analysis (MSA) report must be generated. The goal of this report is to verify that two or more load boards show the same electrical behavior. The example test flow described below assumes that two load boards are required to be released at the same time.

Fifty parts are tested in order, twice on one board and then twice on the other board. It is important to test the devices in the same order so that the same device test results are compared. In **Figure 6**, an offset between the boards can be seen. **Figure 6a** shows a histogram of the measurement results; **Figure 6b** shows the measurements in sequence. You can see that 50 parts were tested four times on two boards; the two distributions represent the boards. In this example, the trend line has a small offset to the left,

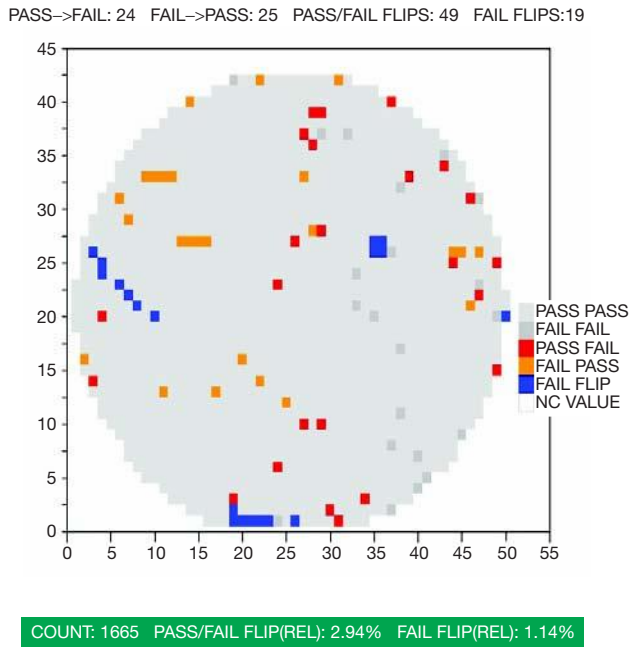

Figure 5 A report for a bin-flip wafer test compares results from two testers. Several designations and a color code on the wafer map indicate pass/fail results: Pass Pass (the site passed on tester 1 and tester 2); Fail Fail (the site failed on both testers); Pass Fail Flip (the site failed on tester 2); Fail Pass Flip (the site failed on tester 1); and Fail Flip (the site failed another test on tester 2).

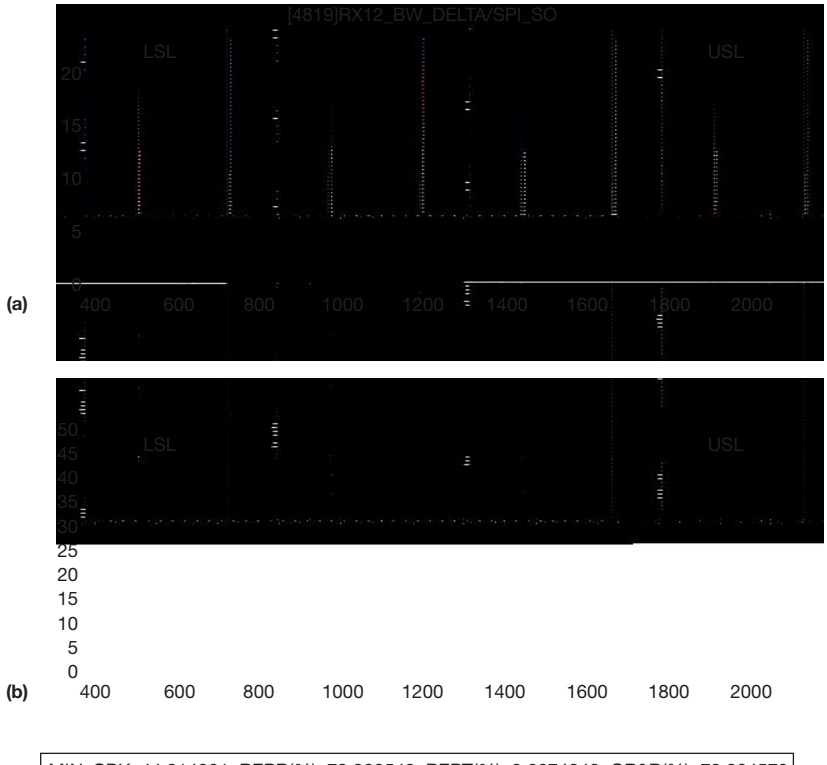

Figure 6 Board-to-board comparison data indicates a difference between devices 1 to 39 and 40 to 50. Shown are a histogram of the measurement results (a) and measurements in sequence (b).

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which indicates a difference between devices 1 to 39 and devices 40 to 50.

BOARD ID

Board identification ensures that the board being tested is the correct load board. Implement a board ID by writing a unique ID to the EEPROM on the load board. An error will then be indicated if the wrong board is selected for the production interface. Since each board has a unique ID, every test performed with it can be traced. In a worst-case situation, production lots can be recalled if tested with a defective board. To improve the measurement correlation between ATE and bench testing, offset calibration factors can be used and loaded automatically, depending on the board used.

QUALITY SCREENING

After all the required data is collected, a quality-assurance (QA) screening procedure can commence. One thousand good parts (minimum) have to be tested with the guard-banded limits. At completion of testing, all parts have to be tested at the QA temperatures with the specification limits. No failures are allowed at this point. If failures appear, it's necessary to reverify the guard bands and test-program stability.

Verifying that all the data results match and that no irregularities were found during the release phase of a test program minimizes the possibility of problems at a later stage. A stable and verified test solution can also help you avert product-yield problems and QA failures down the road. EDN

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AUTHOR'S BIOGRAPHY

Robert Seitz is a test development engineer in the Full Service Foundry business unit at AMS (formerly austriamicrosystems). He has worked in various areas of automated test engineering for seven years at the company.

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SPREAD SPECTRUM
SAFE HAVEN FOR
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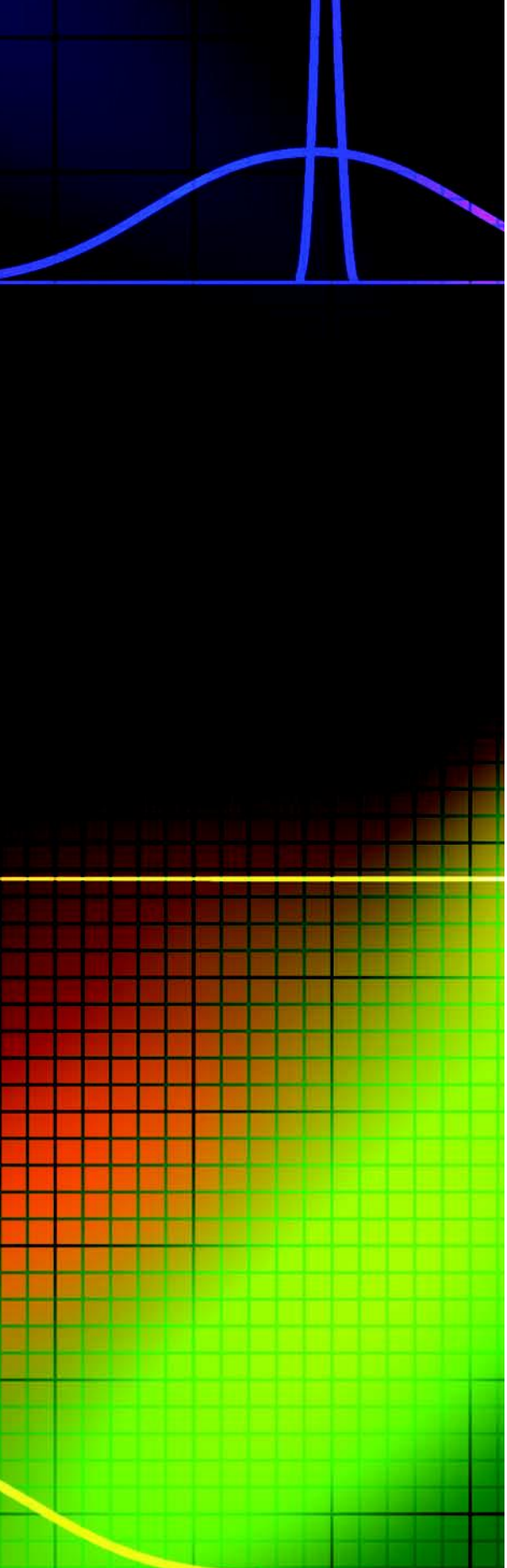

IMAGE: GIULIA FINI

SPECTRUM SPREADING APPEARS TO "WASTE" BANDWIDTH, BUT IT INCREASES CHANNEL CAPACITY, GUARDS DATA SECURITY, AND OFFERS IMMUNITY TO SIGNAL JAMMING AND FADING.

BY RAHUL GARG AND PRAKHAR GOYAL • CYPRESS SEMICONDUCTOR CORP

Wireless communications began to blossom in 1915, with the first wireless voice transmission across the continental United States, and quickly took off from there, with the first commercial radio broadcast in 1920, the first use of police-car dispatch radios in 1921, and the first phone call placed around the world in 1935. Commercial adoption of wireless technology spurred a global radio boom, but the early lack of restrictions on frequency-band usage resulted in noisy channels and unmanageable radio traffic.

The negative impact on communications quality led to the licensing of bands to regulate traffic. Even with legislation, however, further technological enhancements were required to suppress interference.

Moreover, licensing could not be implemented for every band, because reuse of a frequency band is also important for short-range applications. When a channel is used for communication inside a building, for example, its use in a physically distinct location should not be prohibited; such a restriction would result in spectrum underutilization, because such systems will never interfere with one another. Because any number of users could use a license-free band, however, enhancements mitigating interference were even more critical.

Spread-spectrum techniques have been among those enhancements. The concept emerged in the early 1940s and found popularity in the 1980s as the military embraced its use for data security and intrinsic immunity to signal jamming.

Spread spectrum is a means of transmission in which the signal occupies a bandwidth in excess of the minimum bandwidth necessary to send information. Using spread-spectrum techniques, information contained in a narrow band of frequencies (f_m) is translated, or spread, to a wider band (f_s) before transmission (**Figure 1**). This translation does not significantly increase the total power required, because the duration of the transmission remains the same; only the frequency changes.

The methods used to achieve spectrum spreading are frequency-hopping spread spectrum (FHSS) and direct-sequence spread spectrum (DSSS). Many wireless communication protocols, such as Bluetooth, use spread-spectrum techniques at the physical-layer level.

AT A GLANCE

- Frequency-hopping spread spectrum involves changing the transmission frequency from one subchannel to another. It offers immunity to near-far problems.
- Direct-sequence spread spectrum multiplies each bit of a message signal with a sequence of bits before transmission. The resultant signal is spread over a wider frequency range.
- PN codes in DSSS and the hopping sequence in FHSS both guard against eavesdropping, though a sequence must meet more stringent requirements to qualify as a DSSS PN code.
- The choice of PN codes is critical for the performance of a DSSS system and must exhibit high processing gain, minimal autocorrelation, and minimal cross-correlation.
- Every asynchronous digital communication requires the receiver to synchronize itself with the transmitter. Spread-spectrum systems must synchronize the PN code for DSSS and the frequency-hopping pattern for FHSS.

WHY SPREAD SPECTRUM?

Though spectrum spreading might appear to "waste" bandwidth, it actually increases the capacity of the channel. The Shannon-Hartley theorem (**Equation 1**) shows the relationship between channel capacity and channel bandwidth:

$$C=B\times LOG_2\left(1+\frac{S}{N}\right). \quad (1)$$

In the **equation**, C is the channel capacity, or the maximum number of users that can access the channel simultaneously; B is the channel bandwidth; and S/N is the signal-to-noise ratio.

It is reasonable to assume that the channel-capacity-to-bandwidth ratio in **Equation 1** is directly proportional to the required signal-to-noise ratio of the system (**Equation 2**):

$$\frac{C}{B}\alpha\frac{S}{N}. \quad (2)$$

The relationship, however, is not linear.

For a system with a fixed signal-to-noise-ratio requirement, the only way to increase channel capacity is to increase channel bandwidth. Hence, increasing the number of potential users compensates for the waste of bandwidth. Other advantages of spreading a signal over a larger band include the following:

- **Anti-jamming.** A jammer is a wireless transmitter that continuously transmits to a particular channel with high power. Other collocated devices receive this power as increased noise levels, which prevent them from accessing that channel. If communication occurs in the channel, the entire message signal will be lost. With spread spectrum, only a small part of the signal is blocked.
- **Immunity to fading.** In wireless systems, it is least likely that the transmitted signal will traverse the same path every time. It may face multiple reflections (or refractions) before actually reaching the receiver.

Those reflections create multiple wave fronts that interfere with one another constructively or destructively. The interference causes distortions or signal-strength reduction (fading) in the received signal. If the fading is significant enough to lower the received-signal-strength (RSS) levels below the minimum required threshold, the receiver cannot successfully decode the signal.

Because fading depends on the physical surroundings of the system, it is modeled as a random phenomenon. Fading, however, has been observed to have dominant effects only for particular frequencies. Hence, spread spectrum offers a measure of immunity because fading will have an effect only on small portions of the signal.

HOW FHSS WORKS

The frequency-hopping spread-spectrum approach changes the transmission frequency from one subchannel to another at regular intervals (**Figure 2**). A time-averaged view of FHSS requires a much higher bandwidth, even though the instantaneous bandwidth is the same as that of the original message signal.

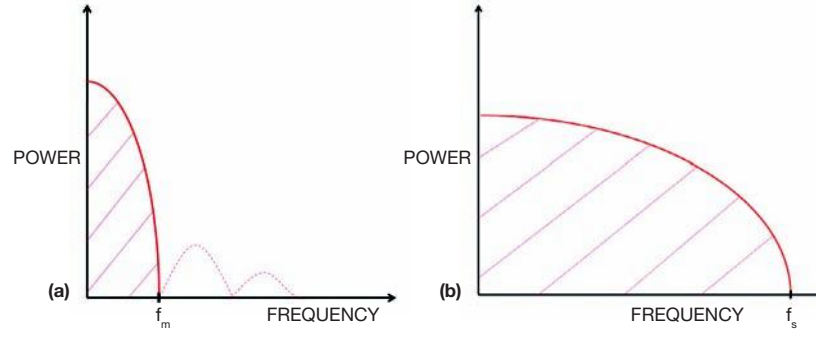

Figure 1 Using spread-spectrum techniques, information contained in a narrow band of frequencies (f_m) (a) is translated, or spread, to a wider band (f_s) before transmission (b).

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Hopping among subchannels occurs in a predetermined sequence; thus, each receiver must know the hopping sequence used by the corresponding transmitter in order to remain synchronized. The sequence safeguards against eavesdropping because a receiver cannot successfully decode the message signal without knowing the hopping sequence.

FHSS offers immunity to "near-far problems," or the interference that results when active transmitters are located in proximity to the target receiver. In the absence of FHSS, closely placed foreign transmitters generate a high power level that appears as very high-level noise to a receiver and can blind the receiver if it is communicating in that channel, blocking the communication. With FHSS, the reception bandwidth is bigger; thus, in a worst-case scenario, only some of the hops are blocked, forcing the system to work in less-than-optimum conditions.

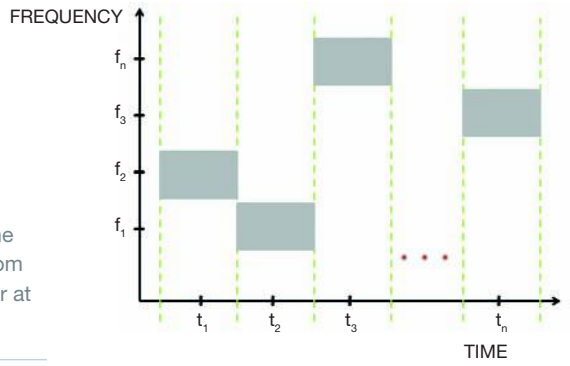

Figure 2 FHSS changes the transmission frequency from one subchannel to another at regular intervals.

HOW DSSS WORKS

Direct-sequence spread spectrum multiplies each bit of a message signal with a sequence of bits before transmission. The resultant signal is spread over a wider frequency range because the chip sequence, also called the pseudo-noise (PN) code, contains multiple-frequency components. The multiplication used here is a logical XOR operation that splits each bit into k number of chips, where k is the length of the PN code (**Figure 3**).

Because the PN code adds a redundant bit pattern for each bit transmitted, spreading has a direct impact on the effective data rate of the system. For a physical signaling rate of R_P, the effective data rate, R_E, will be given as expressed in **Equation 3**:

$$R_E = R_P \div n. \quad (3)$$

An increase in the signal's resistance to interference compensates for the reduced data rate. If one or more bits in the pattern are damaged during transmission, the original data can be recovered by processing the redundant bits with a suitable error-correcting method.

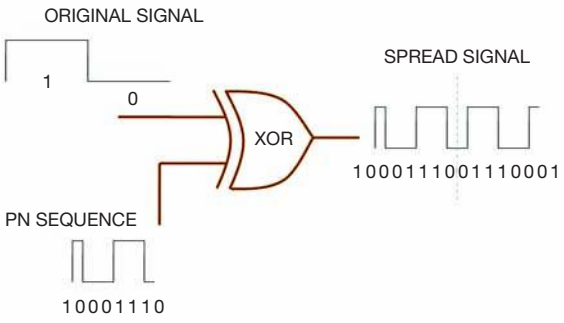

Figure 3 The multiplication used here is a logical XOR operation that splits each bit into k number of chips, where k is the length of the PN code.

Using PN codes, DSSS receivers "tune in" to the corresponding transmitter, tuning out other signals as noise. Because of this selective attention, the signal's resistance to interference increases, and the minimum required signal-to-noise ratio decreases.

Whereas FHSS concentrates the transmitted energy in one subband at a particular time, the energy distribution in DSSS is uniform. DSSS systems transmit over a group of frequencies simultaneously; hence, the range of operation is over wider bands. That uniformity makes the near-far problem more critical for DSSS.

PN codes in DSSS provide security against eavesdroppers, similar to the hopping sequence in FHSS, though in DSSS a sequence must meet more stringent requirements to qualify as a PN code.

DSSS-based systems use a PN-code sequence at the transmitter to spread the narrowband, information-bearing signal into a wideband signal. During transmission, various types of noise and interference affect bandwidth. For proper communication, the corresponding receiver must recover only the desired coded information, rejecting all other signals. Thus, every receiver uses a correlator—a special type of matched filter that responds only to signals encoded with a specific PN code (**Figure 4**). The DSSS receiver shown in the **figure** explains concepts related to PN codes.

ERROR CORRECTION

To understand the role of PN codes in error correction, consider a situation

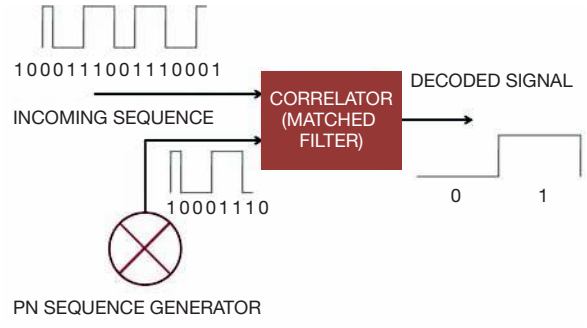

Figure 4 This DSSS receiver is a functional representation meant to explain concepts related to PN codes.

in which the incoming sequence and the PN code differ by just one chip. Because the degree of mismatch is low, the correlator output will not be at its peak, but neither will it be at its lowest value. Applying an appropriate threshold limit on the correlator output will allow a receiver to get a rough measure of the degree of mismatch. Based on that measurement, the receiver can make an intelligent decision about whether the incoming sequence corresponds to the desired PN code. PN codes thus provide error correction against corruption of chips.

PN-CODE CHARACTERISTICS

The choice of PN codes is critical for the performance of a DSSS system. PN codes must have certain desired characteristics, including high processing gain, minimal autocorrelation, and minimal cross-correlation.

High processing gain. Processing gain (G_p) is a theoretical system gain that reflects the relative advantage of frequency spreading in terms of channel capacity and immunity against interference. Expressed mathematically in **Equation 4**, it is the ratio of the chipping frequency (f_c) to the input-signal frequency (f_i):

$$G_P=\frac{f_c}{f_i}. \quad (4)$$

Thus, if a 10-kHz signal is spread over a band of 100 kHz, the corresponding processing gain is 10.

In general, PN codes should add a high processing gain to the system, for two reasons. The first is noise immunity: A higher processing gain implies that the input signal is spread over a larger band that requires the use of longer PN codes. Such systems are more tolerant to noise. The second reason is system capacity. The Shannon-Hartley theorem (**Equation 1**) holds that channel capacity is directly proportional to the channel bandwidth. Systems with higher processing gain have higher capacity because such systems need a higher bandwidth for transmission.

Minimal autocorrelation. Autocorrelation is the degree of similarity of a signal to its time-shifted version. **Equation 5** represents this concept mathematically:

$$R_{AUTO}(\tau)=\sum_{n=0}^{N-1}PN(n)\times PN(n+\tau), \quad (5)$$

where PN(n) is the pseudo-noise sequence, R_{AUTO} is the autocorrelation of the sequence PN(n), n is the length of the PN code, and τ is the delay factor by which PN(n) is shifted.

Time shifting of the signal is not linear; autocorrelation is calculated by shifting it circularly. The autocorrelation is a function of the delay (τ).

For correct decoding, the incoming signal should be phase synchronized with the PN code. The receiver maintains synchronization based on correlator output. Autocorrelation should have a large peaked maximum (**Figure 5**) for perfect synchronization; that is, τ=0, N, 2N, and so on. Otherwise, there is a high probability that the receiver will be inappropriately phase locked to the incoming sequence. Autocorrelation should be minimal for the slightest mismatch of the two waveforms.

Minimal autocorrelation also provides enhanced immunity against multipath interference. Once the receiver is phase locked to the incoming signal, it will not actively respond to time-shifted versions of the incoming sequence.

Minimal cross-correlation. Cross-correlation is similar to autocorrelation but measures the degree of similarity between two independent signals, as is expressed mathematically in **Equation 6**:

$$R_{CROSS}(\tau)=\sum_{n=0}^{N-1}PN_i(n)\times PN_j(n+\tau), \quad (6)$$

where $PN_i(n)$ is a pseudo-noise sequence; $PN_j(n)$ is another pseudo-noise sequence, completely independent of $PN_i(n)$; R_{CROSS} is the cross-correlation of the sequences $PN_i(n)$ and $PN_j(n)$; n is the length of the PN code; and τ is the delay factor.

Cross-correlation is also called the sliding-dot product. If the cross-correlation between two PN sequences is high, the receiver will not distinguish between the signals encoded over them, because the correlator might have sufficiently high output for both the signals.

THE INCOMING SIGNAL SHOULD BE PHASE SYNCHRONIZED WITH THE PN CODE. THE RECEIVER MAINTAINS SYNCHRONIZATION BASED ON CORRELATOR OUTPUT.

Here, the receiver might lose "selective attention" capability, resulting in the dominance of interference effects. To minimize the interference from other DSSS sources, different PN codes ideally should be orthogonal; that is, they should exhibit zero cross-correlation.

Because no PN codes are truly orthogonal, choosing the lowest possible cross-correlation mitigates effects.

SELECTING A PN CODE

In general, it is better to have PN codes that provide a high processing gain, but

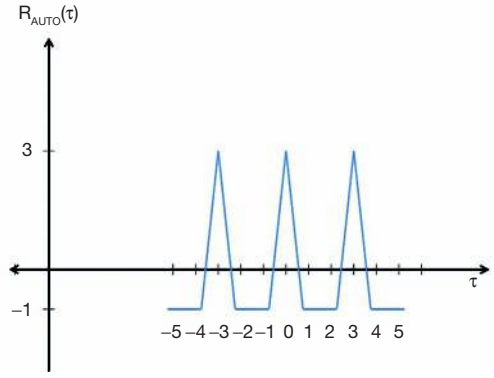

Figure 5 Autocorrelation should have a large peaked maximum for perfect synchronization only; otherwise, there is a high probability that the receiver will be inappropriately phase locked to the incoming sequence.

a higher gain requires a larger bandwidth. Another drawback of higher gain is that it typically needs long PN codes, which directly affect the effective data rate of the system. It is also relatively difficult to qualify a long sequence as a PN code because of the higher processing overhead associated with evaluating these characteristics. Due to these factors, selecting an appropriate PN code is a tedious task.

To simplify the process, some standard codes—Gold codes, m-sequences, and Walsh codes, for example—are chosen as a candidate for PN codes. These codes are known to have desirable characteristics; for example, m-sequences have low autocorrelation, while Gold codes exhibit low cross-correlation properties.

A typical approach for selecting PN codes is to choose some sequences from these standard codes and rate them separately on all of the desired characteristics (usually autocorrelation and cross-correlation only). These sequences can be ranked, based on the assigned ratings and application requirements. The ranks can then be used for deciding whether the corresponding sequence is fit to be a PN code.

Once an appropriate spreading method and spreading sequence are chosen, the next critical step is to establish synchronization between a transmitter and the corresponding receiver. Every asynchronous digital communication requires the receiver to employ a mechanism to synchronize itself with the transmitter; otherwise, it would be impossible for the receiver to decode the incoming signal. Because they are asynchronous in nature, spread-spectrum systems must synchronize the PN code for DSSS and the frequency-hopping pattern for FHSS.

Synchronization is established in two phases: acquisition and tracking. In the acquisition phase, the receiver

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detects whether the incoming signal is from the desired source. In the tracking phase, the receiver performs fine synchronization and tracks the incoming signal in terms of phase, frequency, or both, using a locking mechanism.

SYNCHRONIZATION IN DSSS

With DSSS, if the correlator output is less than a minimum threshold, it will discard the incoming sequence as background noise. Because the autocorrelation of a PN code is minimal, the correlator output is very low—ideally, zero—if the incoming sequence and the locally generated PN code are not phase synchronized. Without explicit measures for synchronization, the receiver could not decode the incoming signal reliably.

Because the PN code achieves signal spreading in DSSS, the carrier frequency of the transmitter remains the same, and there is no need for frequency synchronization between the transmitter and the receiver.

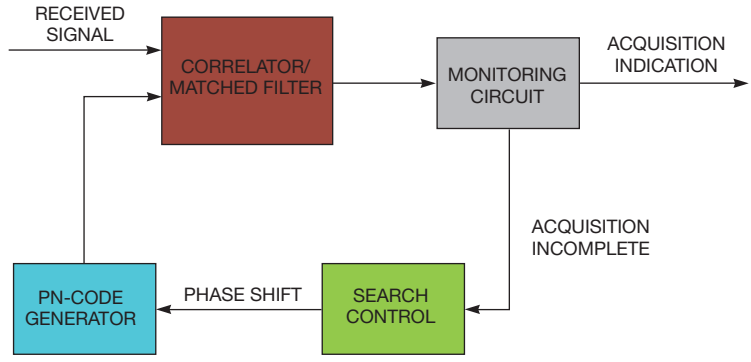

Figure 6 In serial search, a monitoring circuit keeps check on the correlator output. If the output fails to reach a threshold value, the search-control block shifts the phase of the generated PN code.

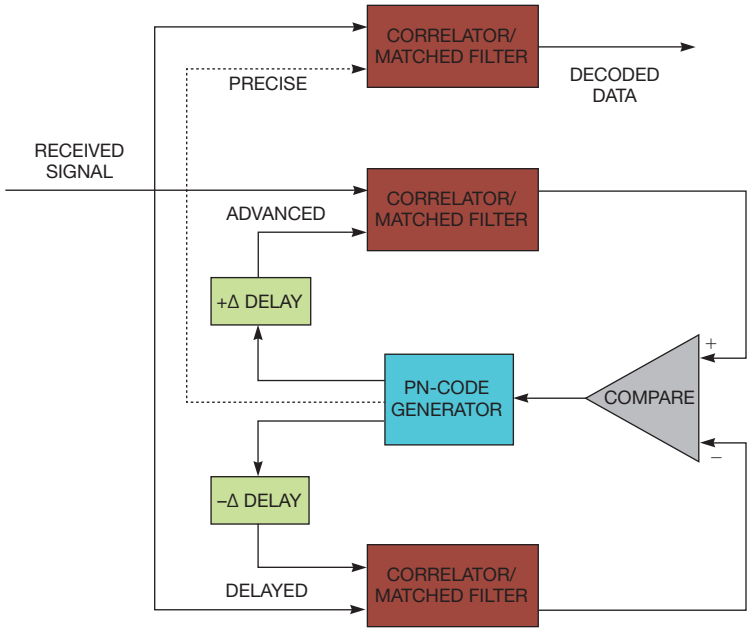

Figure 7 Given that dynamic adjustment is a continuous process, the precisely phased PN code remains precise throughout the reception process. It is this precise version of the PN code that is used for the actual dispreading of the received signal.

ACQUISITION IN DSSS

Correlation between the incoming sequence and the locally generated one has a peaked maximum for perfect synchronization. Using "serial" or "parallel" search, the receiver searches for a phase in which the correlation exceeds a predefined threshold.

In serial search, a monitoring circuit keeps check on correlator output. If the output fails to reach a threshold value, then the search-control block shifts the phase of the generated PN code (**Figure 6**). This process repeats until the correlator output reaches the threshold value, completing acquisition. The configuration forms a feedback loop, referred to as a sliding correlator.

One potential drawback to serial search is that acquisition times are high. Hence, some designs use a parallel approach.

A parallel-search strategy is essentially the same as serial search, but it shortens the acquisition time because it carries out multiple phase comparisons simultaneously, albeit at a trade-off of increased hardware-resource requirements and complexity. The acquisition time is the lowest with a parallel strategy when the number of correlators equals the number of chips in the PN code.

The acquisition process achieves only a coarse synchronization. The degree of synchronization achieved at the end of this phase is within $\pm T_C/2$, where T_C is the chip duration.

TRACKING IN DSSS

Once acquisition is complete, the receiver starts tracking the phase of the incoming sequence to achieve finer synchronization. A delay-locked loop (DLL) is commonly used (**Figure 7**). The DLL generates three phases, or versions, of the PN code—the delayed, advanced, and precise phases—and continuously compares the output of the correlator using the delayed PN code and the output using the advanced PN code. This comparison provides a

measure of the direction of phase drift in the incoming signal; using this metric, the phase of the precise version of the PN code is dynamically adjusted.

The precisely phased PN code remains accurate throughout the reception process. It is this version of the PN code that is used for the actual dispreading of the received signal (**Figure 7**).

SYNCHRONIZATION IN FHSS

With FHSS, because the transmitter keeps changing the center frequency, the receiver and the corresponding transmitter should be in the same frequency channel. Another important requirement is that both transmitter and receiver should spend the same amount of time in a particular channel; otherwise, the receiver might hop to another channel prematurely and lose synchronization with the transmitter.

ACQUISITION IN FHSS

Acquisition in frequency-hopping systems refers to frequency synchronization; its purpose is to put the receiver and transmitter on the same frequency channel. The simplest approach is a dedicated acquisition channel wherein the transmitter and the receiver must initiate communication on the dedicated channel only and wait until acquisition is complete. If the dedicated channel is jammed because of noise, communication will not occur.

Another approach is to start hopping at power-on. The transmitter's hopping rate should be faster than that of the receiver to ensure that the devices end up on the same channel.

TRACKING IN FHSS

After acquisition, the receiver should be able to track the transmitter. Both the transmitter and the receiver should stay in a channel for the same duration and hop to the same new channel once that period is over. Timing synchronization is easier to implement in FHSS than in DSSS because the hopping rate is fixed for both devices. To determine the next channel, the devices have a preloaded lookup table containing available channel numbers.

SYSTEM PERFORMANCE

The synchronization process needs a certain amount of delay for both DSSS and FHSS. Hence, most protocols have an additional header for the sync pulses to ensure that the receiver and the transmitter are synchronized before packets with meaningful information are transmitted. EDN

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BY DENNIS FEUCHT • INNOVATIA LABORATORIES

Forgotten circuits (that should be brought back)

WHAT MAKES A LEGACY IC? HERE WE TAKE A LOOK AT SOME ORIGINAL PARTS AND DISCUSS WHY IT MIGHT BE A GOOD IDEA TO REVISIT THEIR USE.

As electronics technology matures, it shows some signs of aging. As innovation wanes, breakthroughs grow farther apart in time, and risk-taking decreases. In earlier decades, some IC companies were willing to put on the market a few unusual and conceptually original parts. Signetics, for example, dared in the early 1970s to produce a novel IC—Hans Camenzind's 555 timer—and it has become a premier legacy IC.

What about other circuits? This article recounts a few of these parts and why it might be good to bring them back.

AD639 SINE CONVERTER

Long ago, Barrie Gilbert did some investigative work on the two-bipolar-junction-transistor (BJT) differential-amplifier circuit, which has a hyperbolic tangent, tanh, transfer function:

$$i_o = i_{o+} - i_{o-} = I_0 \times \tanh\left(\frac{V_I}{2 \times V_T}\right),$$

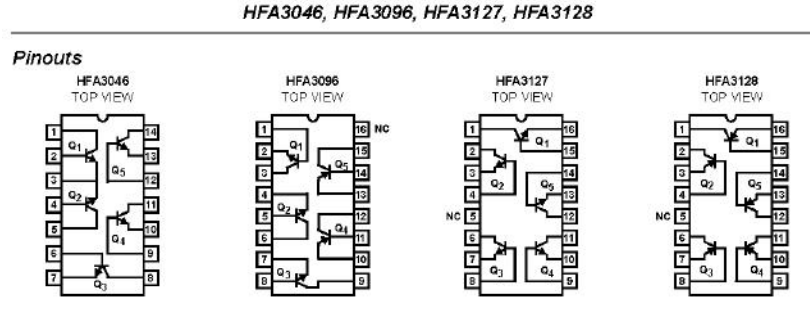
where I_0 is the emitter source current and the thermal voltage, V_T, is 26 mV. To reduce nonlinearity, external emitter resistance, R_E, is placed in series with the emitter in amplifiers. Gilbert, however, applied the engineering adage that "if you can't fix it, feature it" and put it to good use.

Hyperbolic tangents are vaguely related to trigonometric functions, and Alan Grebene at Exar used a single diff amp in the XR2206 function-generator (FG) IC to convert a triangle wave into a sine wave. The result was somewhat acceptable for a first-generation effort, though Gilbert carried out more refinement of the basic idea. He developed the multi-tanh concept of adding the outputs of diff amps that had inputs offset from each other by a fixed voltage. This approach extended the function (and input range) and also led to other novelties, including the one that is used in the AD639 sine converter.

This IC is a trigonometric wonderland in 16 pins, and because its functional capability is so powerful, it was destined to become a legacy IC. Alas, ADI pulled the AD639 from the market without a replacement. I do not know why. Even Gilbert did not know why. It seemed like a part destined to become a legend. It can synthesize all of the basic trigonometric functions (sin, cos, tan sec, csc, cot) and their inverses.

The sine function is accurate to 0.02%, better than most FG sine outputs and better than the total harmonic distortion (THD) of many audio amplifiers. The IC has two of them, plus offset circuitry, and a multiplier and divider. It was given niche-market pricing and thus did not find its way into FG instruments and others requiring accurate or low-THD sine-wave generation. It is specified to 1.5 MHz.

Perhaps the only problem was that because the AD639 was so appealing, ADI put a premium price tag on it, which defeated its spread into the market as a commodity part. Perhaps Rochester Electronics—the leading supplier on the "trailing edge"—could revive it and reap the small fortune that it was destined to produce. There is no reason to confine the mission of Rochester Electronics to that of a replacement-



HFA3046, HFA3096, HFA3127, HFA3128

Electrical Specifications $T_A = 25°C$ (Continued)

PARAMETER	TEST CONDITIONS	DIE			SOIC, QFN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL PAIR MATCHING CHARACTERISTICS FOR THE HFA3046								
Input Offset Voltage	I_C = 10mA, V_{CE} = 5V	-	1.5	5.0	-	1.5	5.0	mV
Input Offset Current	I_C = 10mA, V_{CE} = 5V	-	5	25	-	5	25	µA
Input Offset Voltage TC	I_C = 10mA, V_{CE} = 5V	-	0.5	-	-	0.5	-	µV/°C

Figure 1 Replacements for the CA3000 series in the form of HFA3000-series SOIC parts offer multiple-gigahertz f_Ts but correspondingly lower breakdown voltages. The table shown is excerpted from Intersil parts data.

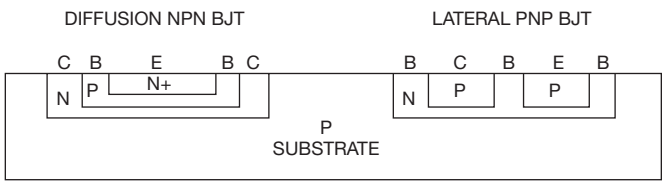


Figure 2 The CA3096's PNP BJTs are constructed as lateral transistors.

parts supplier for obsolete equipment when it could also be considered the fulfiller of the destiny of great parts for new designs that did not catch on the first time around.

CA3096 BJT ARRAY

Somewhat like the AD639 sine converters are the highly versatile building blocks that are transistor arrays. RCA came out with some BJT arrays comprising a CA3000-series line. Some of these parts had f_Ts of over 1 GHz for NPN BJTs, which make them good for new designs today.

When RCA was shuffled around, it eventually ended up with Intersil but had lost the fab facility with its old large-geometry process. Tektronix based the design of the vertical amplifier in its 2205 oscilloscope on CA3046 (or the equivalent National LM3046) parts, which are attractive for implementing fast two- or four-quadrant multipliers.

Intersil inherited a large but finite supply of these parts that is still available but dwindling. They ought to be brought back on an existing process. It is not a major development project, and such parts would be extremely useful. Intersil did create a replacement in the form of HFA3000-series SOIC parts with multiple-gigahertz f_Ts but with correspondingly lower breakdown voltages (**Figure 1**).

While the original CA3000 series was good for ±12V supplies, the HFA series is better designed with ±5V supplies, though the ICs can handle up to about 10V. What is much improved in the HFA series are the PNP BJTs, which are dielectrically isolated rather than made as lateral transistors, as in the CA3096 (**Figure 2**).

The CA3096 is a versatile part, with three NPN and two PNP BJTs. The one drawback is that the lateral PNPs have an f_T of only about 6 MHz. (Making the base thin is difficult for lateral BJTs.) For numerous circuits, however, this specification is not a major impediment.

In one example, a feedback amplifier has a quasistatic gain of 3 and a bandwidth of over 50 MHz (**Figure 3**). It has two forward paths, the slow path through the PNP current mirror and the fast path through Q_2 of the diff-amp input stage. It uses all five array BJTs. The only other semiconductor part is the avalanche diode, Z_1.

You would not be inclined to design this circuit into a new product because of an uncertain component supply. In addition, the HFA part does not have the voltage range. A series comparable to the CA3000 but with dielectrically iso-

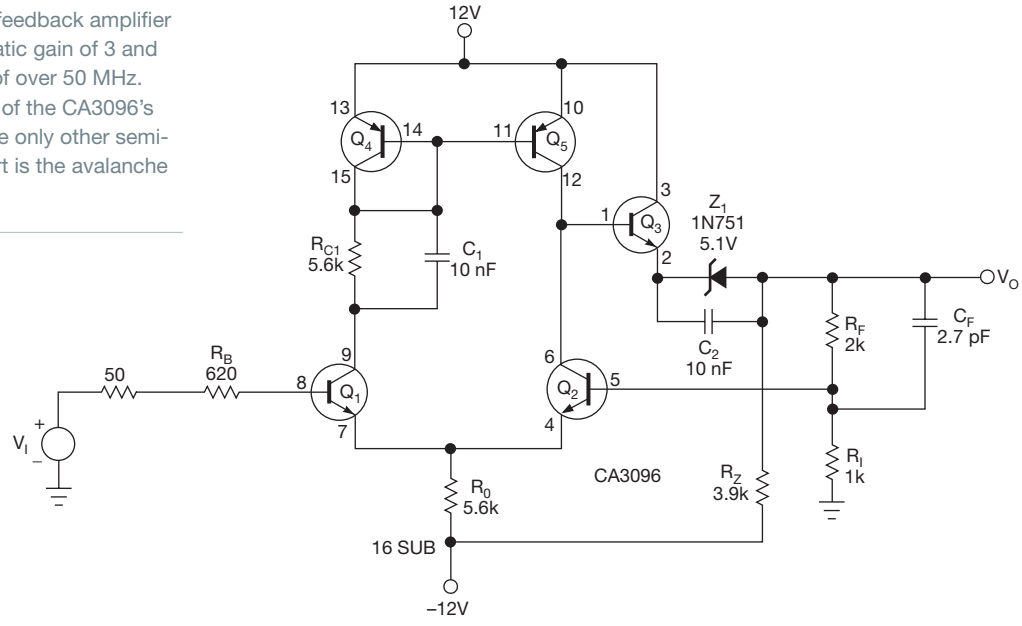


Figure 3 This feedback amplifier has a quasistatic gain of 3 and a bandwidth of over 50 MHz. It uses all five of the CA3096's array BJTs; the only other semiconductor part is the avalanche diode, Z_1.

lated PNPs would be a welcomed addition to the neo-legacy category of ICs.

MC14500B INDUSTRIAL-CONTROL UNIT

The 16-pin MC14500B from Motorola is a single-bit, 1-MHz CMOS processor. It has three single-bit registers (flops) and an arithmetic logic unit and executes 16 instructions. Newer microcontrollers blow this part away, but that is not the point. It is a chunk of versatile logic that needs only an external counter for a program counter (PC) and a program memory driven by the PC.

The data memory is also the I/O memory. Four bits of the memory output drive the op-code input on the MC14500B; the rest are I/O addressing of 8-bit bidirectional latches (MC14599B) and 8-input multiplexers or data selectors (MC14512).

The one-bit accumulator is called the result register (RR). Instructions include Load RR, Load the complement of RR, AND data with RR, Complement data and AND, OR, Complement data and OR, exclusive NOR (equivalence), store and store complement pulse the write line with valid RR output, move input data to input register or to output register, skip next instruction if RR=0, and pulse flag O out or flag F out. Two other instructions, JMP and RTN, also output flag pulses. The JMP flag can be used to load an address into the PC. The RTN instruction outputs an RTN flag and skips the next instruction.

The built-in oscillator generates the clock that drives the PC. The rising edge of the clock increments the PC, and while high, the instruction is fetched. During the low phase of the clock, the instruction is decoded and executed.

Because it uses bit-serial processing and is I/O intensive, what advantage does this part have nowadays? With the requirement of an additional counter, and program and data memory, this part will remain obsolete because it cannot compete with lower-cost 8- to 16-pin flash-programmable ICs that are easy to use and are far more powerful. Although the part is interesting, it requires too much bit-twiddling to be welcomed back into production. This one will remain forgotten, despite its inspiration quotient.

MC14549 AND MC14559 SARs

These successive-approximation registers (SARs) were originally part of the Motorola 4000-series offering of CMOS (mostly) digital ICs. They have 8 bits per IC and can be cascaded for more bits. They are used to build successive-approximation ADCs. Internally, they have a shift register and a parallel-loading register.

Despite the simplicity of an SAR, it is a useful digital function. The SA algorithm searches a range by making a succession of boolean comparisons beginning at midrange. If the voltage is greater, the most-significant bit is set and the next bit is tested until all bits have been determined. All conversions on n bits take n clock cycles, independent of the digitized value.

With an extra comparator and one or two SAR ICs driving an extra DAC, a simple ADC can be added to a system with leftover subparts. Although this level of integration is semi-discrete nowadays, for many applications with multi-DAC and multicomparator ICs—and with a need for a simple ADC—it can be a design possibility.

SARs also could be used for auto-ranging, with fewer average steps than sequential ranging. Similarly, the gain of a variable-gain amplifier (VGA) can be set by an SA search through the large range of the VGA. The weighting of the bits might no longer be binary, but instead be a decade or 1-2-5 sequence. If it's monotonic, however, the scheme works.

MC4530 DUAL FIVE-INPUT MAJORITY GATE

One of the stranger logic functions to make it into integrated form and onto the market was a dual five-input majority gate, sold by Motorola. If three or more of the five inputs are asserted, the output is asserted. Those of you who like to find novel uses for existing logic parts might have an intriguing time with this part. The output was gated with an XNOR (equivalence) gate from a W input,

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to set the polarity of the output.

What are its uses? This part is relevant to unusual applications, but it can coax some creative thinking. It generates a decision when five or fewer subsystems indicate a status in a redundant system. If, for example, the vital-sign monitors in a hospital's intensive-care unit show three or more of five patients are in trouble, a triage state is asserted.

WITH AN EXTRA COMPARATOR AND ONE OR TWO SAR ICs DRIVING AN EXTRA DAC, A SIMPLE ADC CAN BE ADDED TO A SYSTEM WITH LEFTOVER SUBPARTS.

By connecting one input high and one low, two out of three control computers (as in the space shuttle) prevail in a vote on an output assertion. Alternatively, if multiple banks of capacitors are asynchronously charged, sufficient charge is available and the firing device is enabled if m out of n banks indicate that they are charged. The function is egalitarian; any m out of n will trigger an event. Using inverted input logic, a statically stable, multi-ped robot with fewer than m of n feet on the ground triggers a fault state.

A voting hierarchy is implemented by cascading the output of one of the majority gates into one input of another. The first five then have one vote in the second five. Although such uses might be practical, it is still an unusual logic function to try to apply. No wonder it is a forgotten circuit. EDN

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Auto pulse generator senses and responds to a probed load

Raju Baddi, Tata Institute of Fundamental Research, Pune, India

This automatic pulse generator (**figures 1** and **2**) is a test gadget that senses a probed contact to a pair of terminals under test and automatically issues a momentary power pulse to them once proper contact is made. These terminals could be the input of a logic gate, an LED on a circuit board, a transformer or relay coil, etc. The need for such a pulse often arises in the day-to-day engineering work of experimenting and testing.

The gadget is powered with a small 3.6V rechargeable NiCd battery. You can easily construct it in a glue-stick tube (**Figure 3**) with the special arrangement of probes shown. A regular arrangement of independent probes also may be used. The circuit has been tested with a 5V supply, as well.

Two versions are shown: **Figure 1** uses an NE555 timer IC as a monostable and is the easiest to get working. **Figure 2** eliminates the NE555 for a reduced parts count but could be affected by variations in the parameters and different manufacturers of the CD4069 CMOS hex inverter used in place of the NE555.

Transistors Q_1 and Q_2 are switches that connect the +ve and –ve probes to the 3.6V supply and ground when turned on by the CD4069 and the NE555. R_3 and R_4 bias gate G_1's input just below the switching threshold to hold its output high, which holds the output of gate G_2 low. The time constant formed by C_1 provides a certain

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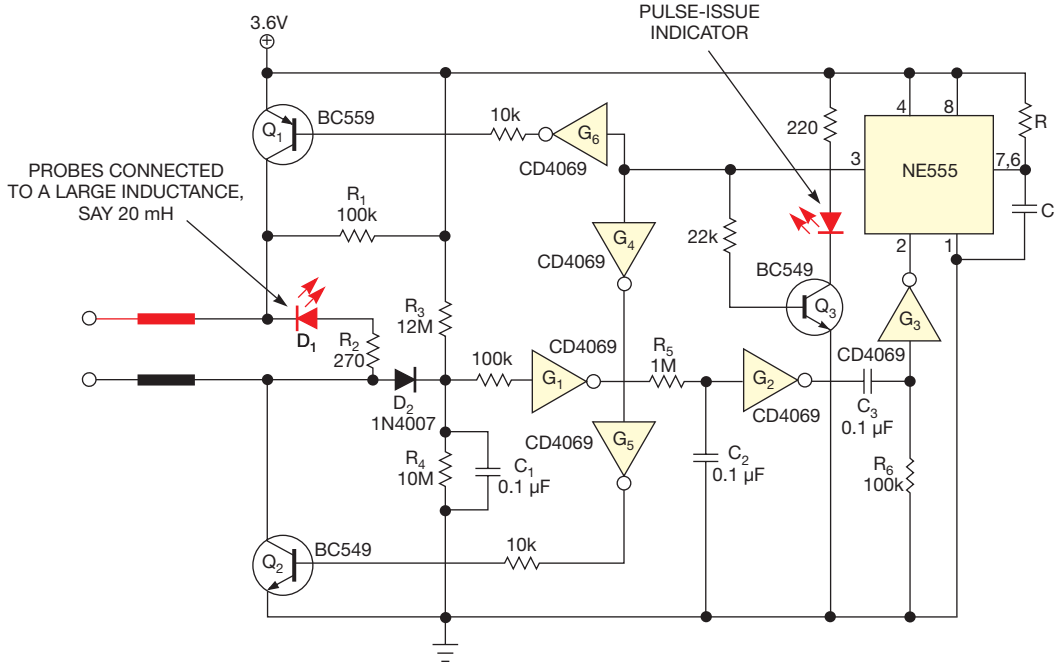


Figure 1 The NE555 version is easy to get working but has an increased parts count.

LINEAR TECHNOLOGY

DESIGN NOTES

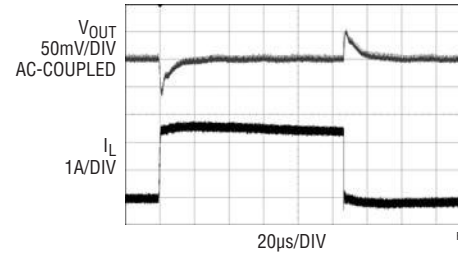
20V, 2.5A Monolithic Synchronous Buck SWITCHER+ with Input Current, Output Current and Temperature Sensing/ Limiting Capabilities

Design Note 511

Tom Gross

Introduction

The LTC®3626 synchronous buck regulator with current and temperature monitoring is the first of Linear's SWITCHER+™ line of monolithic regulators. It is a high efficiency, monolithic synchronous step-down switching regulator capable of delivering a maximum output current of 2.5A from an input voltage ranging from 3.6V to 20V (circuit shown in Figure 1). The LTC3626 employs a unique controlled on-time/constant-frequency, current-mode architecture, making it ideal for low duty cycle applications and high frequency operation, while yielding fast response to load transients (see Figure 2). It also features mode setting, tracking and synchronization capabilities. The LTC3626's 3mm × 4mm package has such low thermal impedance that it can operate without an external heat sink even while delivering maximum power to the load.



12V_{IN} TO 1.8V_{OUT} LOAD STEP RESPONSE,
2.5A LOAD STEP, 2MHz SWITCHING FREQUENCY,
FORCED CONTINUOUS MODE, INTERNAL COMPENSATION

Figure 2. Load Step Response for Figure 1 Circuit

Beyond its impressive regulator capabilities, the LTC3626's current and temperature monitoring functions stand out. They offer both monitoring and control capabilities with minimal additional components.

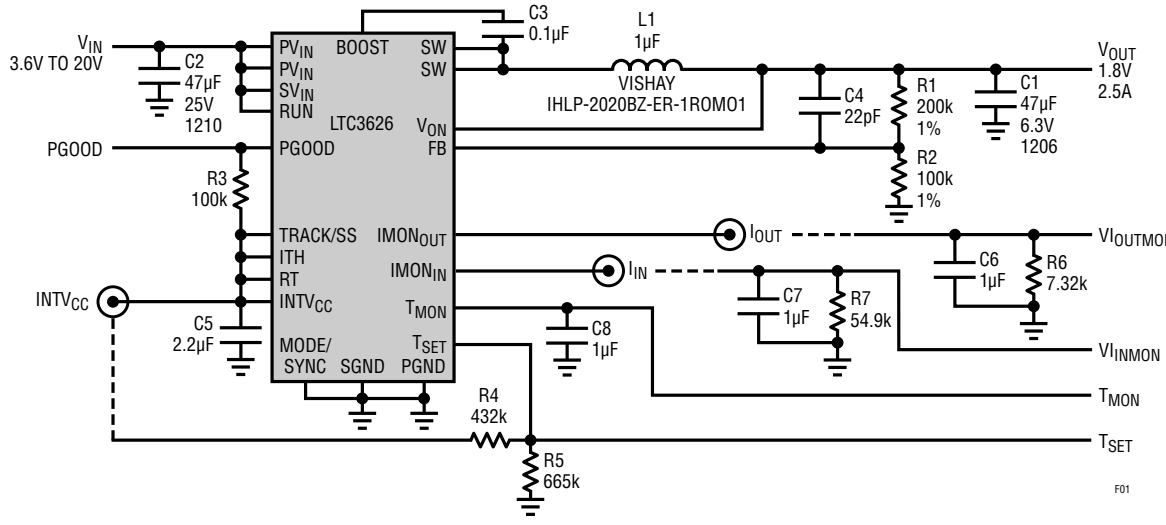


Figure 1. 20V Maximum Input, 2.5A, 2MHz Buck Regulator with Current and Temperature Monitoring

Output/Input Current Sensing

The LTC3626 senses the output current through the synchronous switch during the switch's on-time and generates a proportional current (scaled to 1/16000) at the $IMON_{OUT}$ pin. Figure 3 shows the accuracy of the $IMON_{OUT}$ output by comparing the measured output of the $IMON_{OUT}$ pin with calculated values. Error remains less than 1% over most of the output current range.

Likewise, this same sense current signal is combined with the buck regulator's duty cycle to produce a current proportional to the input current—again by 1/16000—at the $IMON_{IN}$ pin. A precision of better than 5% is achieved over a wide current range (see Figure 4).

Both current signals are connected to internal voltage amplifiers, referenced to 1.2V, that can shut down the part when tripped. So the input and output current limits are set by simply connecting a resistor to the $IMON_{IN}$ or $IMON_{OUT}$ pins, respectively, as shown in Figure 1. The relationship between the current limit and the resistor is:

$$I_{LIM} \simeq \frac{1.2V \bullet 16000}{R_{LIM}}$$

For example, a 10k resistor sets a current limit of approximately 2A.

This simple scheme allows both monitoring and active control of the input and output current limits—the latter can be implemented via external control circuitry, such as a DAC with a few passive components.

Temperature Sensing

The LTC3626 generates a voltage proportional to its own die temperature, which can be used to set a maximum temperature limit. The voltage at the temperature monitor pin (T_{MON}) is typically 1.5V at room temperature. To calculate the die temperature, T_J, multiply the T_{MON} voltage by the temperature monitor voltage-to-temperature conversion factor of 200°K/V, and subtract the 273°C offset. The LTC3626 also has a temperature limit comparator fed by the temperature limit set pin, T_{SET}, and the T_{MON} pin. Hence, by applying a voltage to the T_{SET} pin, a maximum temperature limit can be set according to the following:

$$V_{TSET} = \frac{T_J + 273}{200°K/V}$$

Choosing a maximum temperature limit of 125°C equates to an approximate 2V setting on the T_{SET} pin—the IC will shut down once the die temperature T_J reaches this limit.

Conclusion

The LTC3626 combines current and temperature monitoring capabilities with a high performance buck regulator in a compact package. A microprocessor or other external control logic can supervise conditions via easy-to-use input and output current and temperature monitor pins, and it can shut itself down by setting a threshold voltage on the temperature set limit pin.

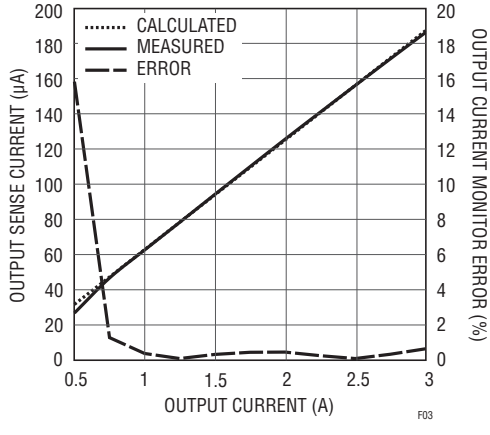


Figure 3. Output Current vs Output Current Monitor

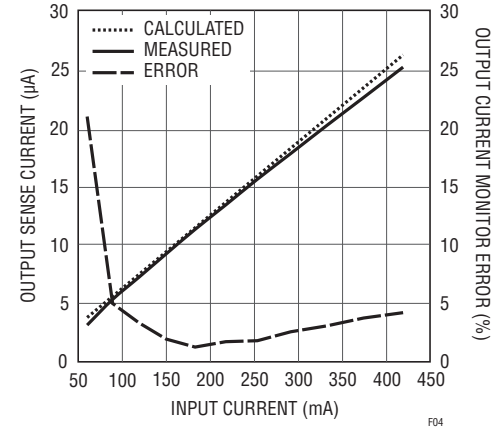


Figure 4. Input Current vs Input Current Monitor

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LINEAR TECHNOLOGY

DESIGN NOTES

Protect Sensitive Circuits from Overvoltage and Reverse Supply Connections

Design Note 497

Victor Fleury

Introduction

What would happen if someone connected 24V to your 12V circuits? If the power and ground lines were inadvertently reversed, would the circuits survive? Does your application reside in a harsh environment, where the input supply can ring very high or even below ground? Even if these events are unlikely, it only takes one to destroy a circuit board.

To block negative supply voltages, system designers traditionally place a power diode or P-channel MOSFET in series with the supply. However, diodes take up valuable board space and dissipate a significant amount of power at high load currents. The P-channel MOSFET dissipates less power than the series diode, but the MOSFET and the circuitry required to drive it increases costs. Both of these solutions sacrifice low supply operation, especially the series diode. Also, neither protects against voltages that are too high—protection that requires more circuitry, including a high voltage window comparator and charge pump.

Undervoltage, Overvoltage and Reverse-Supply Protection

The LTC®4365 is a unique solution that elegantly and robustly protects sensitive circuits from unpredictably high or negative supply voltages. The LTC4365 blocks positive voltages as high as 60V and negative voltages as low as –40V. Only voltages in the safe operating supply range are passed along to the load. The only external active component required is a dual N-channel MOSFET connected between the unpredictable supply and the sensitive load.

Figure 1 shows a complete application. A resistive divider sets the overvoltage (OV) and undervoltage (UV) trip points for connecting/disconnecting the load from V_{IN}. If the input supply wanders outside this voltage window, the LTC4365 quickly disconnects the load from the supply.

The dual N-channel MOSFET blocks both positive and negative voltages at V_{IN}. The LTC4365 provides 8.4V of enhancement to the gate of the external MOSFET

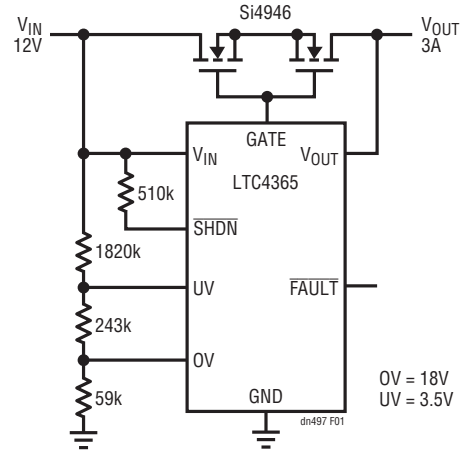

Figure 1. Complete 12V Automotive Undervoltage, Overvoltage and Reverse-Supply Protection Circuit

during normal operation. The valid operating range of the LTC4365 is as low as 2.5V and as high as 34V—the OV to UV window can be anywhere in this range. No protective clamps at V_{IN} are needed for most applications, further simplifying board design.

Accurate and Fast Overvoltage and Undervoltage Protection

Two accurate (±1.5%) comparators in the LTC4365 monitor for overvoltage (OV) and undervoltage (UV) conditions at V_{IN}. If the input supply rises above the OV or below the UV thresholds, respectively, the gate of the external MOSFET is quickly turned off. The external resistive divider allows a user to select an input supply range that is compatible with the load at V_{OUT}. Furthermore, the UV and OV inputs have very low leakage currents (typically < 1nA at 100°C), allowing for large values in the external resistive divider.

Figure 2 shows how the circuit of Figure 1 reacts as V_{IN} slowly ramps from –30V to 30V. The UV and OV thresholds are set to 3.5V and 18V, respectively. V_{OUT} tracks V_{IN} when the supply is inside the 3.5V to 18V window. Outside of this window, the LTC4365 turns off the N-channel MOSFET, disconnecting V_{OUT} from V_{IN}, even when V_{IN} is negative.

Novel Reverse Supply Protection

The LTC4365 employs a novel negative supply protection circuit. When the LTC4365 senses a negative voltage at V_{IN}, it quickly connects the GATE pin to V_{IN}. There is no diode drop between the GATE and V_{IN} voltages. With the gate of the external N-channel MOSFET at the most negative potential (V_{IN}), there is minimal leakage from V_{OUT} to the negative voltage at V_{IN}.

Figure 3 shows what happens when V_{IN} is hot-plugged to –20V. V_{IN}, V_{OUT} and GATE start out at ground just before the connection is made. Due to the parasitic inductance of the V_{IN} and GATE connections, the voltage at V_{IN} and GATE pins ring significantly below –20V. The external MOSFET must have a breakdown voltage that survives this overshoot.

The speed of the LTC4365 reverse protection circuits is evident by how closely the GATE pin follows V_{IN} during the negative transients. The two waveforms are almost indistinguishable on the scale shown. Note that no additional external circuits are needed to provide reverse protection.

There's More! AC Blocking, Reverse V_{IN} Hot Swap™ Control When V_{OUT} is Powered

After either an OV or UV fault has occurred (or when V_{IN} goes negative), the input supply must return to the valid operating voltage window for at least 36ms in order to turn the external MOSFET back on. This effectively blocks 50Hz and 60Hz unrectified AC.

LTC4365 also protects against negative V_{IN} connections even when V_{OUT} is driven by a separate supply. As long as the breakdown voltage of the external MOSFET is not exceeded (60V), the 20V supply at V_{OUT} is not affected by the reverse polarity connection at V_{IN}.

Conclusion

The LTC4365 controller protects sensitive circuits from overvoltage, undervoltage and reverse-supply connections using back-to-back MOSFETs and no diodes. The supply voltage is passed to the output only if it is qualified by the user-adjustable UV and OV trip thresholds. Any voltage outside this window is blocked, up to 60V and down to –40V.

The LTC4365's novel architecture results in a rugged, small solution size with minimal external components, and it is available in tiny 8-pin 3mm × 2mm DFN and TSOT-23 packages. The LTC4365 has a wide 2.5V to 34V operating range and consumes only 10µA during shutdown.

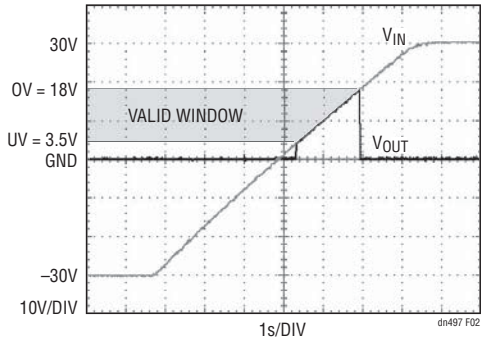

Figure 2. Load Protection as V_{IN} Is Swept from –30V to 30V

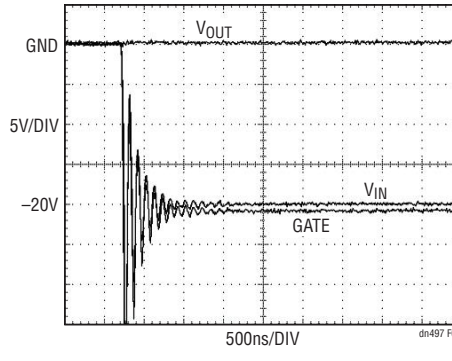

Figure 3. Hot Swap Protection from V_{IN} to –20V

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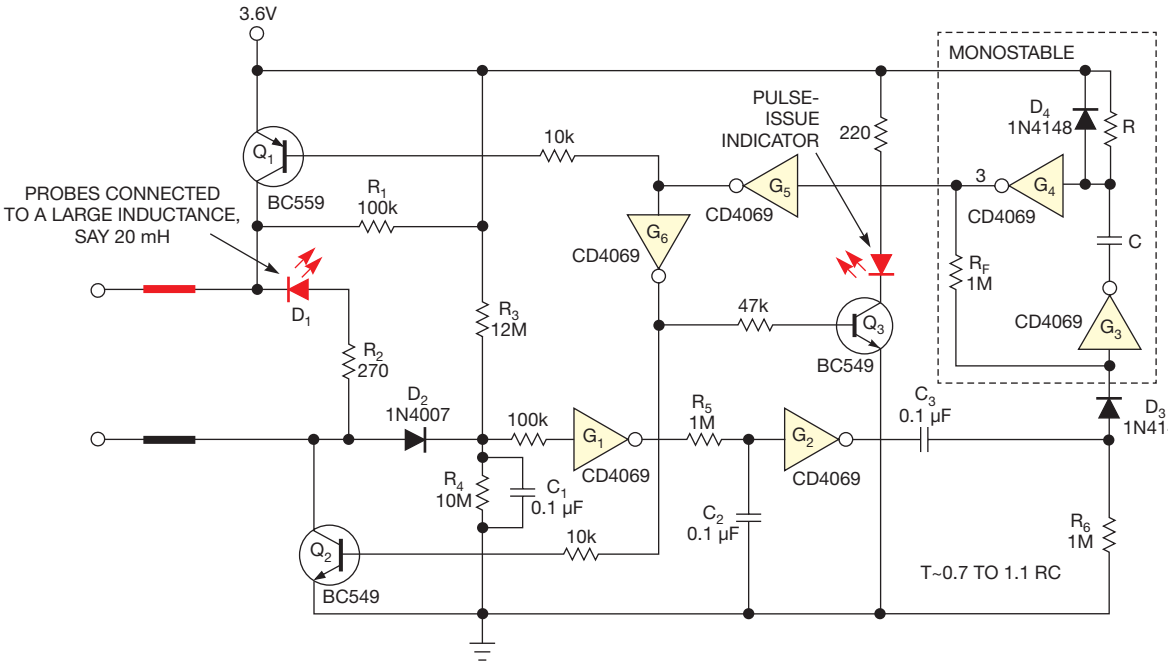

Figure 2 You can eliminate the NE555, but variations in the G_4 input switching threshold can affect the pulse duration.

amount of noise immunity and determines the minimum time for which the test circuit should be connected between the probes. The 100-kΩ resistor in series with the input of G_1 limits the input current in case the probe is accidentally connected to an active circuit.

R_1 connects to the junction of R_3 and R_4 through a reverse-biased diode, D_1. It normally has no effect as long as the probes are not connected through a load, because the series string of R_1, D_1, R_2, and D_2 is a high-resistance circuit compared with the 12 MΩ of R_3. As soon as you connect a passive test circuit such as a resistor/inductor/LED, however, D_1 and R_2 are paralleled by it. Thus, the branch in parallel with R_3 has a lower resistance and the G_1 input voltage increases such that it is now recognized as logic 1, driving G_1's output low.

R_5 and C_2 form a debounce-and-delay network to ensure that the probes are firmly connected to the circuit under test before the power pulse is issued. When the output of G_1 goes low, capacitor C_2 begins to discharge through R_5. The logic input voltage of G_2 changes within a time on the order of R_5C_2.

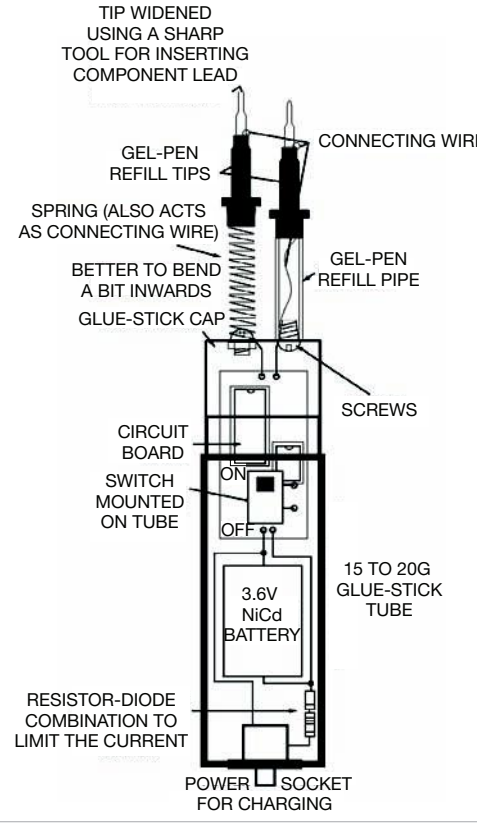

Figure 3 You can build the automatic pulse generator in a used glue-stick tube.

In **Figure 1**, the rising output of G_2 immediately triggers the NE555 monostable through G_3 and the differentiator formed by C_3 and R_6. Once C_3 has finished charging through R_6, G_3's input returns to ground and its output returns high to allow the NE555 to complete its timing cycle with a duration that its R and C values determine.[1] The timed logic 1 output of the NE555 turns on Q_3 to light the "pulse issued" LED, and through G_4, G_5, and G_6 turns on Q_1 and Q_2 to present the power pulse to the circuit under test.

Only one pulse is generated per contact; removing the probes and then reconnecting them will issue a new pulse. If the circuit under test is inductive and greater than 20 mH at

the end of the pulse, the inductive back EMF will flash LED D_1 if the probes are still connected.

In **Figure 2**, the NE555 has been replaced by a monostable comprising G_3 and G_4, D_4, and R_F. R_6 has been changed to 1 MΩ, and diode D_3 has been added to the input of G_3. Resistor R holds G_4's input high, which in the quiescent state causes G_4's output to hold G_3's input low. A rising edge from G_2 causes a low to couple through the initially discharged capacitor, C, to G_4, whose rising output is fed back to G_3 as positive feedback and holds G_3's input high even if the probes are removed. If this happens, D_3 becomes reverse biased and prevents G_2's falling edge from affecting the monostable operation.

Capacitor C then slowly charges through resistor R until G_4's input rises above its switching threshold, and the positive-feedback process reverses. The pulse duration depends on the R×C time constant, and is about 0.7 to 1.1 RC, depending on the G_4 threshold voltage, which can vary between 0.33 and 0.67 of the supply voltage. The author suggests 1 MΩ for R and 40 nF for C, but R could be made variable, as well. D_4 ensures that C discharges rapidly as G_3's output returns high.

In either case of **Figure 1** or **Figure 2**, the momentary high output of the monostable turns Q_3 on to flash the pulse-issued indicator LED. It also turns on both Q_1 and Q_2 to power the probes. D_2 serves to isolate the –ve probe from the primary input of the circuit at G_1 to avoid immediate self-suppression. EDN

REFERENCE

1 NE555 data sheet, Figure 11, Texas Instruments, June 2010, http://bit.ly/127p7kq.

Read 10 or more switches using only two I/O pins of a microcontroller

Aruna Prabath Rubasinghe, University of Moratuwa, Moratuwa, Sri Lanka

There are several ways to read multiple switch inputs using a reduced number of microcontroller-unit (MCU) pins. For example, you can use an analog MCU pin to read multiple switches by assigning a unique voltage to each switch through a resistor network, or you can use a one-wire device, such as the Maxim DS2408 8-channel addressable switch.

The first method has several disadvantages: The MCU has to have an ADC function, debounce wait times reduce the polling rate, and an error results if the switch is opened during the ADC sampling time. The second method also has the drawback of comparatively low speed; it uses 1-wire communica-

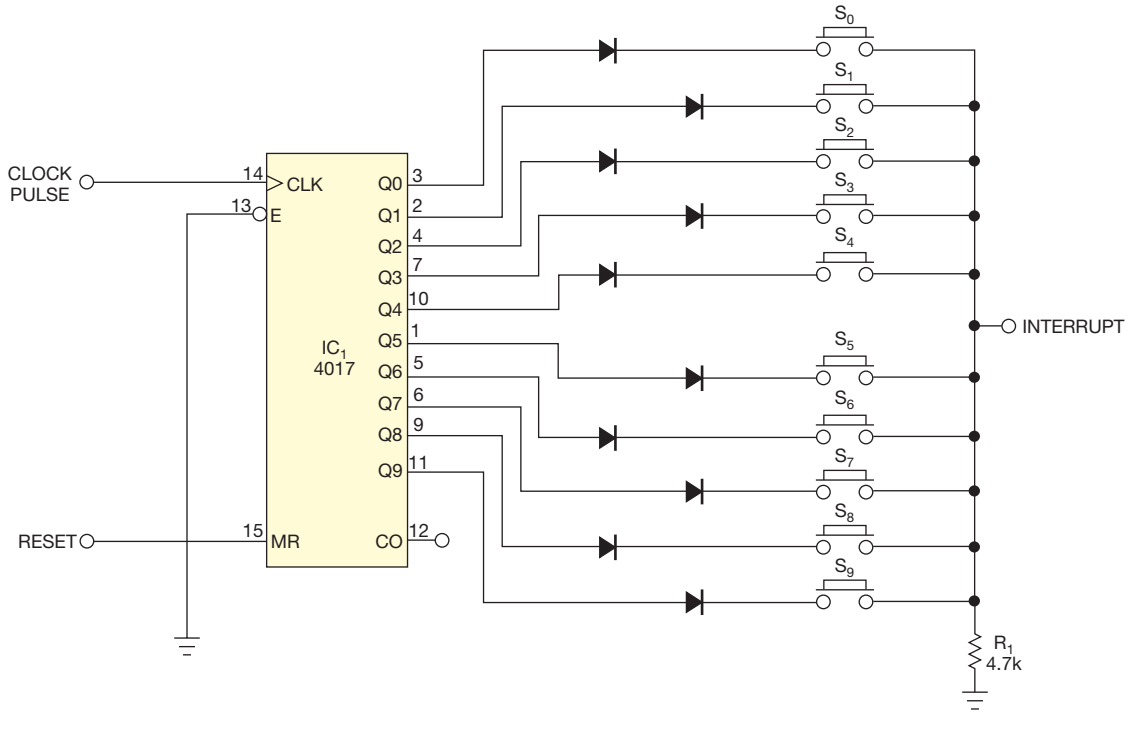

Figure 1 You can easily expand this circuit to many more than 10 switches, yet still use only two MCU I/O pins, by cascading multiple CD4017 counters through their carry-outs to the following enables.

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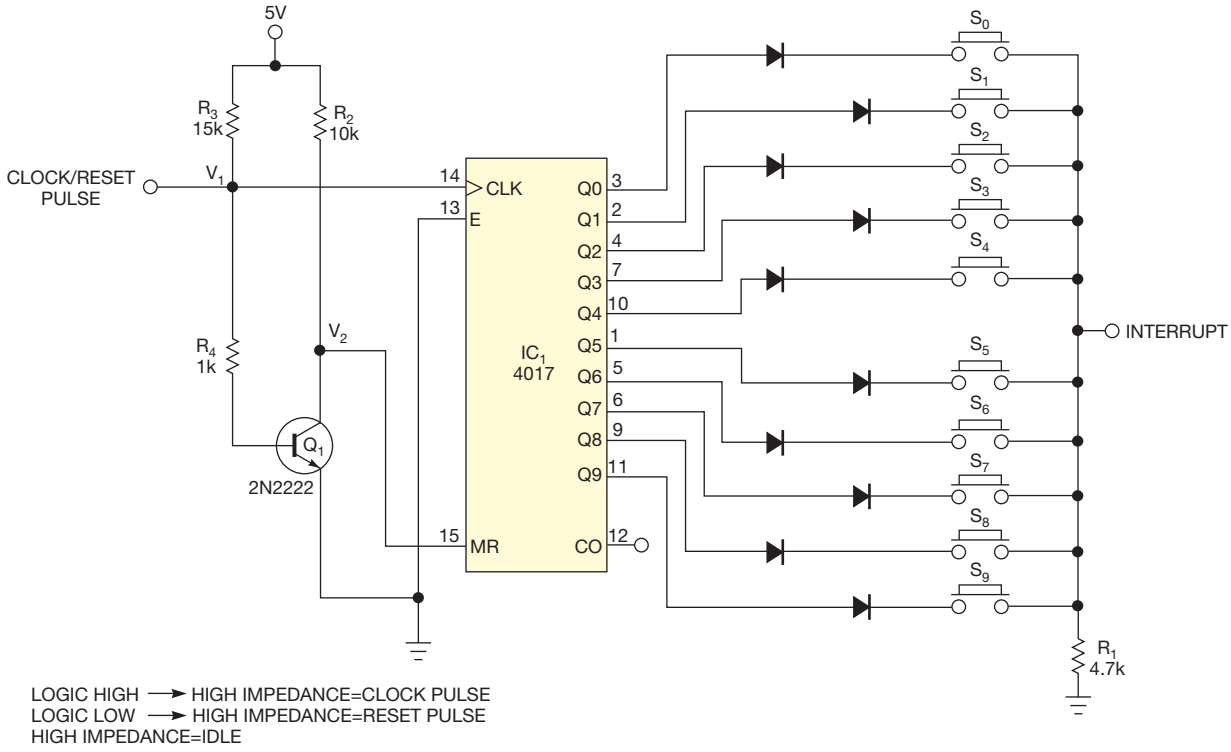

Figure 2 You can add three resistors and a transistor to implement the occasional synchronizing reset without using a third I/O pin.

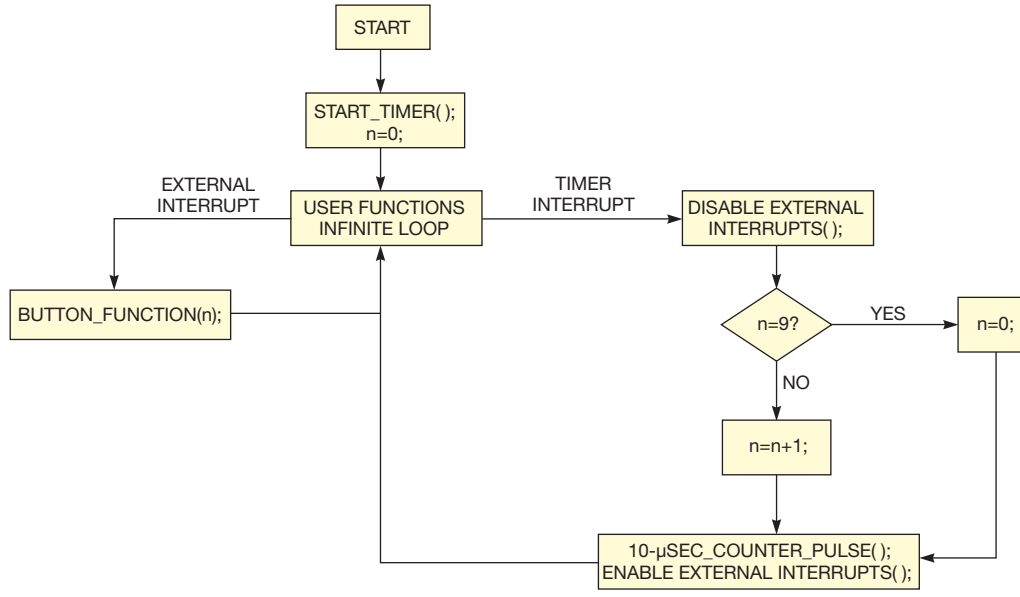

Figure 3 This flowchart displays the process for reading an all-pushbutton system. Only one button at a time should be pressed.

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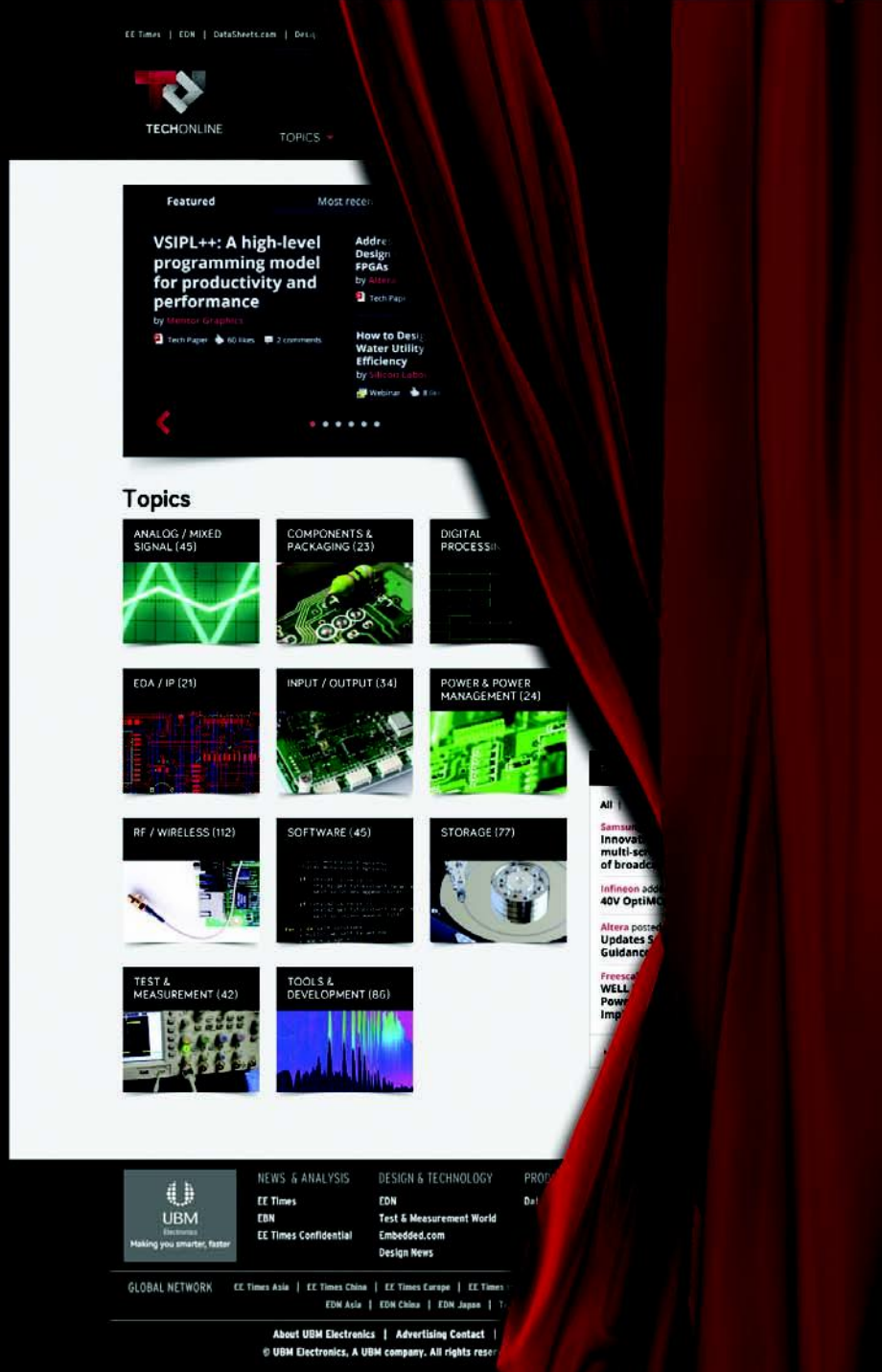

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tion, which requires continuous polling; and each poll generates an 8-bit data sequence relevant to switch positions.

This Design Idea describes a method for reading multiple pushbuttons or open/closed switches using only two digital I/O pins and a timer interrupt of the MCU (**Figure 1**). Optionally, a third I/O pin can be assigned to periodically reset the CD4017 (a cascadable decoded 1-of-10 Johnson counter) for reliable operation should an EMI or ESD event occur that could falsely clock the counter, or you can use the circuit shown in **Figure 2** and retain the two-pin feature. The diodes isolate the counter outputs in the event that two or more switches are closed at the same time. You can increase the number of switches connected by cascading multiple CD4017 ICs using a carry-out signal (pin 12) and a clock signal (pin 14).

Reliable operation following the initial power-up reset depends on the CD4017 counter's remaining synchronized with the MCU counter. This synchronization can be upset by an ESD or EMI event such as a nearby cell phone, so it would be wise to include in the firmware a periodic hardware reset to the CD4017 to keep the counts synchronized. **Figure 2** shows how you can do this without having to use a third MCU pin.

For this function, you use the MCU's ability to keep its I/O pin in three different states: high, low, and, by temporarily changing the pin to an input, high impedance.

In the logic-high state, transistor Q_1 turns on through R_4, making the voltage on V_1 logic high and the voltage on V_2 below the logic-low level. This sets the clock pin to a logic high while keeping the reset pin at a logic low.

In the logic-low state, transistor Q_1 turns off, making the voltage on V_1 logic low and the voltage on V_2 above the logic-high level. This sets the reset pin to logic high while keeping the clock in the logic-low state.

In the idle high-impedance state, transistor Q_1 is turned on through R_3 and R_4, making the voltage on V_1 and V_2 below the logic-low level. This sets both the clock and reset pins of the CD4017 to a logic-low state.

To send a clock edge, therefore, change the state in the following manner: high impedance > logic high > high impedance. Likewise, to reset the CD4017, change the state as follows: high impedance > logic low > high impedance.

The flowchart in **Figure 3** is for an all-pushbutton system and functions as follows: At the start, the MCU sets a counter variable to 0 and starts an interrupt-enabled timer, which is set to overflow and interrupt at 1-msec intervals. In the timer-interrupt routine, several tasks are carried out: External interrupts are disabled; the counter variable is incremented by 1; a 10-µsec clock pulse is sent to the CD4017; and the external interrupt is enabled.

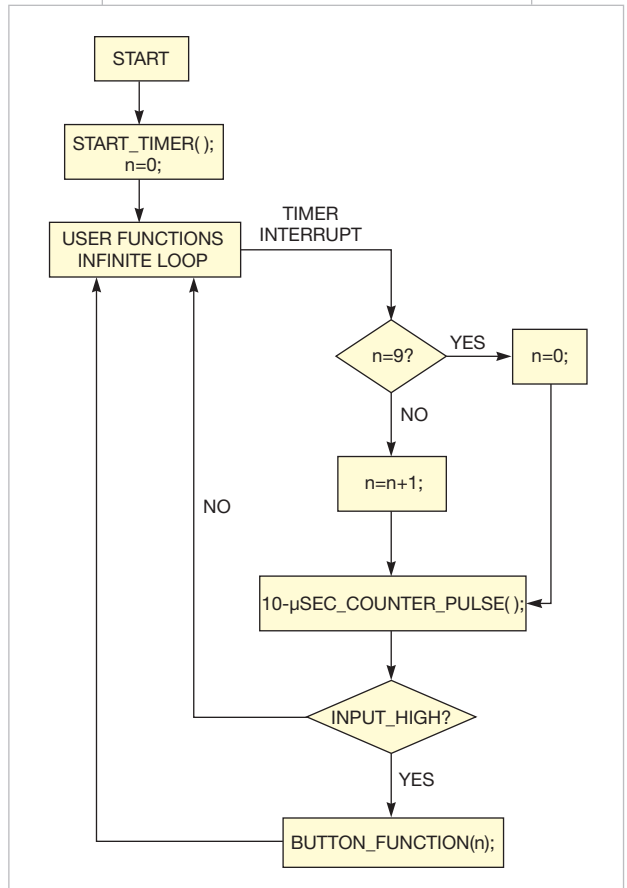

Figure 4 When non-momentary toggle switches are used, you can decode multiple combinations of switch closures by checking the state of the interrupt input.

A THIRD I/O PIN CAN BE ASSIGNED TO PERIODICALLY RESET THE CD4017 DURING AN EMI OR ESD EVENT.

As the MCU clocks the CD4017 every 1 msec and increments the counter variable by 1 if its value is less than 9, the CD4017 output corresponding to the counter-variable value goes to logic high from logic low; that is, if the counter-variable value is 2, then the decoded 2 output of the CD4017 (pin 4) is at logic high while all other outputs are at logic low. At this time, if the user pressed pushbutton S_2, it would send a logic-high signal to the external interrupt pin of the MCU. Pressing any other button does not generate external interrupts, because all other outputs of the CD4017 are in the logic-low state.

When the MCU receives the external interrupt, it gets the current counter-variable value (which is 2) from its memory, identifies the pressed button as S_2, and thus carries out the functions relevant to S_2. When the counter variable reaches 9, it is set to 0 through the software, as the CD4017 also resets automatically at the 10th pulse.

Note that only one button at a time should be pressed; if two consecutive buttons are pressed together, there may not be enough dropout time between successive counter states for the interrupt edge to register. You can resolve this issue by using the flowchart shown in **Figure 4**. EDN

Successfully choose complementary bipolar transistors

Peter Demchenko, Vilnius, Lithuania

For circuit designs that use complementary bipolar transistors, you sometimes need to sort the NPN and PNP transistors to have matching dc-current gains (β). One example of a circuit requiring matching is the output stage of an amplifier. The circuit in **Figure 1** shows a simple test fixture to achieve this match.

Transistors Q_1 and Q_2 are the devices being tested to see if they are matched. In the test fixture, Q_1 and Q_2 share the same base current (I_B); since there is no additional path where the current can flow, no additional compensation is needed. Note, however, that β should be high enough that $I_E \approx I_C$. With this detail in mind, resistors R_1 and R_2 should be equal.

To give the transistors a bit more headroom, an additional voltage drop is introduced between the transistors' base connections. A voltage differential of a few volts is desirable, so a blue LED is a good choice for D_1. Its presence helps to set the base voltage for Q_1 (V_{B1}) to about half of the supply voltage (V_S). Using an LED in the place of D_1 is preferable to using a zener diode due to the sharper knee at the low currents. Moreover, you can see the glow of many blue LEDs at currents below 10 µA; the glow indicates the presence of base current, which means the circuit is working properly. **Equation 1** is used to determine the needed supply voltage:

$$V_{BE1}+V_D+V_{BE2} \approx V_S/2 \qquad (1)$$

A typical blue LED will have a forward voltage of about 3.5V; assuming $V_{BE1}=V_{BE2}=0.7V$, you get a value for V_S of about 9.8V.

Resistor R_1 sets the emitter current of Q_1; it is calculated using **Equation 2**:

$$R_1=(V_S-V_{BE1}-V_D-V_{BE2})/I_{E1} \qquad (2)$$

You should select an emitter current that matches the application in which the transistors will be used, because beta varies with emitter and collector current. With matching transistors ($\beta_1=\beta_2$) installed in the test fixture, the voltage drops across R_1 and R_2 are equal, and the voltmeter will show 0.

The circuit in **Figure 2** is functionally equivalent but uses a simpler method to indicate when the circuit is in balance. With matched gains, neither of the red LEDs (D_2 and D_3) will be on. EDN

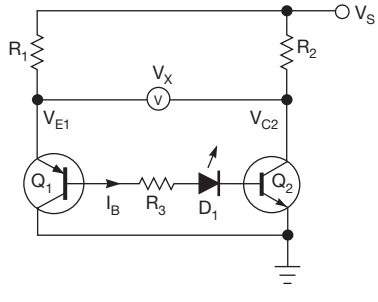

Figure 1 This circuit makes it easy to test and match the current gain of complementary bipolar transistors. Matched transistors will cause the voltmeter to read 0V.

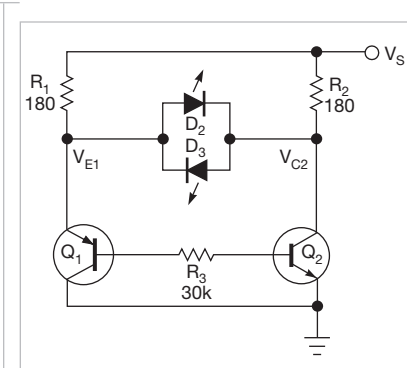

Figure 2 For a simpler version, replace the voltmeter with inverse-parallel-connected red LEDs.

Originally published in the March 17, 1994, issue of *EDN*

Synchronized regulator produces coherent noise

Jim Williams, Sean Gold, and Steve Pietkiewicz, Linear Technology, Milpitas, CA

By using a gated-oscillator architecture instead of a clocked-PWM one, gated-oscillator-type switching regulators permit high efficiency over extended ranges of output current. This architecture eliminates the housekeeping currents associated with the continuous operation of fixed-frequency designs. Gated-oscillator regulators simply self-clock at whatever frequency is necessary to maintain the output voltage. Typically, loop-oscillation frequency ranges from a few hertz to the kilohertz region, depending on the load.

In most cases, this asynchronous, variable-frequency operation doesn't create any problems. However, some systems are sensitive to the asynchronous characteristics. The system in **Figure 1** slightly modifies a gate-oscillator-type switching regulator by synchronizing its loop-oscillation frequency to the system's clock. The oscillation frequency and its attendant switching noise, albeit variable, become coherent with system operation.

To analyze the system in **Figure 1**, temporarily ignore the flip-flop, and assume the circuit directly connects the A_{OUT} and FB pin of the LT1107 regulator. When the output voltage decays, the set pin drops below V_{REF}, causing A_{OUT} to fall. The internal comparator then switches to high, biasing the oscillator and output transistor into conduction. L_1 receives drive pulses, and the circuit deposits this inductor's flyback events into the 100-µF capacitor via the diode, ultimately restoring output voltage. This action overdrives the set pin, causing the IC to switch off until it requires another cycle. This oscillator cycle's frequency is load-dependent and variable.

Now, interposing a flip-flop into the path between the A_{OUT} and FB pins, as the **figure** shows, synchronizes the regulator to the circuit-generated clock. When the output decays far enough, the A_{OUT} pin goes low. At the next clock pulse, the flip-flop's Q_2 output sets low, biasing the comparator-oscillator. This turns on the power switch, which pulses L_1. L_1 responds in flyback fashion and deposits its energy into the output capacitor to maintain output voltage. This operation is similar to the previously described case, except that the flip-flop now synchronizes the sequence of events with the system clock. Although the resulting loop's oscillation frequency is variable, the frequency and all attendant switching noise are synchronous and coherent with the system clock.

The circuit requires a start-up sequence because the output provides power for the clock. The circuit connects the flip-flop's remaining section as a buffer to furnish start-up. The flip-flop's connected CLR_1 and CLK_1 lines monitor output voltage via the 221-, 82.5-, and 100-kΩ resistor string. When power is applied, Q_1 sets CLR_2 low, which permits the LT1107 to switch, thereby raising the output voltage. When the output goes high enough, Q_1 sets CLR_2 high, and normal loop operation commences. Although this circuit uses a step-up regulator, the technique also works with other types. EDN

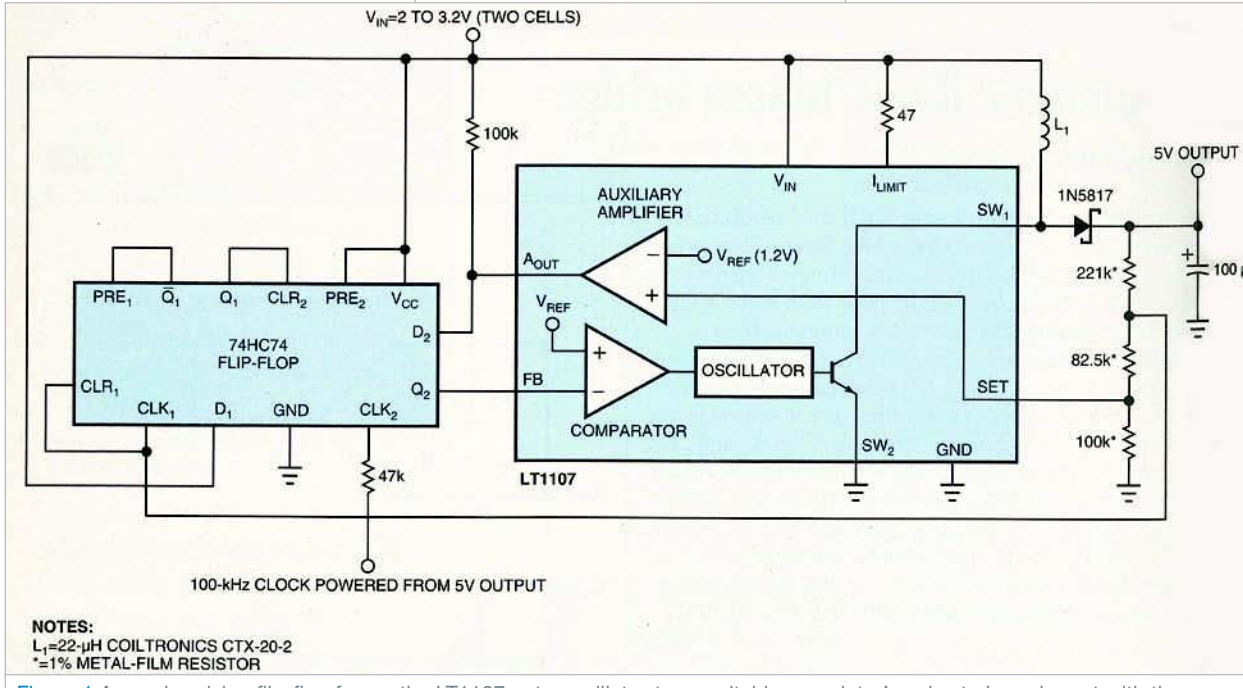

Figure 1 A synchronizing flip-flop forces the LT1107 gate-oscillator-type switching regulator's noise to be coherent with the 100-kHz clock.

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Adding or subtracting a link in the supply chain is never easy. A single substitution of a component, for example, affects other components on the board, pricing, delivery considerations, and even relationships. But buyers have to hedge their bets to ensure a single component doesn't hold up production.

Numerous considerations belong in this category of risk management. The risk of any one thing going wrong between design and production is considerable and is one of the challenges that keep supply-chain managers up at night, according to research conducted by UPS and IDC.

There's no shortage of options in risk management: Companies can calculate it internally; consultants are widely available; distributors consider it part of their core competency; factories hedge against not filling an order; and even logistics companies are entering the fray. An overall risk-management strategy comprises cross-functional groups within an OEM and C-level executive involvement. But buyers play a significant role, as well. Much of this contribution involves relationship management with supply sources and dealing with "exception management" situations.

The classic situation is the component that is hard to find or can't be sourced at the last minute. Most OEMs develop an approved-vendor list that designates two or more sources for a particular component and can be programmed into a system and automated. But the typical forecast window of six weeks or more means that component lead times may change or that there can be rapid shifts in supply and demand, as the industry experienced during the 2011 Japan earthquake and tsunami. This is where buyers contribute most to an effective supply chain.

> In the semiconductor market, no matter how good forecasting is, it takes 16 weeks to manufacture a component.

The first line of defense in a shortage is the component supplier. In times of scarcity, however, the supplier's largest customers will be first in line for delivery. In the semiconductor market, no matter how good forecasting is, it takes 16 weeks to manufacture a component.

Distribution is usually the next stop. Distributors, like suppliers, manage their inventory to customer forecast, but build in both upside and downside parameters for inventory buys. Chances are if one customer cancels an order, there are other customers that also use that part. Strategically, smart buyers will manage relationships directly with both suppliers and distributors. Like suppliers, distributors will try to respond first to their largest or most dependable customers.

For distributors, however, orders change every day, not just in times of crisis. Suppliers or customers may go out of business or discontinue certain product lines. These factors are part of inventory-purchasing decisions. Distributors are likely to have buffer stock for hard-to-find parts, or have an order on the supplier's books if there's a shortfall in finished goods.

When all else fails, buyers can go to the open market or through independent channels. They face several issues in the open market, however. Parts that reach the open market may not carry the manufacturer's warranties unless they are sourced through an authorized channel. Counterfeit parts also enter the channel through open-market deals where bogus parts are mixed in with legitimate components. Authorized channels remain skeptical of the screening procedures.

Sources of authentic parts are available. Authorized distributors will buy inventory when a part reaches its end of life or buy the die, masks, and IP from the original component vendor. When necessary, some of these companies can manufacture components using the original specs. This solution tends to be costly, however, as these businesses don't typically own their own fabs and parts aren't manufactured in massive volumes.

—by Barbara Jorgensen

This story was originally posted by EBN: *http://bit.ly/Vujs8P.*

OUTLOOK

PV INDUSTRY TO SEE INSTALLATION GROWTH, REVENUE DIP

The number of global photovoltaic (PV) installations will see a continued increase in 2013, but the industry will nonetheless experience a decline in overall revenue due to lower volume growth and decreasing system prices, according to market-intelligence firm IHS.

PV installations are projected to reach 35 GW this year, up from 32 GW in 2012. In comparison, industry revenue—system price multiplied by total gigawatts installed—will decline to an estimated $75 billion (down from $77 billion last year) and exhibit an even steeper fall from the market's peak revenue of $94 billion in 2011.

"The conflicting trend of growing PV installation volumes accompanied … by falling revenues will challenge solar companies to continue to reduce their cost structures," says Ash Sharma, director of syndicated solar research for IHS.

Another issue, Sharma adds, will be the rapid globalization of the industry. Europe accounted for more than 80% of solar demand in 2010, but its 2013 share is forecast to slide to 39%. Asia, meanwhile, is on track to replace Europe as the world's largest source of solar installations. **—by Amy Norcross**

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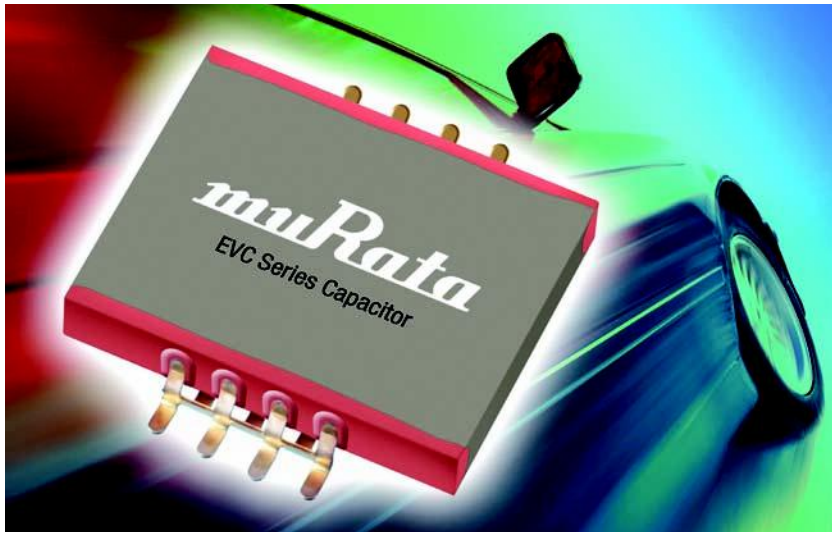


Murata develops high-permissive-current capacitor for automotive market

Murata has added three multilayer monolithic ceramic capacitors to its EVC series of high-permissive-current capacitors aimed at automotive applications. These surface-mounting capacitors measure 16×20 mm and have an EIA U2J temperature characteristic that supports an operating temperature range from –55°C to +125°C. An absolute maximum case temperature of +150°C is permitted for a short duration. The additions to the EVC series offer 1.2 µF/500V dc, 300 nF/1 kV, and 100 nF/1.4 kV. The maximum allowable current, at 100 kHz, is 30A (RMS). Products in the EVC series can be used as smoothing or snubber capacitors for inverter/converter applications or as resonance capacitors for wireless charging systems.

Murata Manufacturing Co Ltd, www.murata.com

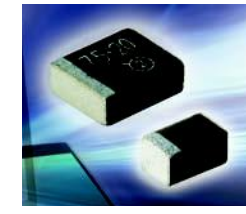
TE Connectivity connectors eliminate soldering

The Mag-Mate connectors from TE Connectivity include multispring pins that streamline the manufacturing process by eliminating the need to solder magnet wires to PCB connections in motors and coils. The solderless press-fit multispring pins also prevent heat damage to board-mounted components. An insulation-displacement connection (IDC) slot on the connectors further aids manufacturing by simultaneously stripping up to two magnet wires of the same size during termination. No prestripping, welding, or soldering is required. Five Mag-Mate connector types accommodate copper-magnet-wire sizes of 0.18 to 0.265 mm (31 to 33 AWG), 0.265 to 0.4 mm (26 to 30 AWG), 0.63 to 0.85 mm (19 to 23 AWG), 0.85 to 1.12 mm (17 to 19 AWG), and 0.4 to 0.63 mm (23 to 26 AWG). The connectors are available in strip form for semiautomatic or fully automatic insertions. A clean metal-to-metal interface produces stable, gas-tight electrical terminations free of oxides and other contaminants.

TE Connectivity, www.te.com

Vishay introduces solid tantalum chip capacitors

Designed for space-constrained applications, the TL8 series of molded Microtan solid tantalum chip capacitors from Vishay Intertechnology employs a high-volumetrically efficient packaging solution to enable high capacitance-voltage (CV) ratings in a low-profile case (0.8 to 1 mm). High voltage ratings make the devices suitable for OLED displays. The TL8 capacitors are available in a variety of footprints, including the 0805 (2×1.25 mm), A case (3.2×1.6 mm), and B case (3.5×2.8 mm). The devices feature high CV ratings from 3.3 µF-35V to 220 µF-4V, standard capacitance tolerances of ±10% and ±20%, and an operating temperature range of –55°C to +85°C, or +125°C with voltage derating. The RoHS-compliant devices are available in 8-mm tape-and-reel packaging. Pricing for US delivery starts at $0.08 per piece.



Vishay Intertechnology, www.vishay.com

Molex connector system handles up to 100A per bay

The EXTreme EnergetiC High-Current Connector System from Molex, which handles applications requiring high current of up to 100A per bay, is intended for use in high-end computing, datacom, and power-supply equipment, including 1U/2U servers,

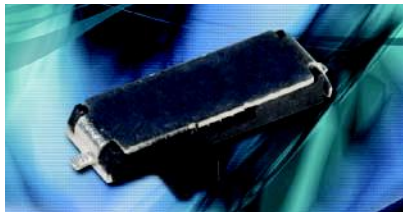
modular power supplies, and power-distribution circuit boards. The connector system is available in right-angle plug and vertical-receptacle configurations, with 4- and 6-power blade bays and a 25-signal bay. Configurations can be designed to support various applications.

Molex Inc, www.molex.com

C&K Components subminiature slide switch has life of 100,000 cycles

The JSX Series SPDT momentary action switch from C&K Components is a subminiature slide switch for consumer-electronic devices. The low-profile (2.6×7.6 mm) JSX switch has an extended electrical and mechanical life of 100,000 cycles, and its tape-and-reel packaging makes it ideal for high-volume assembly. Typical applications include on/off touchscreens, handheld games, remote controls, and instrumentation. Available in a glass-filled housing with a 4/6 nylon (UL94V-2) actuator, the JSX Series switch features beryllium-copper and silver-plated contacts. Phosphor-bronze or silver-plated terminals and a stainless-steel cover and return spring allow for the 100,000-cycle life span. The JSX Series switch's contact rating of 10 mA at 5V dc (resistive), maximum contact resistance of 70 mΩ, and dielectric strength of 100V ac for one minute at 50/60 Hz and 2 mA allow it to be integrated into various applications.

C&K Components, www.ck-components.com



Kemet's high-voltage bulk capacitors save board space

The Kemet Power Solutions (KPS) high-voltage stacked capacitors in X7R dielectric employ a proprietary lead-frame technology that vertically stacks one or two MLCCs in a single surface-mount package. The two-chip vertically stacked device offers up to double the capacitance of a single capacitor in the same or smaller footprint, saving board space in a design. KPS series devices, which are available in rated voltages of 500V dc and 630V dc and an operating temperature range of –55°C to +125°C, provide board flex capability up to 10 mm. The lead frame isolates the capacitors from the PCB to provide better mechanical and thermal stress performance and to address concerns about audible microphonic noise that may occur when a bias voltage is applied. The devices are available in commercial and automotive grades and are suited to applications such as switching-power-supply smoothing circuits, snubbers in lighting ballast circuits, and high-voltage coupling/dc blocking in inverters.

Kemet, www.kemet.com

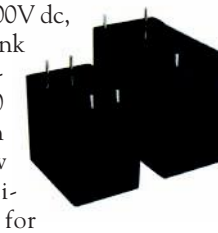
Vishay supports solar apps with snap-in power aluminum capacitors

The 193 PUR-SI Solar snap-in power aluminum capacitors from Vishay Intertechnology have a rated voltage of 500V at 50°C and a category voltage of 450V at 105°C. Designed for solar applications, where the highest voltage is present under no-load conditions, the 193 PUR-SI Solar devices feature a rated ripple current of up to 2.52A at 105°C and 100 Hz. At 500V, the devices feature a maximum operating temperature of 50°C and a useful life of 5,000 hours (no ripple current applied). At 450V, the maximum temperature can be extended to 105°C with a useful life of 6,000 hours. As polarized aluminum electrolytic capacitors with a non-solid electrolyte, the 193 PUR-SI Solar devices are suited for smoothing, filtering, and energy storage in pulsed-power applications. End products include solar photovoltaic inverters, industrial motor controls, and power supplies. Five case sizes are available, ranging from 35×30 mm to 35×60 mm. Pricing for US delivery starts at $5.50 per piece.

Vishay Intertechnology, www.vishay.com

Cornell Dubilier releases type-BLC DC link capacitors for inverter systems

Cornell Dubilier's type-BLC high-energy-density, board-mount, dc link capacitors are designed for medium-power inverter systems used in wind and solar energy systems, electric vehicles, motor drives, and UPS systems. Available in values from 8 to 55 µF and in voltage ratings from 700V dc to 1100V dc, the type-BLC dc link capacitors are packaged in UL94V-0 plastic boxes with four pins for low ESR. These capacitors are designed for long life at high ripple current, up to 36A, with a 25-year life under typical operating conditions. In OEM quantities, prices start at $4. Samples are available in 4 to 6 weeks.



Cornell Dubilier, www.cde.com

productroundup

SMD wirewound resistor from Ohmite handles more than 5W

By using a simple idea from its heat-sink designs, Ohmite reports it has developed SMD wirewound resistors that meet 5W power ratings. The new design incorporates fins in the body of the resistor, creating an additional surface area within the same resistor footprint. The company offers the resistors in 5W and 7W versions, and because tests performed over 1000 hours of continuous operation demonstrated that the resistance drift was negligible (less than 1%), customers can specify very tight tolerances along with the new, higher power ratings. A couple of fins have been removed to allow for a flat zone on the top center of the resistor to enable its use on pick-and-place equipment.

Ohmite, www.ohmite.com

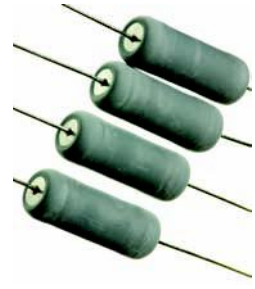
Tiny audio transducer from Transducers USA delivers 80 dBA SPL

The Model TRSTE-5025 surface-mount audio transducer from Transducers USA produces a very high sound-pressure level (SPL) of 80 dBA minimum in a miniscule 5×5×2-mm package. The top port sound release of the TRSTE-5025 makes it suitable for handling the size constraints of small, battery-operated products such as cell phones, handheld GPS units, and portable alarms. The device operates from a voltage range of 2 to 4Vp/p at 90 mA. Output frequency is 4000 Hz in an operating temperature range of –30°C to +85°C. The TRSTE-5025 transducers are shipped in a tape-and-reel package that is compatible with solder-reflow production. Pricing is $0.90 each (production quantities).

Transducers USA, www.tusainc.com

Wirewound resistors from TT Electronics offer surge energy ratings up to 7W

With surge energy ratings ranging from 2 to 7W, the WHS series of flame-proof, wirewound resistors from TT Electronics is suitable for use in power supplies that require a line-input resistor for inrush limiting and protection. The WHS resistors feature a winding design in which a high-purity ceramic substrate is assembled with interference fit end-caps welded to the terminations. The resistive element is then wound on the substrate and welded to the caps. The design enables the resistors to withstand the high surges associated with switch-on, discharge, and external surge events. The WHS2, rated at 2W, provides surge energy ratings of 0.9 to 5.8J. Other models in the series carry ratings of 3, 5, and 7W, in resistance values to 330Ω and surge energy ratings to 60J. All models have UL94-V0 flame-proof protection and operate over a temperature range of –55°C to +155°C.



TT Electronics,
www.ttelectronics.com

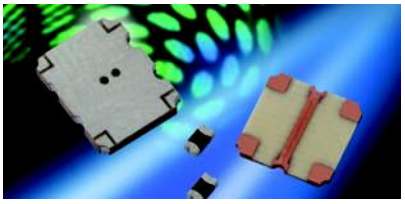
Bulgin's push-pull coupling connectors withstand harsh environments

The Buccaneer 6000 Series of waterproof power, signal, and data connectors from Bulgin features an easy-to-use push-pull latching mechanism, combined with a 30° twist lock, that can connect up to 10 times faster than a traditional screw-thread mechanism. This latest addition to the Buccaneer family, which complements the screw-thread Buccaneer models, is designed to withstand the harshest environments and meets IP66, IP68, and IP69K standards. The Buccaneer 6000 Series includes data (USB or Ethernet), signal, and power versions up to 16A, 277V. Available in interchangeable metal and plastic constructions, the body moldings and pin carriers create a robust interface while avoiding damage during coupling. The company says this design guarantees a correctly sealed connection, even where access is restricted.

Bulgin, bulgin.co.uk

Multilayer capacitors from AVX target RF applications

The MLO3 Series surface-mount capacitors from AVX Corp are available in 500V dc and 250V dc versions that support frequencies ranging from 1 MHz to greater than 5 GHz. The polymer-based capacitors, which are based on AVX's multilayer low-loss organic (MLO) technology, use high-conductivity copper interconnects and are designed for RF power and low-noise amplifiers, filter networks, and MRI systems. The RoHS-compliant RF capacitors are rated for 50V dc to 500V dc and feature capacitance values ranging from 0.1 to 2.5 pF and capacitance tolerance



to ±0.02 pF. AVX reports that the capacitors maintain high Q and high self-resonance while providing low ESR values at high frequencies. Available in the 0603 case size with a 100% tin finish, the MLO3 Series features stable NPO characteristics and an operating temperature range of –55°C to +125°C. **AVX Corp, www.avx.com**

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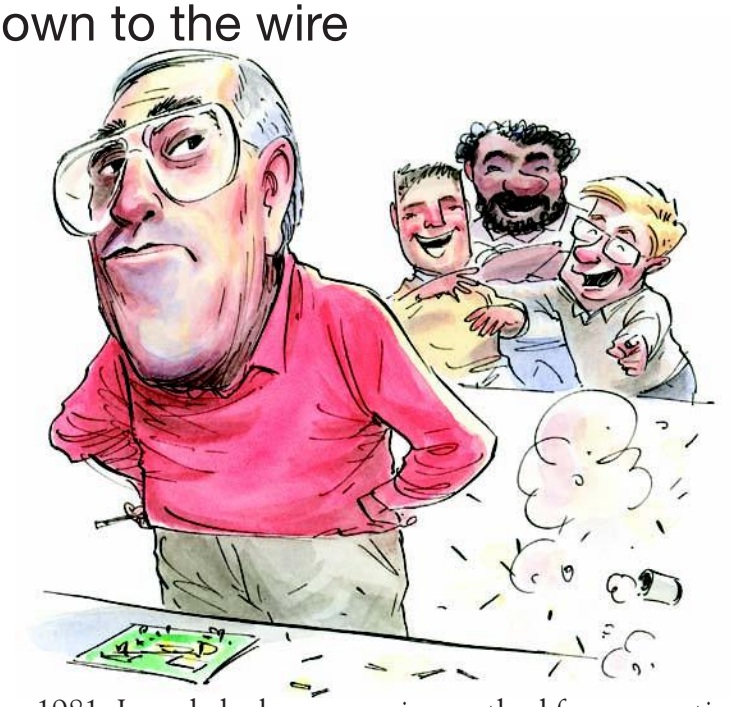
Rush-project troubleshooting comes down to the wire



In 1981, I needed a less expensive method for connecting ICs than the standard etched-copper PCB. I was looking for a method that would produce circuits faster than prototype PCB fabrication and that would allow many changes to be made quickly at low cost. I chose wire wrap, which was used a lot in that decade of digital circuits.

The wire-wrap process uses a motorized tool that wraps a small-gauge (30 AWG) wire tightly around each square IC socket post. The four square corners on the socket posts dig into the wire to provide a low-resistance electrical path. Little did I realize the troubleshooting problems that lurked ahead when I chose this manufacturing method.

The rush was on to wire a dozen board types for a prototype and production system. We chose a universal board with 12 rows of 100 wire-wrap pins. The 100 pins allowed the use of five DIP ICs with 20 leads, seven 14-pin ICs, or any combination not exceeding 100 pins.

Two technicians wired all of the boards using the wire-wrap method. With today's electronic cross-checking tools, we have come to expect 100% of our boards to work 100% of the time. Thirty years ago, we were getting only half the boards to work the first time.

To troubleshoot the faulty wire-wrap boards, we used a good board and traced the clock and other signals from the origination to the next IC. Was too much capacitance loading down the clock oscillation?

We did not have the problem Tracy Kidder describes in his book *The Soul of a New Machine*. Kidder relates a story in which short pieces of wire-wrap wire broke off, shorting various points together. Initial wraps might have been perfect, but when the unwrapped wires were used again, it was common for a half-inch piece of wire at the end to break off and fall into the maze of pins and wires, creating electrical havoc.

In our case, the oscillator ran on the faulty board, but the rest of the board did not function. To troubleshoot, we used a Tektronix 455 scope, putting the amplitude control on the variable setting and then looking at any 5, 12, or 15V signals within that one setting. In that fashion, we could look at an entire signal chain by just moving the scope probe and not adjusting the scope.

While troubleshooting, I heard a "pop" that sounded as if a circuit breaker or a polarized capacitor had exploded. I jumped back a few steps and then noticed the gaggle of engineers nearby who were trying to suppress their giggling. At my feet was the flexible cap of a plastic container—similar in size to the old 35-mm film canisters—that stored connector pins. The engineers had sprayed "freeze spray" into the container until the air and sides inside were at −50°C, then quickly capped the container and left it to sit at room temperature. After a few minutes, the air inside heated to room temperature, and the resultant pressure forced off the cap. Creative coworkers have always liked to "help" in difficult situations.

I rapidly moved the scope probe and looked at all the logic-level signals on the board's complement of ICs. At first glance, everything looked OK. I then went back and slowly examined each waveform. Instead of a large TTL-level voltage swing out of the 74LS04, I was getting a 2V swing. A closer look revealed logic levels of +5 and +3V dc. Even the ground pin was at 3V!

I carefully looked at the bottom of the board to examine the next IC in the signal path after the oscillator. Through the haystack of wires, I saw a wire on the V_{CC} (pin 14) going to +5V dc but did not see any wire on the ground (pin 7). The technician who had wired the boards made a habit of putting all the V_{CC} and ground connections on first. The other technician did not, however, and he had forgotten some of those ground connections. A quick wire wrap on each IC pin 7 to ground fixed the faulty boards.

So in this case of "haste makes waste," I learned that though a schematic can be absolutely correct and perfect, it takes an entire team to produce a successful product. EDN

Bruce Bushey, now a test engineer, was an electronics hobbyist for many years before starting electrical-engineering classes at North Dakota State University (Fargo, ND).

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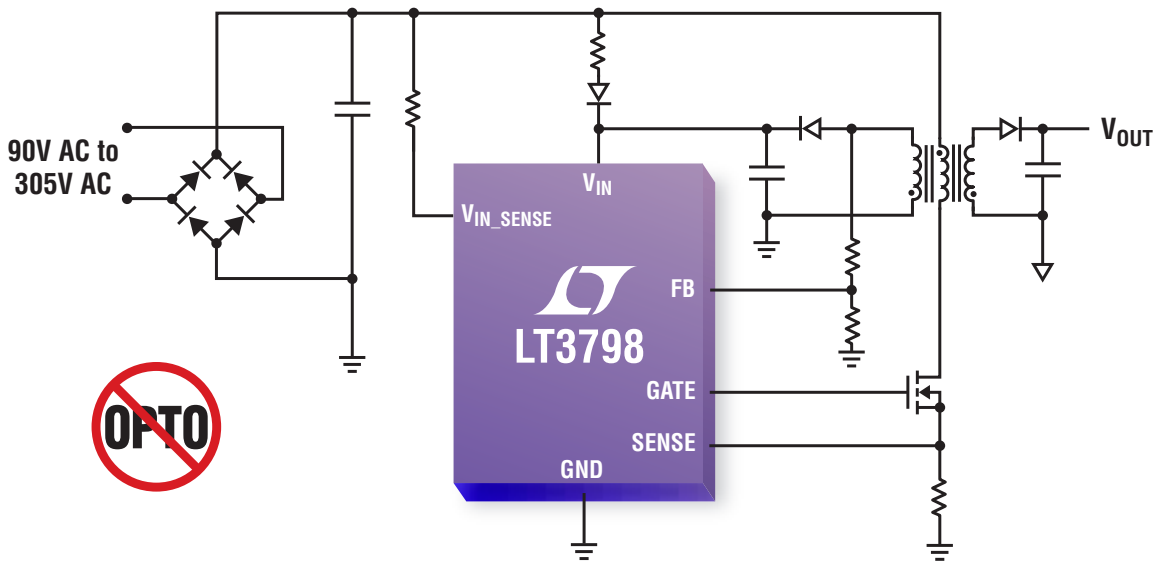
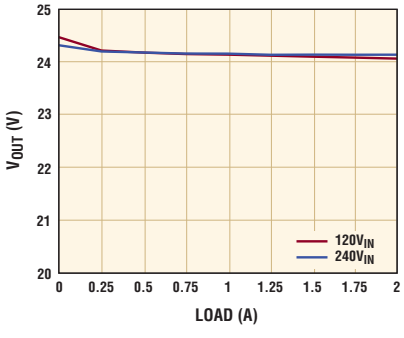


Simple AC/DC Conversion with Active Power Factor Correction

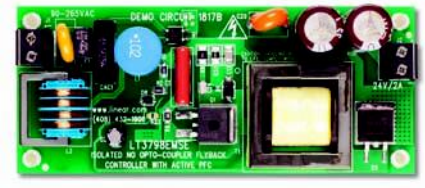
The LT®3798 is a general purpose isolated offline flyback controller that combines active power factor correction (PFC) with no optocoupler required for output voltage feedback into a single-stage converter. The device modulates input current in phase with line voltage to attain a PF greater than 0.97. It has both a voltage and current loop so it can provide a constant current or constant voltage (CCCV) output. Its internal architecture provides low harmonic distortion and delivers efficiencies as high as 90%.

Output Regulation



LT3798 Demo Board

(4.45" x 1.75" x 1.25")



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