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12 Measure and reduce IMD from spectrum analyser /DUT interactions

Intermodulation (IM) distortion is typically caused by active elements within the communication system. It can be measured and corrected using several techniques. As is the case in many precise measurement situations, however, care must be taken to avoid having the measuring instrument contribute to IM effects. This article describes the interaction between IM products generated by a device under test (DUT).

by Michael Simon, Rohde & Schwarz

17 Optimising high-performance CPUs, GPUs and DSPs? Use logic and memory IP

Mobile communications, multimedia and consumer systems-on-chip (SoCs) must achieve the highest performance while consuming the minimal amount of energy to achieve longer battery life and/or fit into lower cost packaging. CPUs, GPUs and DSPs typically each have unique performance, power and area targets for each new silicon process node. Each new generation brings a new set of challenges to SoC designers and a new set of opportunities to create higher performance and more power-efficient IP to enable SoC designers to deliver the last megahertz of performance, while squeezing out the last nanowatt of power and last square micron of area..

by Ken Brock, Synopsys

20 Basic concepts of linear regulator and switching mode power supplies, part 2

This article explains the basic concepts of linear regulators and switching mode power supplies (SMPS). It is aimed at system engineers who may not be very familiar with power supply designs and selection. In part 1 of this article the author covered the basic operating principles of linear regulators and SMPS, including the operation and sources of losses in a buck converter. He continues now with a discussion of design considerations of the switching power components in the converter.

by Henry J. Zhang, Linear Technology

27 Filter futures; SAW, BAW and emerging wireless standards

RF interference has always been an inhibitor of communications, requiring designers to perform major feats to keep it in check. Today's wireless devices must not only reject signals from other services but from themselves, too, as the number of bands packed inside each device increases. A high-end smartphone must filter the transmit and receive paths for 2G, 3G, and 4G wireless access methods in up to 15 bands, as well as Wi-Fi, Bluetooth and the receive path of GPS receivers. Signals in the receive paths must be isolated from one another. They also must reject other extraneous signals whose causes are too diverse to list. Without acoustic filter technology, it would be impossible.

by Robert Aigner, Triquint Semiconductor

Cover image

This month's cover shows screen detail from Yokogawa's latest generation of ScopeCorders – more on page 8

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DIGITAL POWER: YOUR NEW BEST FRIEND?

A number of recent power-supply and regulator product introductions that have been published at www.edn-europe.com have drawn attention to what might amount to a trend. A while back – I'm sure you remember – everything in the power world was (we were told) poised to go digital. The performance demanded of point-of-load regulators was approaching the point where only a high-performance, possibly DSP based, digital control loop would be able to cope. If you wanted to design a high-performance power regulation function, you would need to get coding, and in the passing, you'd gain all the advantages of digital connection – comprehensive monitoring and fault management, remote control, plus a system-level view of power usage. Not surprisingly, the power design community was sceptical. In some scenarios – large data centres, for example – the case for hierarchical power control and monitoring from AC inlet to point-of-load is compelling. Although, even there, it's not clear to what extent it's actually being implemented as against being an aspiration. A lot of other designers remained, and remain, to be convinced that the return – whether in efficiency, or performance, or any other parameter – justified adopting a whole new methodology.

Perhaps as a result, I've noticed a stream of products that, in various ways, package up the digital power function, reap some of its potential benefits, and make it accessible without the user "buying in" to the complete digital picture. For example, there's CUI's NSM2P Novum No-Bus PoL modules that use a digital control loop that you set up then leave to run stand-alone – you can have reporting over a bus connection if you wish, but you don't have to code anything. Or Intersil's power controllers that carry out automatic loop compensation; or ZMDI/Murata's fully-digital PoL power blocks. Other similar stories are here, or here, or here; the overall impression is that the module makers, at least, have got the message that if they want to get designers using digital power architectures, they had better wrap them up in an accessible format.

In the US, my colleague Bill Schweber has been having similar thoughts; let me pass you over to him;

"Nearly all power-supply regulators – whether AC/AC, AC/DC, DC/DC, or DC/AC – use some sort of closed-loop feedback topology to maintain the desired output despite line, load, and other changes. Smart (or experienced) system designers know that a solid supply is the foundation for overall product reliability, as it keeps the circuit free of frustrating, intermittent supply-related glitches and malfunctions.

"Traditionally, the closed loop has been implemented entirely via analog circuitry. Power-supply circuit designers have not only developed innovative, clever, and quite successful analog closed-loop configurations which meet many input/output requirements, they have also been able to accommodate other priorities such as the need for low noise, good transient response, power-factor correction (PFC), and efficiency. These topologies require deep understanding of the primary,

secondary, and even tertiary characteristics of the active and passive components in the design. It is not news that it's a long way from a good schematic to a good physical realization of power-supply regulator.

"But the digital winds are blowing through the power supply world, and it is not just to keep things cool. The actual closed loop is going digital, as we see from many recent product announcements. As usual, a technical trend that began with discrete-component, larger, more-expensive designs is now trending down to modules and even ICs.

"Closing the loop digitally goes beyond just setting critical loop parameters digitally but still closing it via analog circuitry, which has been done for a few years. Instead, it's handing over the actual regulatory control to A/D and D/A converters working with a processor and firmware – something the justifiably cautious and conservative supply regulator world has been hesitant to do.

"Going digital for the loop makes a lot of sense, at least in theory. It allows the supply dynamics to be more closely tailored to the needs of individual applications. It also makes it easier to meet the often conflicting demands of multiple performance attributes, and move the "compromise" sweet spot around a little as marketing revises the priorities.

"Is "going digital" a good thing, or not? As with so many questions in engineering, the answer is simple: it depends. It certainly has the potential for improving performance and simplifying hardware design, since it allows designers to implement control strategies that would be difficult, if not impossible, to do otherwise. It also allows the same circuit to offer different control strategies, such as for a DC/AC inverter, which can be instructed to provide a choice between low-distortion, stepped-sine output versus a square-wave output with higher distortion but greater efficiency.

"But I also worry that the responsibility that comes with this flexibility is a temptation and weak spot. It's not that there will be bugs in the software – there will be those – but the flexibility of software means that some vendors will use it as an excuse to get lazy to cut corners to meet schedules. We've seen this before, the feeling that the product can be fixed in the field via upgrades.

"Further, users suffer as the product's characteristics change, often without their knowledge, consent, or understanding. Prototype and field debugging will become more of a challenge as well, since the same apparent supply circuit may have different performance and waveforms. Will such field updates become a common, accepted practice? To me, these downsides can be a nasty side of a good thing. After all, if you can't count on your power supply being anything if not consistent and repeatable, what can you count on?

"What's your view on supplies going digital? Do you welcome it, fear it, or perhaps both?"

pulse

Tektronix takes 802.11 WLAN test solutions to full 165-MHz bandwidth

Tektronix has announced upgrades to its mixed domain oscilloscopes, performance oscilloscopes, spectrum analysers and analysis software with the aim of addressing a number of key aspects of testing wireless LAN integration in embedded systems.

In introducing the new features, Tek says that many companies are offering 802.11ac testing – but at 80-MHz bandwidth: increasing demands for over-the-air bandwidth reflect directly on the capabilities needed of T&M hardware and software. Tek sees differing requirements in test of the RFICs that form the basis of the WLA designs; in the design of modules; and in the challenges facing embedded systems designers who can assume that the chipset is capable of doing its job but need to verify that the full connectivity is working in their design.

To meet these needs, Tek has produced the uprated RSA5000B real-time signal analyser (now claimed to have the widest-available bandwidth); the MDO4000B mixed-domain oscilloscope (positioned as the lowest-cost wideband solution for WiFi measurements)

and SignalVu-PC Software supporting RF Measurements, with in-depth analysis software for complex RF signals and support for Wi-Fi 802.11a/b/g/j/n/p/ac tests.

The RSA5000B real-time signal analyser now series has up to 165 MHz acquisition bandwidth, expanding measurement capabilities for the 160 MHz bandwidth found in 802.11ac, up from 40 MHz in prior 802.11 versions. The minimum signal duration for 100% Probability of Intercept (POI) by the instrument has improved 33% to 2.8 μ sec. This ensures that brief signals are discovered, triggered on and saved, minimising time-to-intercept in spectrum management applications.

Real-time features that were previously extra-cost options are now standard in RSA5000B instruments, including swept DPX, density trigger, time-qualified triggers and improved minimum signal duration. Spectrum processing rate has increased by 33%, to more than 390,000 spectrums/sec. The 5000B is not a swept spectrum analyser – taking that architecture to such a wide bandwidth would be very challenging, Tek says – but employs a very fast A/D front end with digital processing. Example specifications for the RSA5126B variant include frequency

range of 1 Hz to 26.5 GHz; EVM (preliminary) for 802.11ac 160 MHz of -42 dB; internal preamp to 26.5 GHz; and bandwidth up to 165 MHz. Features in the core set of spectrum analysis capabilities include characterisation of pulsed signals.

More aimed at the designer of embedded systems with connectivity, Tek has also uprated the spectrum analysis performance of its mixed domain oscilloscopes (MDOs.) The MDO4000B Series, used with SignalVu-PC, now offers the widest-available bandwidth vector signal analyser for advanced modulation analysis. You can view it, Tek adds, as a wideband spectrum

analyser – with scope channels. As an 802.11ac test solution, it is half the cost of other mid-range offerings, Tek claims, and lists enhancements that include;

- Spurious Free Dynamic Range (SFDR) has improved to 60 dBc guaranteed and 65 dBc typical (from 55/60 typical) giving higher confidence while performing spurious searches.

- Phase noise performance has improved

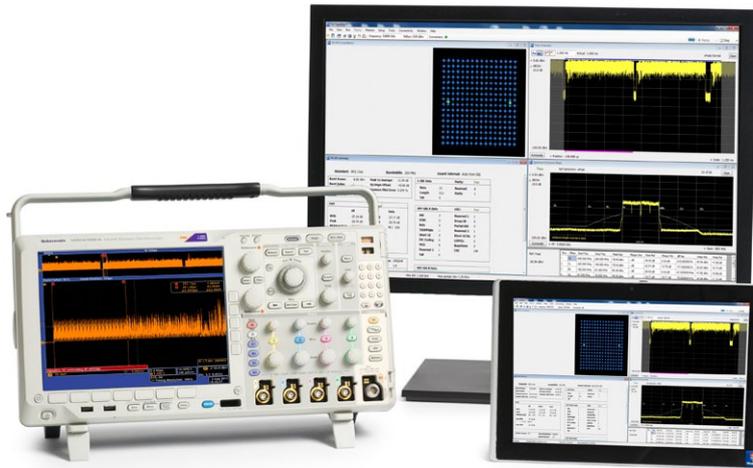
as much as 20 dB enabling close-in spurious measurements and phase noise evaluation.

- Vector calibrated I&Q data enable high-accuracy modulation and vector measurements.

- Maximum RF acquisition time has been doubled from 79 msec to 158 msec enabling longer time correlation with the rest of the system as well as the capture and analysis of multiple bursts of modulated data.

- Lower Frequency Limit has dropped from 50 kHz to 9 kHz enabling EMI diagnostics over the frequency range specified by international regulations.

When used with SignalVu-PC Vector Signal Analysis (VSA) software, the MDO4000B offers a wide bandwidth (≥ 1 GHz) vector signal analyser, making this combination suitable for such RF test and measurement tasks as general modulation analysis, pulse analysis, frequency and phase settling, radar and spectrum management. Prices start at \$12,400.



Tektronix
www.tektronix.com

Arbitrary waveform generators in bandwidths to 160 MHz

Teledyne LeCroy's WaveStation function/arbitrary waveform generators now includes three models with bandwidth up to 160 MHz and 500 Msamples/sec sample rate — over three times more bandwidth and four times more sample rate than the existing models.

These instruments have a larger 4.3-in. colour display, intuitive front panel, two output channels, and PC waveform editing software; they are available with bandwidths of 80 MHz, 120 MHz and 160 MHz, each with 500 Msamples/sec sampling rate, 14-bit resolution and 16 kpts memory per channel. Applications with greater memory needs may access 512 kpts of memory on channel 2, a feature that is standard on all new models.

The front panel provides access to basic waveforms and various operating modes. Users can create basic sine, square, ramp, pulse, and noise waveforms. The display shows all relevant waveform parameters and waveform shapes. High sample rate and high resolution with low jitter and low harmonic distortion ensures precision of the generated waveform. Accompanying the WaveStation hardware is a PC software utility which runs on an external PC and provides additional waveform creation capabilities. Waveforms can be created, shaped and edited with the software using mathematical operators,



digital filters, or by placing individual sample points. The software also provides a flexible waveform drawing tool allowing you to create a freeform waveform sketch on the PC and output it from the WaveStation. The software provides the capability of importing waveforms captured on a WaveAce oscilloscope via USB and recreating them on the WaveStation.

USB and GPIB connectivity enable control of a WaveStation remotely or integration into a test system. All necessary I/O for synchronisation can be accessed on the rear panel. A front panel USB port provides a means of saving waveforms.

Teledyne LeCroy
www.teledynelecroy.com

“LiFi” - a proposal for massive-MIMO visible-light communication networks

National Instruments and the University of Edinburgh are collaborating on work to use LED lighting as a vehicle for local, in-room, broadband download connections. National Instruments (NI) and Professor Harald Haas, lead researcher at the University of Edinburgh have described development of a test bed that aims to dramatically improve indoor wireless communications capacity. The project is a massive multiple input, multiple output (MIMO) technique, referred to as spatial modulation, that potentially provides a highly energy-efficient capacity increase in another step on the path toward fifth-generation (5G) wireless communications.

Haas and Professor Cheng-Xiang Wang, head of the Advanced Wireless Technologies Lab at Heriot-Watt University, recently used NI PXI Express hardware and NI LabVIEW system design software to create the first working prototype showing spatial modulation techniques over a wireless RF channel. In 2011, Haas demonstrated a concept, nicknamed LiFi, using visible light communication over a single-channel, point-to-point link. He now plans to combine these technologies to create even higher density optical wireless networks—called optical attocell networks—that will harness massive MIMO gains in both the optical and RF domains for energy-efficient indoor wireless communications.

“We’ve known for a long time that decreasing cell size can significantly increase cellular capacity and user data rates, but it’s not been clear how we could facilitate that given current spectrum, energy and interference limitations,” said Haas. “RF wireless and optical wireless networks that work together using spatial modulation and massive MIMO approaches could allow us to effectively

mitigate interference and significantly increase energy efficiency, coverage and capacity using existing infrastructure.”

The Edinburgh team is extending its research capabilities with the LabVIEW reconfigurable I/O (RIO) architecture for rapid prototyping. Using the NI FlexRIO Software Defined Radio Bundle with reconfigurable FPGAs and interchangeable I/O adapter modules, the team is building prototypes that operate beyond the rates of a commercial RF wireless system. The team recently achieved 3.5 Gbit/sec from a single colour LED, allowing them to create an ultra-realistic test bed.

Prof. Haas says that the energy-efficiency factor is hard to quantify, since he proposes using LEDs that will be powered for room illumination in any case. Today’s lighting LEDs are mostly blue-emitters that energise broad-spectrum phosphors – his results of 3.5 Gbit/sec are achieved with a selective blue filter to capture the blue component from the LED emitter, and using OFDM at up to 64 QAM – using OFDM provides the expected (and needed) multipath immunity, he says. Today’s sensing and detection devices already offer more-than-adequate performance for such a system, Haas has found. If the lighting is implemented with RGB emitters, then potentially, and with optical filtering, his results could be multiplied on a per-colour basis. Asked about the back-channel, Haas comments, “We’re not proposing abandoning RF entirely; [with future mobile devices] as now, the uplink bandwidth requirement will be much less than the downlink.”

National Instruments
www.ni.com

ScopeCorders extend measurement range with real-time power analysis

Yokogawa has added processing power and algorithms to its ScopeCorder product line to add a suite of real-time calculations, particularly centred around power measurements. Also extended in the new instrument release is the ability for the portable data acquisition recorders to capture and analyse transient events and trends for up to 200 days in power, mechatronics and transportation applications.

The two new instruments in the family of portable multi-channel data-acquisition recorders are the DL850E and DL850EV (Vehicle Edition) ScopeCorders. Introducing the instruments. The company's Product Marketing Manager Kelvin Hagebeuk acknowledges that this instrument format is one in which Yokogawa stands almost alone; and the main competition to the functions it provides is likely to be a PC-based configuration involving data acquisition cards in a rack-mount format. In contrast, he emphasises, the ScopeCorder product is ready to gather data out-of-the-box; "you don't have to program it".

All members of the ScopeCorder family are equipped with a set of basic arithmetic mathematical functions such as addition, subtraction, division, multiplication, fast Fourier transformation and other computations, but the new DL850E versions also offer the /G5 option for real-time measurement of electrical power as well as the existing /G3 option for real-time mathematical computations and digital filtering and the /G2 option for user-defined computations. With the /G5 electrical power option, trend calculations such as active power, power factor, integrated power and harmonics can be carried out at data update rates up to 100 ksamples/sec using a dedicated digital signal processor (DSP)



that is able to calculate and display up to 126 types of electrical power related parameters in real time. The DL850E combines features from a high-performance digital oscilloscope and a multi-channel data-acquisition recorder. It can capture and analyse both transient events and trends over time periods from milliseconds up to 200 days, storing acquired data in the large acquisition memory, the internal hard disk and/or an external PC hard disk. Maximum sample rate is 100 Msamples/sec, and real-time bandwidth, around 20MHz.

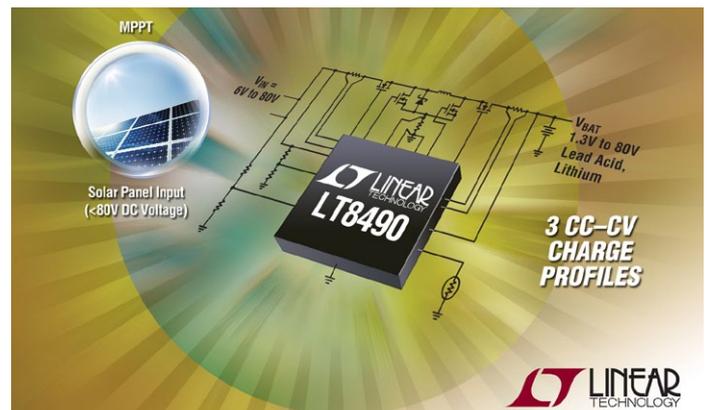
Flexible modular inputs enable the DL850E to combine measurements of electrical signals, physical parameters from sensors, and data from CAN/LIN serial buses – with decode facilities. A choice of 17 input modules allows the instrument to be configured up to a maximum of 128 channels, giving engineers a thorough insight into any application by synchronising the measurement of different types of electrical and physical signals. Individually isolated and shielded input channels provide high resolution and high sample rates, while Yokogawa's unique "dual capture" feature allows transient signals to be captured during long-term measurements by recording at two different sampling rates.

Data is always time-stamped, from an internal clock if the instruments are running stand-alone. An option adds GPS time synchronisation so that the time-stamps on separate instruments are correlated to within 200 nsec; Yokogawa provides software so that you can re-assemble the records from several such instruments and data collections into one display.

A more detailed version of this item is here, or; **Yokogawa** www.tmi.yokogawa.com

IC optimises PV charging up to 80V, handles multiple battery types

An 80V buck-boost lead acid and lithium battery charging controller actively finds the true maximum power point in solar applications; LT8490 is a synchronous buck-boost battery charging controller for lead acid and lithium batteries, featuring automatic maximum power point tracking (MPPT) and temperature compensation. The device operates from input voltages above, below or equal to the regulated battery float voltage. PV panels deliver a variable voltage depending on both the level of illumination they receive, and the pattern (light/shade) they experience – as a source they have variable voltage, current and impedance. Maximum power transfer to a load depends on matching source to load at any instant; the 8490 scans the V/I operating band of the PV panel to find this exact point.



The LT8490's full-featured battery charger offers multiple selectable constant-current constant-voltage (CC-CV) charging profiles, suiting it for charging a variety of lithium or lead acid chemistry types, including sealed lead acid, gel cells and flooded cells. All charge termination algorithms are provided onboard, eliminating the need for software or firmware. The LT8490 operates over a wide 6V to 80V input voltage range and can produce a 1.3V to 80V battery float voltage output using a single inductor with 4-switch synchronous rectification. The device is capable of charging currents as high as 10A depending on the choice of external FETs. The LT8490's MPPT circuit enables a sweep of the full operating range of a solar panel,

finding the true maximum power point, even in the presence of local maxima points caused by partial shading of the panel. Once the true maximum power point is found, the LT8490 will operate at that point while using a dithering technique to quickly track changes in the local maximum power point. With this methodology, the LT8490 fully exploits the power generated by a solar panel, even in non ideal operating environments. The LT8490 costs \$10.35 (1,000).

A longer version of this item is here, or;
Linear Technology
www.linear.com/product/LT8490

More dsPICs for appliance, automotive and industrial applications

dsPIC33EP512GM710 is a family of digital signal controllers from Microchip that enable dual motor control, dual CAN communication and advanced sensor interfaces. Six PWM pairs efficiently control two BLDC or PMSM 3-phase motors with a single DSC; the family implements a CAN communication bridge for systems with multiple CAN buses, and integrated precision analogue enables advanced sensor designs. This is an expansion of Microchip's dsPIC DSC portfolio that adds



higher levels of integration for motor-control applications. The new family of DSCs enables dual motor control with 12 motor-control PWM channels (6 pairs), dual 12-bit ADCs, multiple 32-bit quadrature encoder interfaces, and two CAN modules. With this level of integration, the dsPIC33EP512GM710 family can independently control two motors with a single MCU for optimised system costs. This family can also serve as a communication hub for automotive or industrial applications to connect with multiple CAN buses.

This family expands the existing dsPIC33EP families by providing 512 KB Flash, 48 KB RAM, and four op amps. Other features of this family include enhanced analogue functionality with two independent ADC modules, configurable as 10-bit 1.1 Msamples/sec with four sample and holds, or 12-bit, 500 ksamples/sec with one sample and hold, supporting up to 49 channels. This analogue integration enables advanced sensor applications that require multiple precision ADCs with several sample-and-holds as well as the processing power of a DSP. The dsPIC33EP512GM710 family also includes a Peripheral Trigger Generator (PTG) for scheduling complex, high-speed peripheral operations which saves software cycles and reduces firmware complexity.

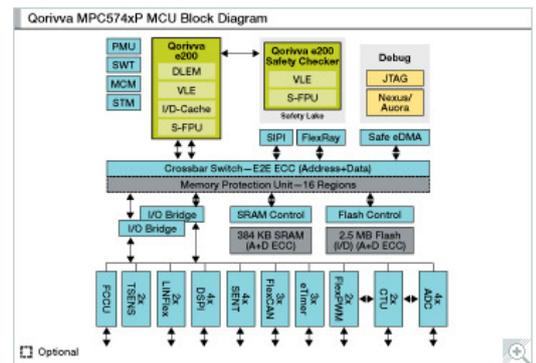
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Microchip
www.microchip.com/get/V37V

Freescale and MicroSys cooperate on industrial functional safety

Freescale Semiconductor and embedded system solutions provider MicroSys Electronics GmbH are collaborating to establish an integrated development platform for functional safety. The SafeAssure kit, developed by MicroSys (miriac-EK5744), is engineered to speed and simplify the creation of industrial equipment required to meet functional safety standards.

The highly-integrated kit is designed to reduce component redundancies, lower bill of material costs and speed development for systems engineers targeting industrial safety applications. The kit provides



an optimised platform for evaluating, designing and prototyping applications which must meet safety standards such as the European Commission's 2006/42/EC Machinery Directive, the IEC 61508 (2010) and 62061 (2005) safety standards, as well as the ISO 13849 (2008) standard. MicroSys and Freescale are additionally working with international certifying organization TÜV SÜD on a concept assessment of the miriac-EK5744 kit.

The kit integrates Freescale's 32-bit Qorivva MPC5744P microcontroller (MCU) and the MC33907 system power management IC with physical transceivers. These Freescale components are part of the Freescale SafeAssure program, which offers a broad solution set of MCUs, sensors and analogue ICs, as well as support for functional safety application design that includes training, safety documentation and technical support.

According to Dieter Pfeiffer, CEO of MicroSys Electronics GmbH, "Other safety kits require more board components to deliver the functionality required to meet today's demanding safety standards, but Freescale's Qorivva MPC5744P integrates advanced dual lock-step cores, together with many other integrated safety features, allowing for a single-MCU based development platform that delivers the performance and functionality that industrial customers demand from next-generation equipment."

Freescale
www.freescale.com/SafeAssure
MicroSys Electronics
www.microsys.de/

Isolated high-side switch for industrial automation designs

STMicroelectronics has introduced an octal high-side switch featuring integrated galvanic isolation. Employing an RF communication technique through the isolation layer of ISO8200B ensures excellent levels of immunity to electromagnetic noise, in compliance with international standards and performing better than integrated devices featuring transformers. As an integrated galvanic isolated switch, ST's ISO8200B fulfils mandatory safety requirements and saves the space normally occupied by conventional opto-electronic isolation circuitry while also enhancing reliability. Energy-saving design ensures very low levels of quiescent current, thus reducing power dissipation by more than 10% compared to traditional, opto-coupler based solution. It is, ST says, the first galvanic-isolation high-side switch with pure RF communication, enabling savings in board space and power, with improved noise immunity. Pricing is from \$3.50 (1000).



A more detailed version of this item is here, or;
STMicroelectronics
www.st.com

Off-line LED drivers optimised for European lighting markets

Power Integrations has added to its LYTSwitch-4 LED-driver IC family, with parts optimised for high-line applications (high-line, i.e. for an input voltage range of 185 VAC to 265 VAC as opposed to the the low-line input voltage range of 90 VAC to 132 VAC.) The parts deliver accurate output current and high efficiency for bulb and tube applications and high-bay lighting; lamps deliver uniform light output and provide good performance in TRIAC-dimmable applications. PI's Andy Smith comments that, "TRIAC dimmers aren't going away: we have to provide good performance when LED lighting is used with them." LYTSwitch-4 ICs feature a combined PFC and CC single-stage converter topology resulting in a power factor greater than 0.95 and efficiencies of over 90% in typical applications. Designs based on the new drivers meet EN61000-3-2C regulations for total harmonic distortion (THD); optimised designs deliver less than 10% THD. Regulation is better than $\pm 5\%$, overall, across load and production spread, reducing the need for over-design to meet minimum luminance targets, cutting system cost. The devices' high switching frequency (132 kHz) enables smaller, lower-cost magnetics to be used, and frequency dithering

reduces EMI filtering requirements. These factors enable LED-driver designs to fit easily into space-restricted bulb styles. Power Integrations adds that, used with leading-edge and trailing-edge TRIAC dimmers, and at low conduction angles, designs comply with NEMA SSL-7. Start-up is very fast, typically less than 500 msec, even when dimmed to less than 10% light output, and "pop-on" is virtually eliminated. You can evaluate the LYTSwitch-4 LED-driver IC family using a new high-line LED lighting reference design that has been co-developed with Cree. DER-396 describes a PAR38 spotlight LED driver design. These documents and all other similar reference designs with Cree are hosted at <http://www.powerint.com/ledrivers/cree>

High-line LYTSwitch-4 ICs come in eSIP-7C (E) and eSIP-7F (L) packages, priced from \$0.58 (non-dimming) to \$0.62 (dimming) (10,000). Reference designs are downloadable at www.powerint.com/en/design-support/reference-designs/design-examples

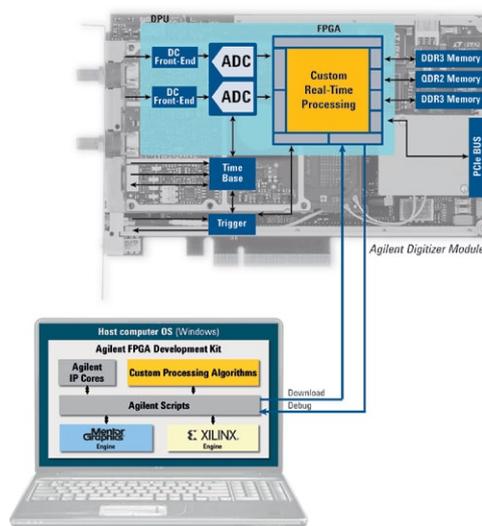
Power Integrations
www.powerint.com/products/lytswitch-family/lytswitch-4

PCI Express high-speed digitiser extends signal-processing features

Agilent has added to its high-speed digitisers with PCIe models supporting custom on-board signal processing capability; the U5309A 8-bit PCIe digitiser samples at up to 2 Gsamples/sec. Previously, Agilent announced the U5303A 12-bit PCIe high-speed digitiser and the U5340A FPGA development kit to address the needs of OEM applications such as analytical time-of-flight, LIDAR ranging, pulsed radar and ultrasonic imaging.

The U5309A high-speed digitiser has two channels with an analogue bandwidth from DC to 500 MHz, a large DDR3 memory for long acquisition time, and a very high data throughput with its PCIe 2.0 eight-lane interface. In addition, the U5309A includes a Xilinx Virtex-6 FPGA, which allows users to load custom real-time signal processing algorithms created with the U5340A FPGA development kit software.

The PCIe high-speed digitiser focuses on interoperability, reusability and upgradability. The software driver provided for both the U5303A and the new U5309A supports multiple programmable interfaces for easy integration of the data converter into existing environments.



Agilent
www.agilent.com/find/U5309A

Secure microcontrollers to protect data in cloud-based transactions

Inside Secure and Intrinsic-ID have announced a new class of secure microcontrollers for smart cards, and other applications that apply Hardware Intrinsic Security (HIS), to provide the highest levels of security for cloud-based transactions. By combining Inside Secure's secure microcontroller designs with patented HIS technology from Intrinsic-ID, the companies will use the unique physical characteristics of each chip to protect cryptographic keys, and thus make the devices extremely hard to clone or reverse engineer.

The Intrinsic-ID HIS technology built into a device such as a secure microcontroller uses physically-unclonable functions

(PUFs) to generate cryptographic keys that do not depend on a value having to be stored in memory. Keys are generated at power-up, or on demand; no key material is present at rest, therefore a very high security level can be achieved. The HIS-based microcontroller chips will be packaged in multiple formats, with the first being a USB smart card token to support the Intrinsic-ID Saturnus secure cloud application.

A longer version of this item is here, or;
Intrinsic-ID
www.intrinsic-id.com

Safety package specific to STM32 microcontrollers in development

ST has signed an agreement with Yogitech to develop a comprehensive safety package for STM32 microcontrollers; the joint effort aims to speed up time-to-market for critical safety applications in industrial- and factory-automation markets. ST and Yogitech have agreed to develop a safety manual and software test libraries as a simple, quick, and effective means of detecting and flagging potentially

dangerous failures in STM32 designs using tailored development tools from IAR Systems.

"The complexity of modern integrated circuits is such that the adoption of a black-box approach for safety analysis is no longer an option," said Silvano Motto, CEO of Yogitech. "The development of the STM32 safety package takes advantage of fRM methodology, our patented white-box approach to address functional safety analyses of integrated circuits approved by TÜV SÜD and by many lead companies in multiple application domains like industrial and automotive."

A longer version of this item is here, or;
STMicroelectronics
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Yogitech
www.yogitech.com

MEASURE AND REDUCE IMD FROM SPECTRUM ANALYSER/DUT INTERACTIONS

Intermodulation (IM) distortion is typically caused by active elements within the communication system. It can be measured and corrected using several techniques. As is the case in many precise measurement situations, however, care must be taken to avoid having the measuring instrument contribute to IM effects. This article describes the interaction between IM products generated by a device under test (DUT) and IM products generated internally in a spectrum analyser.

Reducing intermodulation distortion in advanced communication systems is critical to optimising the system's efficiency and signal quality. IM can increase the occupied bandwidth, cause interference in adjacent channels, add signal distortions, and increase spectrum usage.

IM contributions of the spectrum analyser can make measurements of the overall intermodulation distortion either too optimistic or pessimistic. This article presents examples demonstrating cancellation of IM products and the steps necessary to avoid any influence of the spectrum analyser on the measurement results.

INTERMODULATION DISTORTION

Intermodulation products of 3rd order created by nonlinearities in a device such as a power amplifier are major contributors to performance degradation in a communication system. This is true for in-band intermodulation (for example, with multi-carrier OFDM systems where the transmit signal is degraded) as well as for out-of-band intermodulation where the adjacent channels are affected (measured as Adjacent Channel Leakage Ratio, ACLR).

In-band IM distortion leads to a degraded signal quality in terms of, for example, modulation accuracy measured by the error vector magnitude (EVM). In a transmitter, the output amplifier is most frequently responsible for the intermodulation performance, as it handles the highest power in the transmit signal path. Active devices ahead of the power amplifier can, however, also contribute to the IM performance if not carefully designed.

If two active devices in a signal path generate intermodulation products with approximately the same amplitudes, the resulting IM is dependent on the phase relationship of the individual IM products. The individual IM products may add up leading to an increased IM distortion or subtract each other leading to a cancellation of IM distortion.

When measuring intermodulation products with a spectrum analyser, effects similar to those created by cascaded active devices can occur. This is because a spectrum analyser includes non-linear devices such as the input mixer or a pre-amplifier and therefore generates its own IM products. These distortions can have amplitudes similar to the IM products generated by the DUT. Depending on the phase relationship between the IM products of the DUT and spectrum analyser, the overall IM distortion can be higher (in-phase IM products) or lower (opposite phase IM products) than the DUT's actual IM distortion. Both cases lead to unwanted measurement distortions and must be avoided.

Spectrum analysers use mechanical step attenuators behind

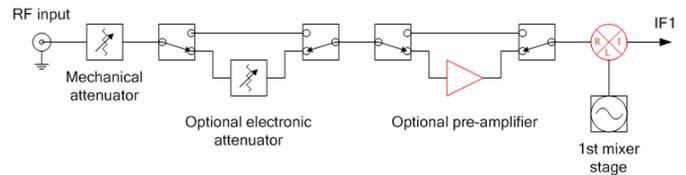


Figure 1. Typical RF front-end of a spectrum analyser. Components highlighted in red can generate IM products.

the RF input connectors to adjust the level at the input of non-linear devices like the first mixer (Figure 1). By tuning the level at the first mixer appropriately, IM distortion can be avoided. Even if a pre-amplifier is used, the main contributor to IM distortion is normally the input mixer – but all semiconductor components following the step-attenuator can contribute to IM distortion.

DYNAMIC RANGE

For a given power level of a measurement signal, several factors limit the dynamic range of a spectrum analyser:

- The inherent noise floor PN of the spectrum analyser for lower power levels
- The compression of the input mixer for high power levels
- The phase noise for small signals close to a high level carrier

When multiple tones are applied to the spectrum analyzer, IM products can limit the dynamic range.

3rd order intermodulation, in particular, must be considered because they result in the highest IM products. Spectrum analyser data sheets provide a specification for two-tone IM distortion with the so called Third Order Intercept point (T.O.I.), measured with a two-carrier CW signal. The T.O.I. is the theoretical power level that would generate 3rd order IM products having the same level as the applied CW signals. It can be calculated [Reference 1] as;

$$TOI = P_{in} + P_{\Delta} / 2 \quad (1)$$

where TOI is the Third Order Intercept point in dBm, P_{in} is the level of each two-tone input signal in dBm and P_{Δ} is the

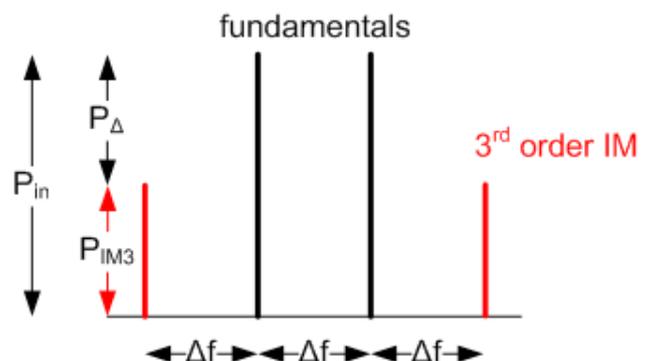


Figure 2. Schematic diagram of 3rd order IM components and relevant parameters.

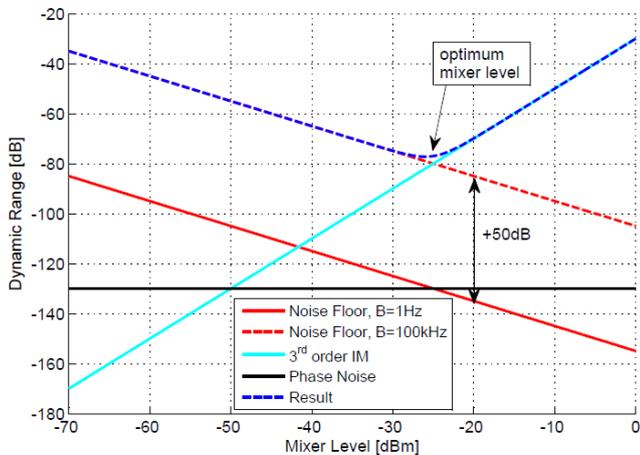


Figure 3. Dynamic Range Chart with noise floor increase due to a wideband signal. TOI = 15 dBm, DANL = -155 dBm/Hz, Phase Noise = -130 dBc.

amplitude of the IM products relative to P_{in} (see Figure 2).

Due to compression occurring when operating an active device in the non-linear range, the T.O.I. level cannot be attained in a real measurement (e.g. at an output of an amplifier). It is, however, a good figure of merit to calculate the intermodulation free dynamic range P_{Δ} :

$$P_{\Delta} = 2(TOI - P_{in}) \quad (2)$$

The amplitude PIM3 of the 3rd order IM products is accordingly

$$\begin{aligned} P_{IM3} &= P_{in} - P_{\Delta} \\ &= P_{in} - 2(TOI - P_{in}) \\ &= 3P_{in} - 2TOI \end{aligned} \quad (3)$$

Another factor limiting dynamic range, especially for low input powers, is the spectrum analyser's noise floor. Data sheets specify this as the Displayed Average Noise Floor (DANL).

Summing the distortions yields the so-called dynamic range chart shown in Figure 3. For low-input power levels, the noise floor limits the dynamic range. For higher levels, the limiting factor is 3rd order IM distortion.

2nd order IM distortions and phase noise also influence the dynamic range. 2nd order IM is not considered further in this article because the distortion products fall at frequencies far from the signal ($f_1 + f_2$ and $f_2 - f_1$) and are therefore not relevant for in-band distortion and ACLR. Summing all distortion sources in the linear domain gives the actual dynamic range for a spectrum analyser. The minimum of this curve is called the optimum mixer level. At this point, the spectrum analyser achieves the maximum dynamic range. By using the preamplifier and step attenuator, the mixer level for a given input signal can be set to this optimal value.

For real measurements, the increase in noise floor due to a wide signal bandwidth must be taken into account. Filter settings are not of importance for the analyser's first mixer because this mixer always sees the full bandwidth and therefore only the

signal bandwidth is relevant. The bandwidth dependent noise floor relative to the mixer level is given [Reference 1] as;

$$P_N = [DANL + B - P_{in}] dB \quad (4)$$

with B as the bandwidth of the signal in dB. As a result, the dynamic range decreases and the optimum mixer level shifts to the right. Figure 3 shows an example with B = 100 kHz (50 dB).

TWO-TONE EXAMPLE

A two-tone measurement can be used to demonstrate the interaction of IM products of a DUT and spectrum analyser. Here CW signals of two generators are combined and fed into the DUT and the resulting 3rd order IM products are measured by a spectrum analyser. Consider two tones at frequencies f_1 and f_2 of equal amplitude and uncorrelated phase, separated Δf apart. They will produce 3rd order IM products at $f_1 - \Delta f$ and $f_2 + \Delta f$.

P_{Δ} is used to characterise the amount of IM distortion. Figure 4 shows a block diagram of the measurement setup.

In the following example the fundamentals are centred around 5.2 GHz ($\Delta f = 312.5$ kHz) and have a signal level of -6 dBm each.

The first step is to focus solely on the IM products of the spectrum analyser (path 1 in Figure 4). In other words, there is no DUT in the signal path. All IM products observed in the analyser display are generated by the first mixer of the spectrum analyser. To verify whether the observed IM products are generated by the spectrum analyser, the amount of input attenuation can be varied. This also alters the input power to the first mixer. If the displayed IM products are a result of the analyser's first mixer, an increase of input attenuation will decrease the IM products' amplitude by a factor of two, since the mixer is then operating in a more linear range. Figure 5a shows a measurement on an R&S FSQ26 spectrum analyser.

In the next step, the DUT (wideband power amplifier) is inserted into the signal path (path 2 in Figure 4). Now the DUT and spectrum analyser will both generate IM products that will interact within the spectrum analyser. The resultant signals are displayed in Figure 5b. The input power to the spectrum analyser is kept at the same level as in the previous measurement. If the input attenuation is increased in this setup, the IM products now also increase as opposed to the previous measurement, where they decreased. This behaviour is due to the IM products cancelling each other because the IM products of DUT and analyser are of opposite phase. If the input attenuation is increased, the spectrum analyser contributes less IM products and the cancellation effect is reduced.

The strength of this effect depends on the combination of

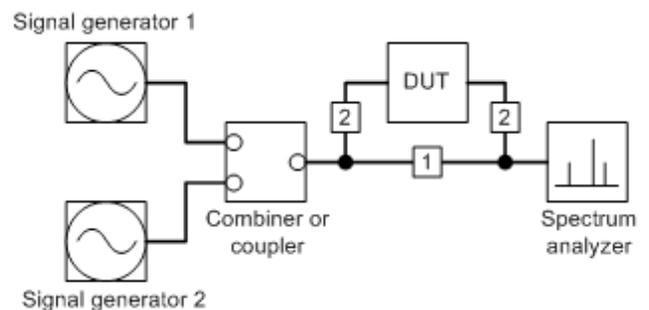


Figure 4. Measurement Setup without (path 1) and with DUT (path 2).

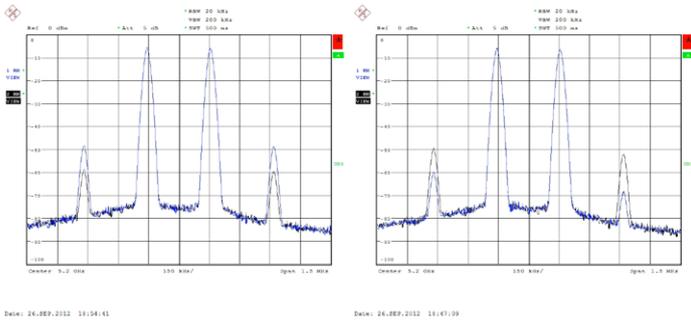


Figure 5a. Result of a two-tone measurement without DUT. An increase of input attenuation results in a decrease of IM products. Blue trace: 0 dB input attenuation, black trace: 5 dB input attenuation.

Figure 5b. Measurement with DUT. IM cancellation occurs. An increase of input attenuation also increases IM products since IM cancellation is reduced. Blue trace: 0 dB input attenuation, black trace: 5 dB input attenuation.

DUT and spectrum analyser and the specific phase relation of their IM products. A test with a different type of DUT or spectrum analyser could easily result in constructive IM interference. In this case, the behaviour illustrated in Figure 5a would be observed.

The IM products contributed by the spectrum analyser will decrease with additional attenuation until only the DUT's IM products remain. In any case, a contribution of the spectrum analyser to the IM products must be avoided to obtain correct measurements.

The cancellation effect is frequency dependent due to the changing phase relation with frequency. Therefore, the same setup can show varying degrees of IM cancellation, depending on frequency.

Cancelling IM products lead to measurement results that are too optimistic. On the other hand, IM products that interfere constructively result in measurements that are too pessimistic. This is true for measurements characterising the DUT's IM distortion as shown in Figure 5b above and also for (ACLR) and modulation accuracy. An example for an EVM measurement is given in the next section.

OFDM MEASUREMENTS

This example shows the effect of IM distortion on modulation accuracy (EVM). In an OFDM signal, all subcarriers are separated by Δf . IM products created by any pair of subcarriers will occur at subcarriers left and right of the pair. Thus signal quality in an OFDM system is strongly influenced by IM distortion.

A signal with a structure as shown in Figure 6 can be used to demonstrate this effect. Two carriers with QPSK modulation are followed by two unused carriers. This structure is repeated several times. IM products will fall at the frequencies of the unused carriers left and right of the pair. By analysing the constellation diagram of the unused carriers, signal distortion due to IM products can be determined. IM phase – which determines whether constructive or destructive IM interference occurs – can easily be visualised.

The expected data points of the unused carriers lie in the origin of the constellation diagram. IM distortion will shift these points beyond the origin. In a real OFDM system, unused carriers would not be analysed. But for demonstration purposes, this procedure easily shows the effects of IM cancellation and an EVM value that is too optimistic.

Figure 7 shows the constellation diagram of an unused car-

rier for three measurement setups. First a measurement without DUT (i.e. the signal path 1 in Figure 4) and 0 dB input attenuation is shown (magenta).

Here the shifted symbols are a result of the R&S FSQ26's IM products. Next the DUT is put back into the setup (signal path 2) and 5 dB input attenuation is used (blue) so that the spectrum analyser doesn't contribute to the IM distortion. This way only the IM products from the DUT influence the result.

In the last step, the input attenuation is reduced to 0 dB (red) and the IM products of the DUT and analyser interact with each other. Due to the fact that they have opposite phases, the IM products interfere destructively and cancellation occurs (compare with 5b). The symbols are shifted closer to the ideal symbol at the origin resulting in a significantly reduced EVM. In this situation, the modulation accuracy of the DUT would therefore be overestimated.

ESTIMATING IM DISTORTION

The chance of IM cancellation or amplification is inevitable if the DUT and spectrum analyser both have a similar T.O.I. The DUT's true amplitude P_{Δ} will be distorted by the analyser's contribution. It is the engineer's task to determine the amount of input attenuation to use in order to reduce the error caused by the analyser's IM contribution to a desired level.

In the previous examples, the measured T.O.I. of the R&S FSQ26 is 15 dBm and of the DUT 10 dBm. Equation (2) can be used to calculate the amplitudes of the IM products P_{Δ} . Taking as an example an input amplitude of -10 dBm, the R&S FSQ26 generates IM products with $P_{\Delta,SA} = 50$ dB (T.O.I.=15 dBm) and the DUT has $P_{\Delta,DUT} = 40$ dB (T.O.I.= 10 dBm). An IM product of the spectrum analyser that is only 10 dB below the DUT's IM products is enough to lead to significant interference – either constructive or destructive – depending on the phase relation.

When the analyser's and DUT's IM products interfere, the resulting amplitude error is given by

$$e_A = 20 \log \left(1 \pm 10^{\frac{d}{20}} \right) \text{dB} \quad (5)$$

where d is the negative amplitude difference between the IM products of the analyser and DUT in dB, -10 dB in the above example (see Figure 8). For in-phase IM products, the elements in equation (5) within brackets are added. For opposite phase products they are subtracted. Referring to the above example, the calculation becomes (IM cancellation due to opposite phases assumed):

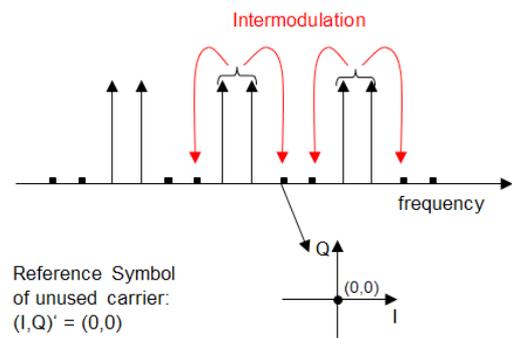


Figure 6. OFDM carrier structure with alternating pairs of active and inactive carriers. Red arrows indicate the position of the resultant IM products.

$$e_A = 20 \log\left(1 - 10^{-10/20}\right) = -3.3 \text{ dB}$$

meaning that the amplitude of the DUT's IM products are 3.3 dB lower than expected.

To avoid interference, the input power to the analyser's first mixer must be reduced. This is done by adding sufficient input attenuation. Adding e.g. 10 dB attenuation in the above example reduces Pin by 10 dB to -20 dBm and PΔ,SA = 70 dB. PΔ,DUT stays at 40 dB. Now the IM products of the spectrum analyser are 30 dB below the DUT's and the amplitude error is reduced to

$$e_A = 20 \log\left(1 - 10^{-30/20}\right) = -0.3 \text{ dB}$$

An engineer would most likely first define a maximal allowable amplitude error eA for his application and calculate it as

$$\text{IM amplification: } d_{\text{goal}} = 20 \log\left(10^{e_A/20} - 1\right) \text{ dB}$$

$$\text{IM cancellation: } d_{\text{goal}} = 20 \log\left(1 - 10^{e_A/20}\right) \text{ dB}$$

Based on equation (2), PΔ for DUT and analyser can be calculated. If the current amplitude difference dcurr = PΔ,SA - PΔ,DUT is lower than dgoal, the mixer level must also be lowered in order to reduce the analyser's IM products. As a result, the optimum mixer level shifts to a lower value. This can be expressed as an effective T.O.I. that is lowered by d/2

$$TOI_{\text{eff}} = TOI - d_{\text{goal}} / 2 \quad (6)$$

For the example with dgoal = 30 dB, dcurr = 10 dB and TOI = 15 dBm, the effective TOI is 0 dBm. The dynamic range chart (Figure 3) would change accordingly. The amplitude error requirement will shift the 3rd order IM curve up by dgoal and the optimum mixer level will shift to a lower value. A price must be

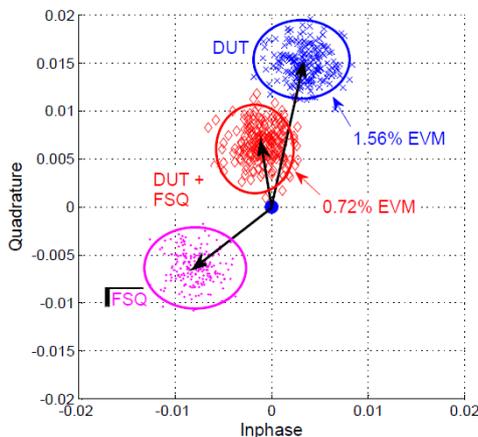


Figure 7. Constellation diagram of an unused carrier showing shifted symbols due to IM distortion for different setups. The reference symbol lies in the centre.

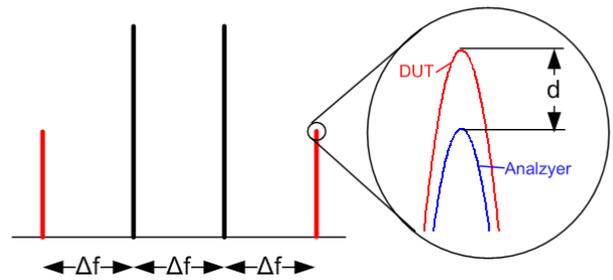


Figure 8. The detailed view shows the difference in IM amplitude between analyser and DUT.

paid for making these adjustments, however, because they also reduce the dynamic range. This obviously makes the dynamic range specification of the spectrum analyser very important. Instruments with a higher dynamic range initially will be better able to accommodate the reduction.

The additional attenuation that needs to be added for reducing the mixer level by the required amount is

$$Att = \frac{1}{2} (d_{\text{goal}} - d_{\text{curr}}) \text{ dB} \quad (7)$$

10 dB in the above example.

CONCLUSION

Interfering IM products of a DUT and spectrum analyser can result in distorted intermodulation measurements, ACLR and modulation accuracy. Care must be taken when IM products of the DUT and analyser are of similar amplitude since this can lead to distorted measurements. Depending on whether constructive or destructive IM interference occurs, the displayed results can either be worse or better than the real DUT performance.

To reduce the analyser's influence on IM distortion, the mixer level must be lowered so that a tolerable error is reached. To do so, additional input attenuation must be used.

To verify for a given measurement setup that the analyser's contribution to the IM distortion is negligible, a two-tone measurement can be used to check for IM cancellation or amplification. This way the amplitude error originating from interfering IM products can be estimated.

The different architectures of spectrum analysers decide upon the propensity of IM distortion. Analysers such as the R&S FSW or R&S FSQ8 are less likely to add IM products to the measurement since they have a considerably higher T.O.I. (typically 20 dBm and 23 dBm, respectively). For these analysers, less input attenuation is required to protect the input mixer, which results in a higher dynamic range.

Reference

- Ref 1. Fundamentals of Spectrum Analysis. C. Rauscher, Rohde & Schwarz, 2001
- Additional reading on www.rohde-schwarz.com:
- Measurement of Harmonics using Spectrum Analyzers. Application Note 1EF78, 2012
- Intermodulation Distortion Measurements on Modern Spectrum Analyzers. Application Note 1EF79, 2012

About the Author

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BY BONNIE BAKER

BAKER'S BEST



Find input and output resistance with IBIS

The I/O buffer information specification, or IBIS, is a simulation system that allows the user to model then simulate signal integrity scenarios before committing the circuit to the printed circuit board (PCB). One sets the modelling scenario by connecting the applicable input and output IC pins of an IBIS model to a PCB signal path model.

Additionally, the IBIS model provides interesting pre-simulation information to the IC user. The IBIS model itself contains this information embedded in the various tables inside the model. This pre-simulation information includes input/output pin impedances and the electrostatic discharge (ESD) cells details. Figure 1 shows the configuration for an I/O (input/output) digital buffer.

For these gates, the IBIS model lists a table of the typical, minimum, and maximum current responses versus voltage input. IBIS modellers use data from the designer's SPICE stack simulations or bench data. For instance, Table 1 shows a truncated example of an IBIS model output gate.

The ads129x.ibs model assigns the DIO_33 and DIO_18 sub-models to the families SCLK and DAISY_IN pins. Both pins have an I/O function. The DIO_33 sub-model uses power supply voltages of 0 and 3.3V. The DIO_18 sub-model uses power supply voltages of 0 and 1.8V.

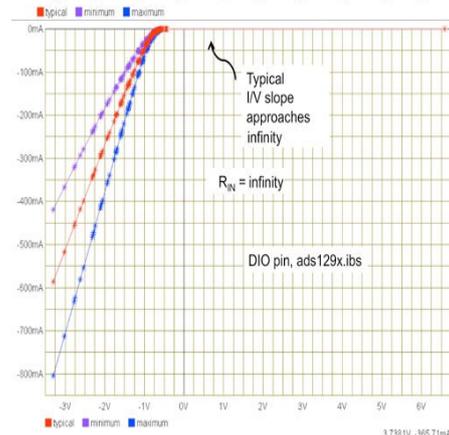
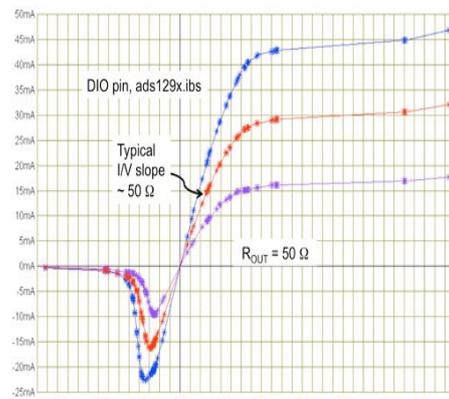
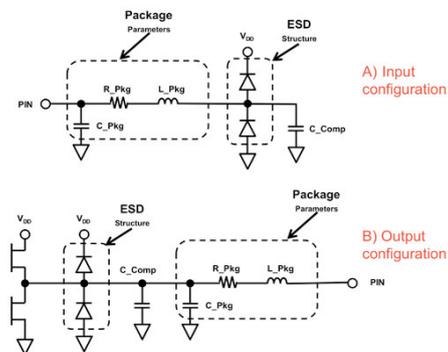
Figure 2 shows a graphical representation of the data in Table 1, the partial listing from the ads129x.ibs IBIS model. The ADS129x is a family of low-power, 8-channel, 24-bit analogue front-end (AFE) for biopotential measurements delta-sigma ADCs. Figure 2 shows the graphical representation of the data in Table 1.

In Figure 2, the output pin traverses from 3.3V below ground up to 3.3V above the power supply voltage. With this excursion, you can see the reaction of the minimum, typical, and maximum output current. A point of interest in this figure is between 0.2V and 1V (typical curve). In this region, the impedance of the gate or the voltage to current relationship equals

50 Ohms. You can find the same relationship with the minimum and maximum curves.

Figure 3 shows an example of the input gate of the same pin. The good news with this input pin representation shows an input impedance of infinity. But this diagram contains more information than the pins reaction in the active range (between 0 and 3.3 V). With an input voltage between -3.3 and 0 volts, there is a good indication of how the ESD cells are operating.

You can download this model (ads129x.ibs) and generate both Figure 1 and Figure 2 by copying the ibis file into excel.



References

- 1 The IBIS model, Part 1: A Conduit into signal integrity analysis, Analog Applications Journal, Texas Instruments, 4Q 2010
- 2 The IBIS model, Part 2: Determining the total quality of an IBIS model, Analog Applications Journal, Texas Instruments, 1Q 2011
- 3 The IBIS model, Part 3: Using IBIS models to investigate signal-integrity issues, Analog Applications Journal, Texas Instruments, 2Q 2011
- 4 Johnson, Graham, High-speed Digital Design: A Handbook of Black Magic, Prentice Hall, ISBN: 0-13-395724-1
- 5 ads129x.ibs, IBIS Model, Texas Instruments
- 6 Baker, Bonnie, Signal integrity and characteristic impedance, EDN, June 23, 2011
- 7 Baker, Bonnie, Beyond the data sheet with IBIS, EDN, May 25, 2011

[Model]	DIO_33			
[Pulldown]				
I	Voltage	I(typ)	I(min)	I(max)
	-3.3	-0.00029	-0.00021	-0.00031
	-1.84587	-0.00076	-0.00051	-0.00088
	-1.82183	-0.00077	-0.00052	-0.00091
	-1.81596	-0.00077	-0.00052	-0.00092
	-1.76483	-0.00089	-0.00053	-0.00102
	-1.52605	-0.00146	-0.00086	-0.00149
	-1.33133	-0.00192	-0.00113	-0.00255
	-1.32453	-0.00193	-0.00114	-0.00261
	-1.318	-0.00195	-0.00115	-0.00268
	-1.26241	-0.00208	-0.00123	-0.00347
	-1.25734	-0.00211	-0.00123	-0.00354
	-1.25238	-0.00214	-0.00124	-0.00361
	-1.23555	-0.0023	-0.00126	-0.00385
	-1.16669	-0.00295	-0.00136	-0.00586

OPTIMISING HIGH-PERFORMANCE CPUS, GPUS AND DSPS? USE LOGIC AND MEMORY IP

Mobile communications, multimedia and consumer systems-on-chip (SoCs) must achieve the highest performance while consuming the minimal amount of energy to achieve longer battery life and/or fit into lower cost packaging. CPUs, GPUs and DSPs typically each have unique performance, power and area targets for each new silicon process node. Each new generation brings a new set of challenges to SoC designers and a new set of opportunities to create higher performance and more power-efficient IP to enable SoC designers to deliver the last megahertz of performance, while squeezing out the last nanowatt of power and last square micron of area. SoC designers need to first be aware of the advances in logic and memory IP and then they must know how to take advantage of these advances for the key components of their chips using the latest EDA flows and tools to stay ahead of their competitors.

In this article we describe available logic library and memory compiler IP and a typical EDA flow for hardening processor cores. The article provides innovative techniques, using those logic libraries and memory compilers within the design flow, to optimise processor area. The article then goes on to describe methods using these same elements for optimising the performance and power consumption of processors. The article finishes with a preview of how the innovation of FinFET technology will affect logic and memory IP and its use in hardening optimal CPU, GPU and DSP cores.

Why Different PPA Goals for CPU, GPU and DSP Cores?
CPU, GPU and DSP cores co-exist in an SoC and are typically optimised to different points along the performance, power and area (PPA) axes (Illustration).

For example, CPUs are typically tuned first for high performance at the lowest possible power while GPUs, because of the relatively large amount of silicon area they occupy, are usually optimised for small area and low power. GPUs can take advantage of parallel algorithms that reduce the operating frequency, but they increase the silicon area—accounting for up to 40% of the logic on an SoC. Depending on the application, a DSP core may be optimised for performance, as in the case of base station applications with many signals, or optimised for area and power for handset applications.

Logic Libraries for High-Performance and Low-Power Core Optimisation

Synthesisable CPU, GPU and DSP cores, today's high-performance standard cell libraries and EDA tools can achieve an optimal solution without having to design a new library for every processor implementation. To optimally harden high-performance core, designers need the following components in a standard cell library:

- Sequential cells
- Combinational cells
- Clock cells
- Power minimization libraries and power optimisation cells for non-critical paths

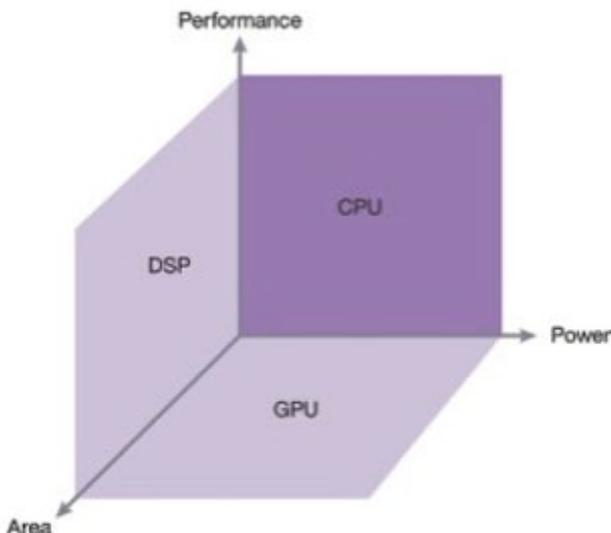
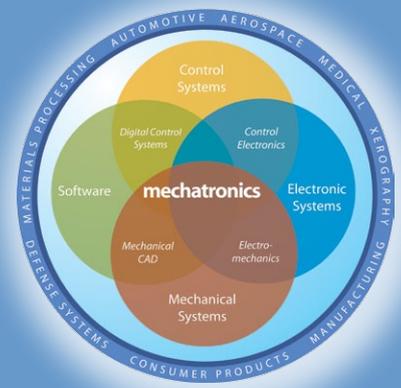


Figure 1: Primary PPA Targets for CPUs, GPUs and DSPs

The article continues with the author considering each of these SoC elements in turn; read the complete article here, at www.edn-europe.com.

MECHATRONICS IN DESIGN

FRESH IDEAS ON INTEGRATING MECHANICAL SYSTEMS, ELECTRONICS, CONTROL SYSTEMS, AND SOFTWARE IN DESIGN



Hydraulic transmission lines

By Kevin Craig

In applications where large forces/torques are required, with a fast response time and high accuracy, hydraulic control systems are essential. They have a more competitive power-weight ratio than electrically-actuated systems, which are limited by magnetic saturation, and they excel in environmentally-difficult applications. In addition, the hydraulic medium is mechanically stiffer than the electromagnetic medium. Self-lubrication and inherent heat transfer are also advantages.

Fluid power applications are numerous, e.g., vehicle steering, braking, and suspension systems; industrial mechanical manipulators and robots; and actuators for aircraft and marine vessels, to name a few. They are all multidisciplinary systems and require a systems approach to design and implement with optimal energy consumption. Hydraulic valves, pumps, motors, cylinders, and accumulators are all routinely modelled and analysed. Often overlooked in a hydraulic control system are the hydraulic transmission lines and failure to model their dynamic effect could lead to poor performance and possible instability.

The hydraulic transmission line is a distributed system. The motion of the fluid in the transient condition takes place under the action of fluid inertia, friction, and compressibility, as well as the driving pressure forces. Fluid velocity, pressure, and temperature vary from point to point along the pipe/hose length and radius, which may itself be compliant. A lumped-parameter model which describes the dynamic behaviour of the transmission line with acceptable accuracy is needed.

It is insightful to use the electric-hydraulic analogy to develop and understand the lumped-parameter model. The effort variables are electric voltage and fluid pressure, while the flow variables are electric current and fluid flow rate. Energy is stored via the effort variables in the electrical capacitor and fluid capacitance. Energy is stored via the flow variables in the electrical inductor and fluid inertia. Energy is dissipated in the electrical and fluid resistance elements. Fluid resistance and fluid inertia are generally well understood. Fluid capacitance is due to the bulk modulus (measure of fluid compressibility) of the fluid, which is reduced by entrained air, and the compliance of the flexible hose. The analogue RLC electrical circuit shown in Figure 1 and

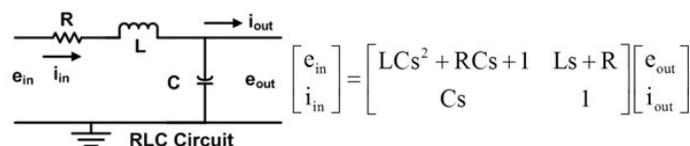


Figure 1 Hydraulic transmission line circuit and input-output matrix

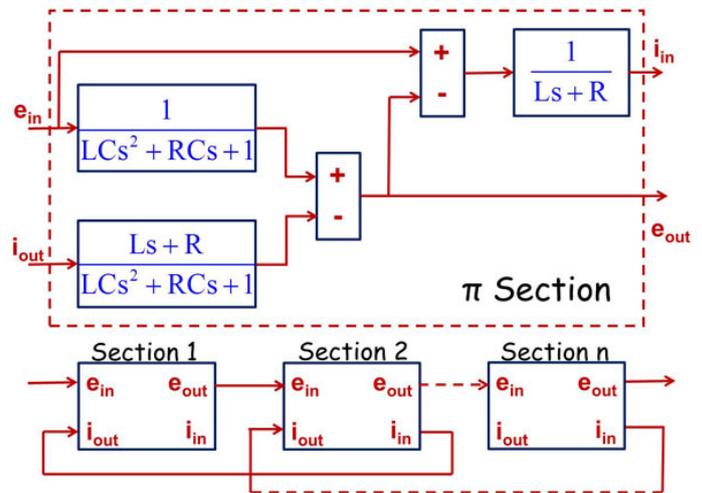


Figure 2 Hydraulic transmission line block diagram

the input-output matrix is derived by applying Kirchhoff's Laws, applicable to both electrical and hydraulic circuits.

A block diagram for one lumped element, called a π section because of its circuit shape, is shown in Figure 2. This applies to both the electrical and hydraulic circuits. This is easily implemented in MatLab/Simulink and gives the same results as obtained using the predefined electrical and hydraulic transmission line blocks in MatLab SimScape. This approach, however, gives more insight and understanding. The greater the number of sections used, the closer the dynamic behaviour prediction is to that obtained from the distributed-parameter model, and more importantly, to the actual system behaviour.

How are the hydraulic resistance, inertia, and capacitance determined for each section of the transmission line? It is common to assume laminar, unidirectional flow using the average pressure and velocity at any cross section and at any instant. The pressure change-flow rate relationship is then linear and algebraic, with the resistance R as the proportionality constant. The lump of fluid in a section can be treated as a rigid body to which we apply Newton's 2nd Law to get the relationship between pressure change and the rate of change of flow rate, with the fluid inertance I , as it is called, as the proportionality constant. The capacitance C of the fluid lump shows the relationship between volume change and pressure change, and is due to the compressibility of the fluid, represented by its bulk modulus, and modified to include the effects of entrained air and flexible hoses.



Solutions from AC to Point of Load

Our Latest Products

Picor Cool-Power Isolated ZVS DC-DC Converters

Simple to Use

- Complete Isolated DC-DC converter with zero-voltage switching module
- Three input voltage ranges for communication, industrial, rugged/M-Grade applications
- Communication converters have max peak input voltage of 100 V / 100 ms (non-operating)
- 2,250 V input to output isolation

High Density

- 50 W / 60 w output power (dependent upon converter model)
- Surface mount 22mm x 16.5mm x 6.7mm high-density package
- 900 kHz switching frequency, minimizes input filtering and reduces output capacitance

Rich Feature Set

- On/Off Control, positive logic ENABLE
- Wide trim range +10/-20% Trim
- Temperature monitor™ & Over-temperature Protection (OTP)
- Input UVLO & OVLO and output OVP
- Over current protection with auto restart
- Adjustable soft-start
- Output voltage sensing without opto coupler use for higher reliability



Cool-Power	Input	Output Set	Output Range	I _{OUT} Max
Communications (-40°C to 125°C)				
PI3101-00-HVIZ	36 – 75 V _{in}	3.3 V	3.0 to 3.6 V	18 A
PI3105-00-HVIZ		12 V	9.6 to 13.2 V	5 A
PI3110-01-HVIZ	41 – 57 V _{in}	18 V	16.2 to 19.8 V	3.3 A
Industrial (-40°C to 125°C)				
PI3109-01-HVIZ	18 – 36 V _{in}	5 V	4.0 to 5.5 V	10 A
PI3106-01-HVIZ		12 V	9.6 to 13.2 V	4.2 A
M-Grade (-55°C to 125°C)				
PI3109-00-HVMZ	16 – 50 V _{in}	5 V	4.0 to 5.5 V	10 A
PI3106-00-HVMZ		12 V	9.6 to 13.2 V	4.2 A
PI3111-00-HVMZ		15 V	12 to 16.5 V	3.3 A

Resources



Blog Post: The technology behind the Cool-Power ZVS DC-DC Converters



Video: An Introduction to Vicor's Cool-Power ZVS DC-DC Converters

Two-Part Web Seminar Series About EMI

Watch Part 1

The Causes and Impact of EMI in Power Systems

Watch Part 2

Practical Design Considerations and Solutions for the Reduction of Conducted EMI and Filter Size in Power Systems

VI Brick AC Front End

Overview

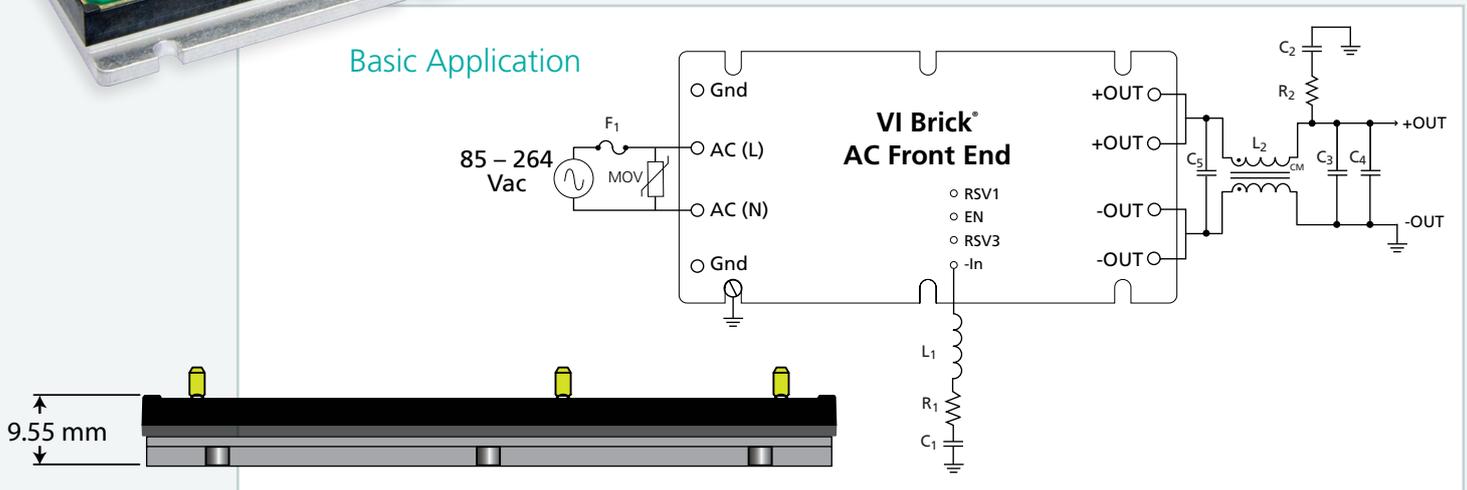
- Universal Input: 85 – 264 Vac
- Output: 48 Vdc - isolated, regulated (SELV)
- Power: 330 W - over entire input voltage range
- Isolated AC-DC converter with active Power Factor Correction (PFC)
- Integrated rectification, filtering and transient protection
- Peak efficiency: >92%
- EN55022, Class B EMI conducted emissions with a few components
- EN61000-3-2 harmonic limits
- -55 to 100°C baseplate operation

Features

- Low profile, 9.55 mm height above board
- Small footprint, size of a business card
- Flanged aluminum package for secure mounting and thermal management
- Consistent high efficiency across the worldwide mains (flat efficiency curve)
- Reduced power loss and cooling requirements
- Module includes PFC, regulation, isolated 48 V output (SELV), filtering, rectification, transient protection, agency approvals, simplified thermal management
- Simple design, requires few external components
- Module power density, 121 W/in³
- Complete solution including hold-up capacitors, 54 W/in³



Basic Application



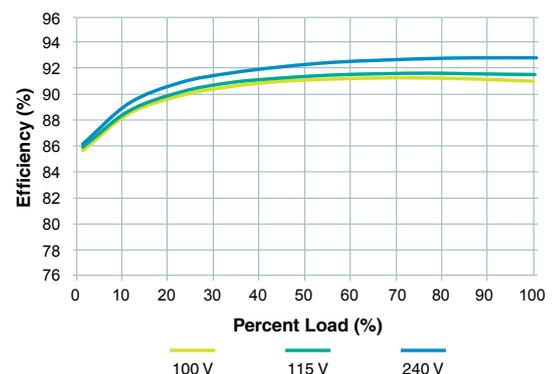
Resources

- [▶ An Introduction to the Vicor AC Front End Module](#)
- [▶ Webinar: Designing High Performance AC-DC Power Systems Using a Power Component Approach](#)
- [▶ AC Front End Product Information](#)

Part Number	Input Voltage	Output Voltage	Output Power	Operating Temperature
FE175D480C033FP-00	85 – 264 Vac	48 Vdc	330 W	-20 to 100°C
FE175D480T033FP-00	85 – 264 Vac	48 Vdc	330 W	-40 to 100°C
FE175D480M033FP-00	85 – 264 Vac	48 Vdc	330 W	-55 to 100°C

Replace the “-00” suffix in the part number with “-CB” to order an evaluation board.

Consistent High Efficiency Over Line, Load, Temperature



Picor Cool-Power ZVS Buck Regulators

Wide Operating Range

- Wide V_{IN} (8 – 36 V) and wide V_{OUT} (1 – 16 V)
- 12 V-optimized performance with PI34xx Series
- 40°C to 125°C operating range

Simple to Use; Fast Development Time

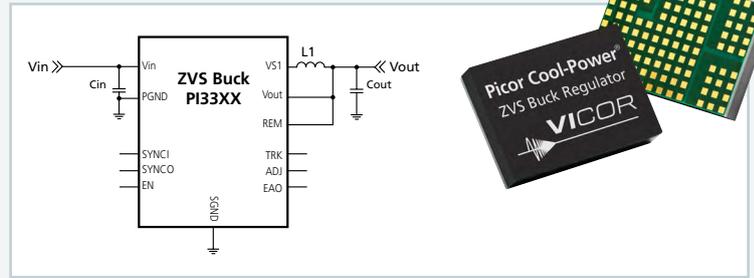
- Internal compensation - few external components
- No additional design or additional settings required

High Efficiency

- Up to 98% peak efficiency (19 V_{IN} to 15 V_{OUT})
- PI34xx Series optimized for 12 V_{IN} with even higher efficiency
- Light and full load high-efficiency performance

Flexible and Rich Feature Set

- Paralleling and single wire current sharing
- Frequency synchronization
- User adjustable soft-start & tracking
- Power-up into pre-biased load
- Optional I²C functionality & programmability



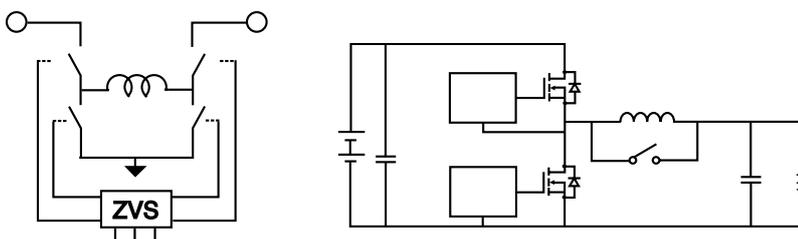
Cool-Power Model Number	Output Range		I_{OUT} Max
	Set	Trim Range	
PI3311-00-LGIZ	1.0 V	1.0 V to 1.4 V	10 A
PI3318-00-LGIZ	1.8 V	1.4 V to 2.0 V	10 A
PI3312-00-LGIZ	2.5 V	2.0 V to 3.1 V	10 A
PI3301-00-LGIZ	3.3 V	2.3 V to 4.1 V	10 A
PI3302-00-LGIZ	5.0 V	3.3 V to 6.5 V	10 A
PI3303-00-LGIZ	12 V	6.5 V to 13.0 V	8 A
PI3305-00-LGIZ	15 V	10.0 V to 16.0 V	8 A
Higher Current Versions			
PI3311-01-LGIZ	1.0 V	1.0 V to 1.4 V	15 A
PI3318-01-LGIZ	1.8 V	1.4 V to 2.0 V	15 A
PI3312-01-LGIZ	2.5 V	2.0 V to 3.1 V	15 A
PI3301-01-LGIZ	3.3 V	2.3 V to 4.1 V	15 A
I²C Functionality and Programmability			
PI3311-20-LGIZ	1.0 V	1.0 V to 1.4 V	10 A
PI3318-20-LGIZ	1.8 V	1.4 V to 2.0 V	10 A
PI3312-20-LGIZ	2.5 V	2.0 V to 3.1 V	10 A
PI3301-20-LGIZ	3.3 V	2.3 V to 4.1 V	10 A
PI3302-20-LGIZ	5.0 V	3.3 V to 6.5 V	10 A
PI3303-20-LGIZ	12 V	6.5 V to 13.0 V	8 A
PI3305-20-LGIZ	15 V	10.0 V to 16.0 V	8 A
PI3311-21-LGIZ	1.0 V	1.0 V to 1.4 V	15 A
PI3318-21-LGIZ	1.8 V	1.4 V to 2.0 V	15 A
PI3312-21-LGIZ	2.5 V	2.0 V to 3.1 V	15 A
PI3301-21-LGIZ	3.3 V	2.3 V to 4.1 V	15 A
12 V Optimized Option			
PI3420-00-LGIZ	1.0 V	1.0 V to 1.4 V	15 A
PI3421-00-LGIZ	1.8 V	1.4 V to 2.0 V	15 A
PI3422-00-LGIZ	2.5 V	2.0 V to 3.1 V	15 A
PI3423-00-LGIZ	3.3 V	2.3 V to 4.1 V	15 A
PI3424-00-LGIZ	5.0 V	3.3 V to 6.5 V	15 A

8 – 36 Vin
8 – 18 Vin

I²C is a trademark of NXP Semiconductors

Resources

- Video: Interview with ECE Europe about ZVS Regulators
- Webinar: ZVS Point-of-Load Regulation – Enabling High Performance On-Board Power Solutions
- Webinar: Design Considerations For High Performance On-Board Power Design
- Cool-Power ZVS Buck Regulators Product Information



- Reduces Q1 turn-on losses
- Reduces gate drive losses
- Reduces body diode conduction

Benefits of Zero-Voltage-Switching Topology

VI Chip PRM Module

Simple to Use

- Point-of-load, Buck-Boost regulation
- Factorized Power Architecture
- Minimal external components

High Density

- Up to 1,700 W/in³, with 500 W in 1.1in² package

Wide Vin Optimized for 48 Vout

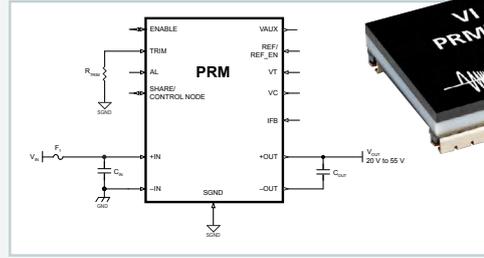
- 24 Vin, 18 – 36 Vin range
- 36 Vin, 18 – 60 Vin range
- 45 Vin, 38 – 55 Vin range
- 48 Vin, 36 – 75 Vin range

High Efficiency

- Full chip 500 W: 97.8%
- Half chip 250 W: 96.7%

Flexible

- Regulation: Remote sense, local loop, adaptive loop
- Parallel capabilities



PRM Modules Model Number	Input Voltage Nom. (V)	Input Voltage Range (V)	Output Voltage Voltage Range (V)	Output Power Max.	Output Current Max.	Package Size
P024F048T12AL	24 V	18 – 36 V	26 – 55 V	120 W	2.5 A	Full
P036F048T12AL	36 V	18 – 60 V	26 – 55 V	120 W	2.5 A	Full
P045F048T17AL	45 V	38 – 55 V	26 – 55 V	170 W	3.5 A	Full
P045F048T32AL	45 V	38 – 55 V	26 – 55 V	320 W	6.67 A	Full
P048F048T12AL	48 V	36 – 75 V	26 – 55 V	120 W	2.5 A	Full
P048F048T24AL	48 V	36 – 75 V	26 – 55 V	240 W	5.0 A	Full
PRM48BH480T200A00	48 V	38 – 55 V	5 – 55 V	200 W	4.17 A	Half
PRM48BF480T400A00	48 V	38 – 55 V	5 – 55 V	400 W	8.33 A	Full
✘ PRM48AH480T200A00	48 V	36 – 75 V	20 – 55 V	200 W	4.17 A	Half
✘ PRM48AF480T400A00	48 V	36 – 75 V	20 – 55 V	400 W	8.33 A	Full
✘ PRM48BH480T250A00	48 V	38 – 55 V	20 – 55 V	250 W	5.21 A	Half
✘ PRM48BF480T500A00	48 V	38 – 55 V	20 – 55 V	500 W	10.42 A	Full

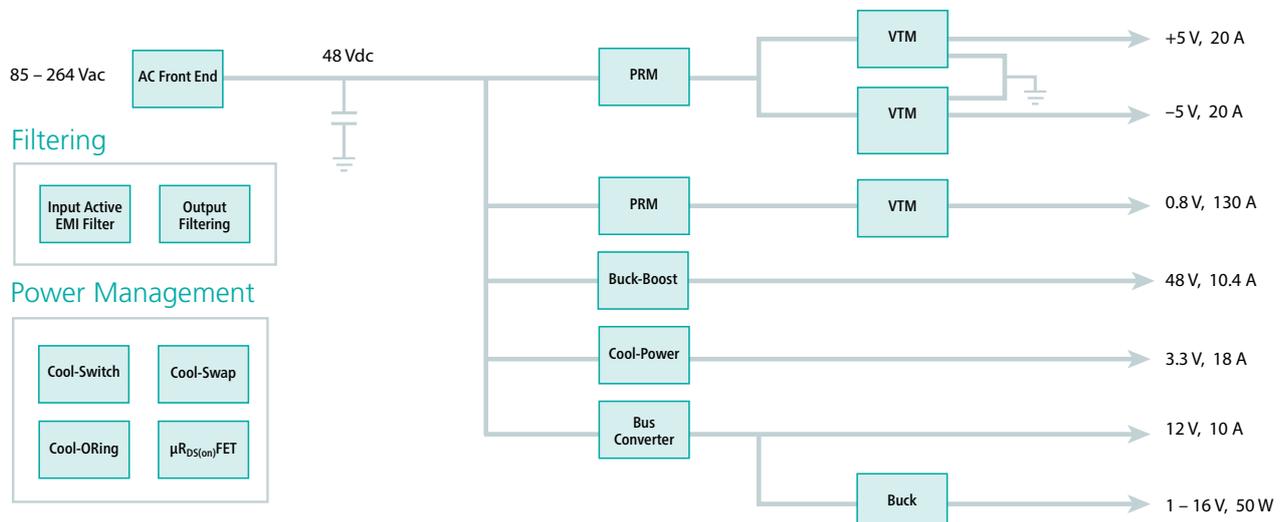


These PRM modules can be further configured to meet your exact needs.

<input type="checkbox"/>	V	Min: <input type="text"/>	Max: <input type="text"/>
Undervoltage Lockout	<input type="checkbox"/>	Min: <input type="text"/>	Max: <input type="text"/>
Hysteresis	<input type="checkbox"/>	Min: <input type="text"/>	Max: <input type="text"/>
Overvoltage Lockout	<input type="checkbox"/>	Min: <input type="text"/>	Max: <input type="text"/>
Hysteresis	<input type="checkbox"/>	Min: <input type="text"/>	Max: <input type="text"/>
Overvoltage Lockout	<input type="checkbox"/>	Min: <input type="text"/>	Max: <input type="text"/>
Hysteresis	<input type="checkbox"/>	Min: <input type="text"/>	Max: <input type="text"/>
Output Voltage			

Resources

- Video: Overview of Vicor's VI Chip PRM Module
- PRM Product Information
- Configure a PRM for your application's requirements



Solutions from AC to Point of Load

Introducing... The Growing ChiP Lineup

"Converters housed in Package" Technology

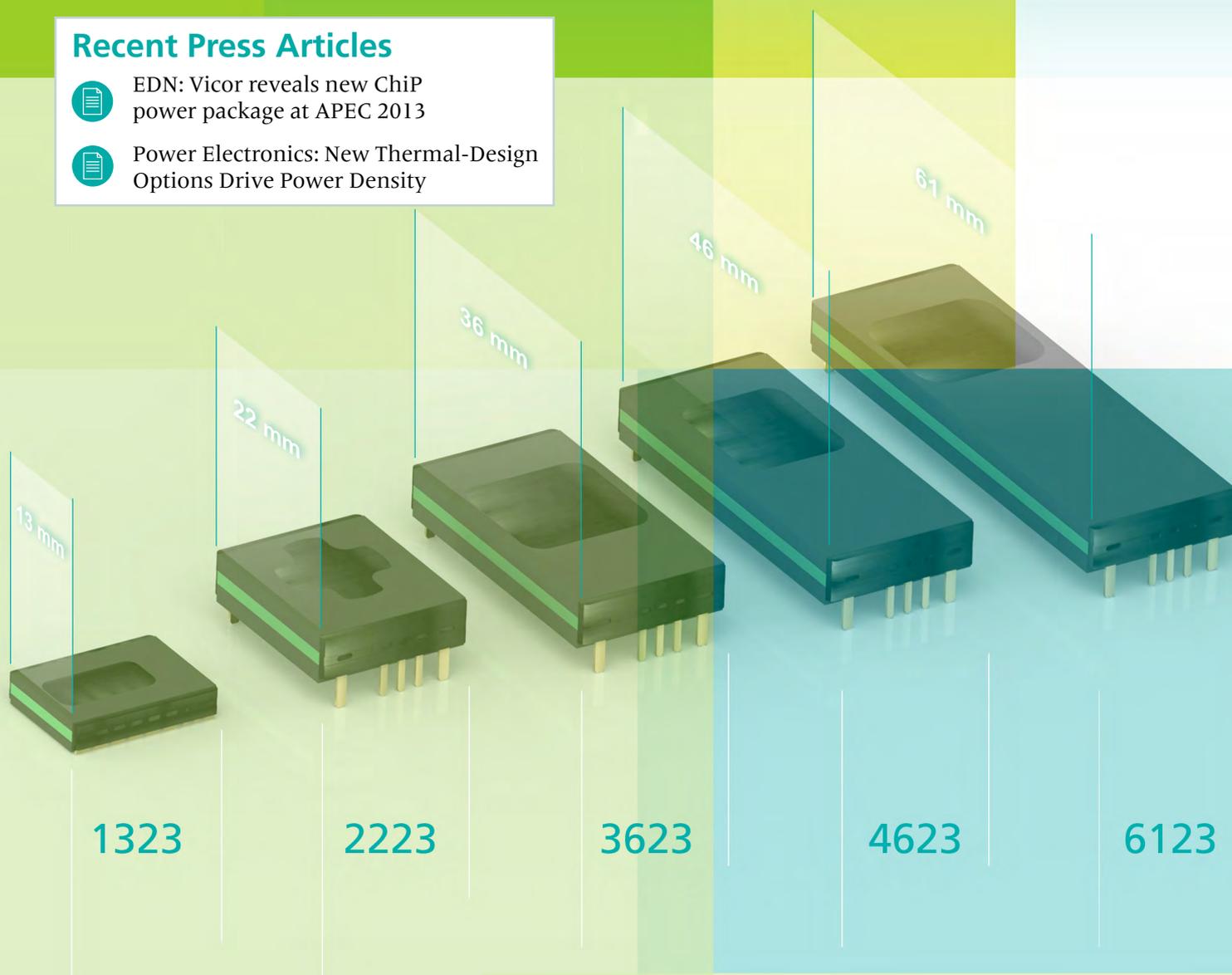
Recent Press Articles



EDN: Vicor reveals new ChiP power package at APEC 2013



Power Electronics: New Thermal-Design Options Drive Power Density



Resources



2013 APEC Plenary Session
Patrizio Vinciarelli, CEO, Vicor Corporation



Stephen Oliver
Vice President, VI Chip Product Line



Vicor's CEO discusses ChiP technology at APEC



An introduction to ChiP technology

Online Design Tools

Online Simulator

- Simulate electrical and thermal behavior
- User defines line and load conditions, input and output impedance and filters
- Simulations include start-up, steady state, shutdown, Vin step and load step, as well as thermal.
- Electrical and thermal performance showed in charts and tables

- Determine trim resistors for fixed and variable output voltage trimming
- Calculate required bus capacitance for VI-ARM, FARM, and ENMod modules
- Thermal calculator for heat sink selection

Filter Design

- Select attenuation and frequency
- Choose from five different topologies
- Supports regulated and unregulated converters

Design Calculators

Resources

-  Video: Using Vicor's online simulator
-  Online simulator: VI Brick IBCs
-  Online simulator: BCMs
-  Online simulator: PRMs
-  Filter design tool
-  Design calculators



Watch Video

Visit NEW Website ▶

Navigate >
Select >
Architect >
Configure >
Simulate >

Configure Your Product

PowerBench™ online design center

- Design your own DC-DC converters to meet your application's requirements
- Or use hundreds of predefined designs
- Online registration allows designs to be saved

VI Chip® PRM® Module

- Point-of-Load Buck-Boost regulation with remote sense
- Full Chip (up to 500 W in 1.1 in²)
- Half Chip (up to 250 W in 0.57 in²)

Other DC-DC Converters

- Maxi, Mini, Micro Series: Full (160–600 W), Half (100–300 W), Quarter (50–150 W)
- VI-200 / VI-J00 Series: Full brick (50–200 W), Half brick (25–100 W)
- ComPAC, VIPAC Arrays and chassis-mount MegaMods

AC-DC Converters

- VIPAC - Autoranging input with filtering, multiple output, cold plate chassis,
- FlatPAC - Multiple output and autorange input with heat sink or conduction-cooled models

Complete power systems

- Westcor custom AC-DC
- High power density, small size, high efficiency
- Fan-cooled, slide-in assemblies

Resources

-  PowerBench online design center
-  Design calculators
-  Webinar: Modeling, Simulation, and Selection Techniques in Power Design

VI Chip PRM Module Configurator

User Defined Module

Specify a User Defined PRM Module All PRM Modules

Designer's Reference (This text is for reference in M)

Input Voltage

Voltage Range Platform

1. Wide (36-75 V) Narrow (38-55V)

	Selection Range
Vin Low Line	<input type="text"/> V
Vin Nominal	<input type="text"/> V
Vin High Line	<input type="text"/> V
Undervoltage Lockout	<input type="text"/> %
Undervoltage Lockout Hysteresis	<input type="text"/> %

Enabling Our Customers' Competitive Advantage

At Vicor, we enable customers to efficiently convert and manage power from the wall plug to point of load.

We master the entire power chain with the most comprehensive portfolio of high efficiency, high-density, power distribution architectures addressing a broad range performance-critical applications.

Vicor's holistic approach gives power system architects the flexibility to choose from modular, plug-and-play components ranging from bricks to semiconductor-centric solutions.

By integrating our world-class manufacturing and applications development, we can quickly customize our power components to meet your unique power system needs.

Focus Performance-Centric Markets /Applications

Communications

- > 400 VDC Power Distribution
- > Datacom
- > Netcom
- > Telecom Infrastructure

Computing

- > Data Centers
- > High Performance Computing
- > Network Servers

Industrial

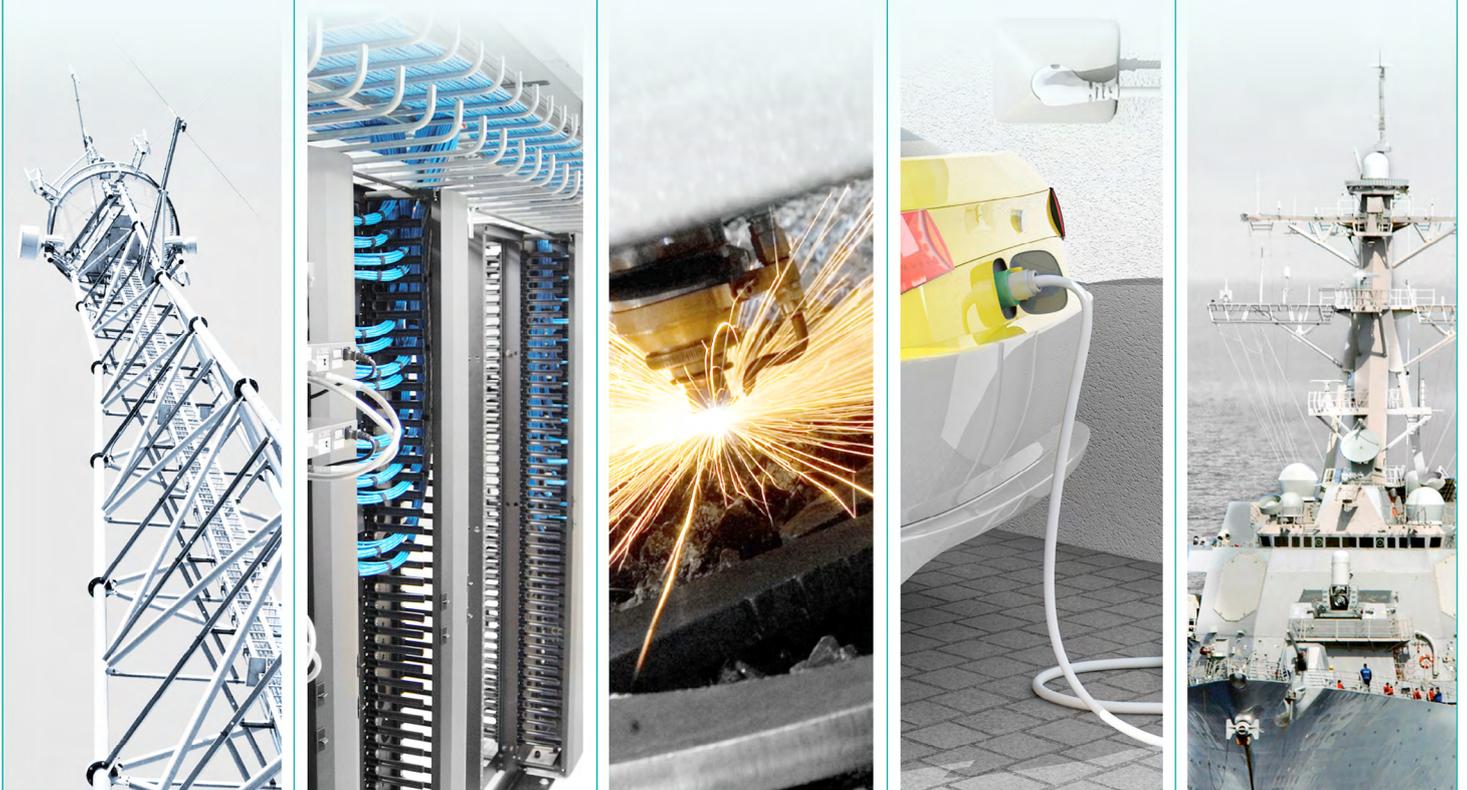
- > ATE
- > Lighting
- > Process Control
- > Transportation

Automotive

- > Electric Vehicles
- > Hybrid Vehicles

Defense/Aerospace

- > Aircraft Test Equipment
- > Ground Vehicles
- > Radar
- > Telemetry
- > Unmanned Vehicles



FILTER FUTURES; SAW, BAW AND EMERGING WIRELESS STANDARDS

RF interference has always been an inhibitor of communications, requiring designers to perform major feats to keep it in check. Today's wireless devices must not only reject signals from other services but from themselves, too, as the number of bands packed inside each device increases.

A high-end smartphone must filter the transmit and receive paths for 2G, 3G, and 4G wireless access methods in up to 15 bands, as well as Wi-Fi, Bluetooth and the receive path of GPS receivers. Signals in the receive paths must be isolated from one another. They also must reject other extraneous signals whose causes are too diverse to list. To do so, a multi-band smartphone will require eight or nine filters and eight duplexers. Without acoustic filter technology, it would be impossible.

SAW: MATURE BUT STILL GROWING

Surface acoustic wave (SAW) filters are used widely in 2G receiver front ends and in duplexers and receive filters. SAW filters combine low insertion loss with good rejection, can achieve broad bandwidths and are a tiny fraction of the size of traditional cavity and even ceramic filters. Because SAW filters are fabricated on wafers, they can be created in large volumes at low cost. SAW technology also allows filters and duplexers for different bands to be integrated on a single chip with little or no additional fabrication steps.

The piezoelectric effect that exists in crystals with a certain symmetry is the 'motor' as well as the 'generator' in acoustic filters. When applying a voltage to such a crystal, it will deform mechanically, converting electrical energy into mechanical energy. The opposite occurs when such a crystal is mechanically compressed or expanded. Charges form on opposite faces of the crystalline structure, causing a current to flow in the terminals and/or voltage between the terminals. This conversion between electrical and mechanical domains happens with extremely low energy loss, achieving exceptional efficiency of 99.99% in both directions.

In solid materials, alternating mechanical deformation creates acoustic waves that travel at velocities of 3,000 to 12,000 m/sec. In acoustic filters, the waves are confined to create standing waves with extremely high quality factors (Q) of several thousand. These high-Q resonances are the basis of the frequency selectivity and low loss that acoustic filters achieve.

In a basic SAW filter, an electrical input signal is converted to an acoustic wave by interleaved metal interdigital transduc-

ers (IDTs) created on a piezoelectric substrate, such as quartz, lithium tantalite (LiTaO3) or lithium niobate (LiNbO3). Its slow velocity makes it possible to fit many wavelengths across the IDTs in a very small device.

SAW filters, however, have limitations. Above about 1 GHz,

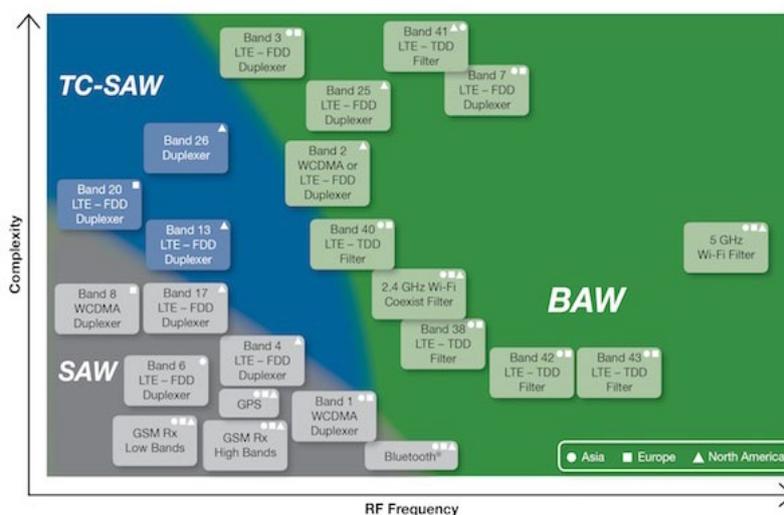
their selectivity declines, and at about 2.5 GHz their use is limited to applications that have modest performance requirements. SAW devices also are notoriously sensitive to temperature changes: the stiffness of the substrate material tends to decrease at higher temperatures and acoustic velocity diminishes.

An alternative approach is to use temperature-compensated (TC-SAW) filters, which include over-coating of the IDT structures with layers that increase stiffness at higher temperatures. While an uncompensated SAW device typically has a temperature coefficient of frequency (TCF) of about -45 ppm/°C, TC-SAW filters reduce this to -15 to -25 ppm/°C. However, because the process doubles the number of required mask layers, TC-SAW filters are more complex and thus more expensive to manufacture, but still less expensive than bulk acoustic wave (BAW) filters.

BAW filters provide compelling performance advantages above 1.5GHz

HIGH-PERFORMANCE BAW

While SAW and TC-SAW filters are well-suited for use at up to about 1.5 GHz, BAW filters deliver compelling performance advantages above this frequency (see Figure). BAW filter size also decreases with higher frequencies, which makes them ideal for the most demanding 3G and 4G applications. In addition, BAW design is far less sensitive to temperature variation even at broad bandwidths, while delivering very low loss and very steep filter skirts.



BAW filters provide compelling performance advantages above 1.5GHz

In the full version of this article, the author proceeds to describe the detail of BAW principles and construction, outlines the filtering performance of which current devices are capable, and indicates where further improvements in specification may be expected. Read the complete article here, online or via a pdf download.

BASIC CONCEPTS OF LINEAR REGULATOR AND SWITCHING MODE POWER SUPPLIES

PART II

This article explains the basic concepts of linear regulators and switching mode power supplies (SMPS). It is aimed at system engineers who may not be very familiar with power supply designs and selection. In part I of this article (available here) the author covered the basic operating principles of linear regulators and SMPS, including the operation and sources of losses in a buck converter. He continues now with a discussion of design considerations of the switching power components in the converter.

SWITCHING FREQUENCY OPTIMISATION

In general, higher switching frequency means smaller size output filter components L and C_o. As a result, the size and cost of the power supply can be reduced. Higher bandwidth can also improve load transient response. However, higher switching frequency also means higher AC-related power loss, which requires larger board space or a heat sink to limit the thermal stress. Currently, for output current applications at or above 10A, most step-down supplies operate in the range of 100 kHz to 1 MHz ~ 2 MHz. For load currents under 10A, the switching frequency can be up to several MHz. The optimum frequency for each design is a result of careful trade-offs in size, cost, efficiency and other performance parameters.

OUTPUT INDUCTOR SELECTION

In a synchronous buck converter, the inductor peak-to-peak ripple current can be calculated as:

$$\Delta I_{L(P-P)} = \frac{(V_{IN} - V_O) \cdot V_O / V_{IN}}{L \cdot f_s} \quad (14)$$

With a given switching frequency, a low inductance gives large ripple current and results in large output ripple voltage. Large ripple current also increases MOSFET RMS current and

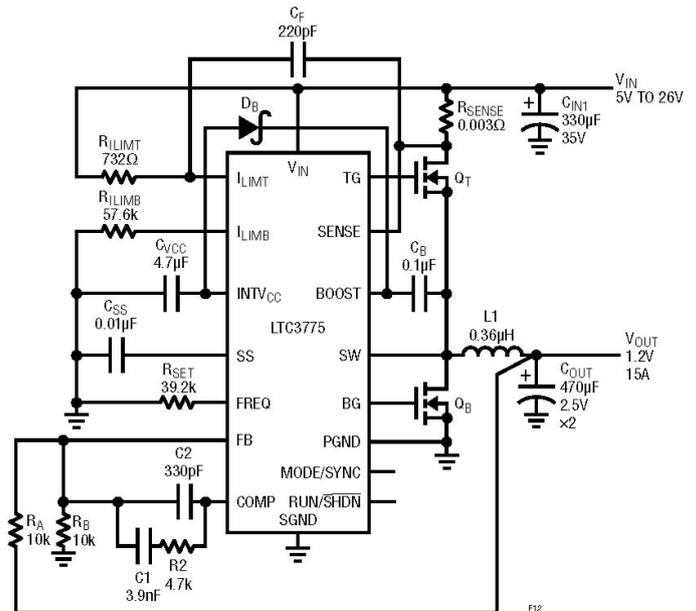


Figure 12. The LTC3775 voltage mode synchronous buck supply offers a high step-down ratio

conduction losses. On the other hand, high inductance means large inductor size and possible high inductor DCR and conduction losses. In general, 10% ~ 60% peak-to-peak ripple current is chosen over the maximum DC current ratio when selecting an inductor. The inductor vendors usually specify the DCR, RMS (heating) current and saturation current ratings. It is important to design the maximum DC current and peak current of the inductor within the vendor's maximum ratings.

POWER MOSFET SELECTION

When selecting a MOSFET for a buck converter, first make sure its maximum VDS rating is higher than the supply V_{IN(MAX)} with sufficient margin. However, do not select a FET with an excessively high voltage rating. For example, for a 16V_{IN(MAX)} supply, a 25V or 30V rated FET is a good fit. A 60V rated FET can be excessive, because the FET on-resistance usually increases with rated voltage. Next, the FET's on-resistance R_{DS(ON)} and gate charge Q_G (or Q_{GD}) are two most critical parameters. There is usually a trade-off between the gate charge Q_G and on-resistance R_{DS(ON)}. In general, a FET with small silicon die size has low QG but high on-resistance R_{DS(ON)}, while a FET with a large silicon die has low R_{DS(ON)} but large Q_G. In a buck converter, the top MOSFET Q1 takes both conduction loss and AC switching loss. A low Q_G FET is usually needed for Q1, especially in applications with low output voltage and small duty cycle. The lower side synchronous FET Q2 has small AC loss because it is usually turned on or off when its VDS voltage is near zero. In this case, low R_{DS(ON)} is more important than Q_G for synchronous FET Q2. When a single FET cannot handle the total power, several MOSFETs can be used in parallel.

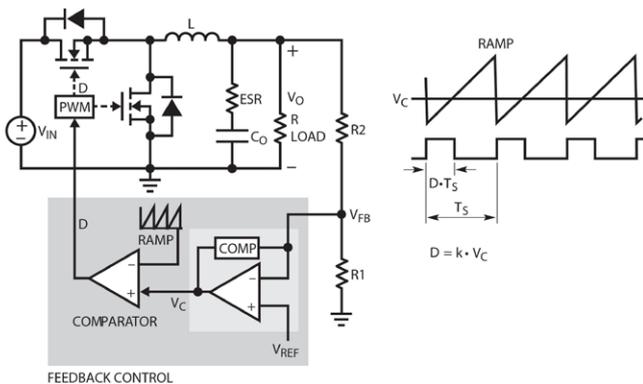


Figure 11. Block diagram of a voltage mode-controlled buck converter

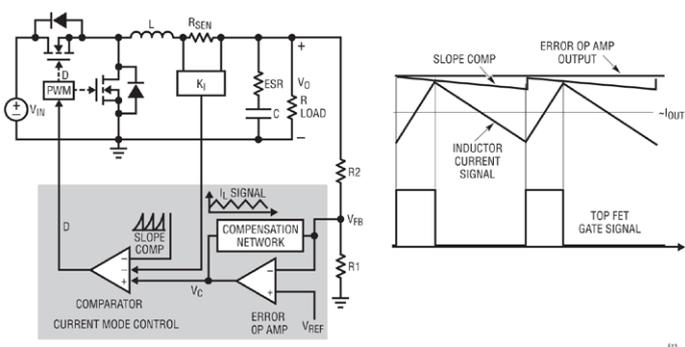


Figure 13. Block diagram of a current mode-controlled buck converter

INPUT AND OUTPUT CAPACITOR SELECTION

First, the capacitors should be selected with sufficient voltage derating. The input capacitor of a buck converter has pulsating switching current with large ripple. Therefore, the input capacitor should be selected with sufficient RMS ripple current rating to ensure its lifetime. Aluminum electrolytic capacitors and low ESR ceramic capacitors are usually used in parallel at the input.

The output capacitor determines not only the output voltage ripple, but also the load transient performance. The output voltage ripple can be calculated by Equation (15). For high performance applications, both the ESR and total capacitance are important to minimize output ripple voltage and to optimize load transient response. Usually, low ESR tantalum, low ESR polymer capacitors and multilayer ceramic capacitors (MLCC) are good choices.

$$\Delta V_{OUT} \approx \Delta I_{L(P-P)} \cdot \left(ESR + \frac{1}{8 \cdot f_S \cdot C_{OUT}} \right) \quad (15)$$

CLOSE THE FEEDBACK REGULATION LOOP

There is another important design stage for a switching mode supply—closing the regulation loop with a negative feedback control scheme. This is usually a much more challenging task than using an LR or LDO. It requires good understanding of loop behaviour and compensation design to optimise dynamic performance with a stable loop.

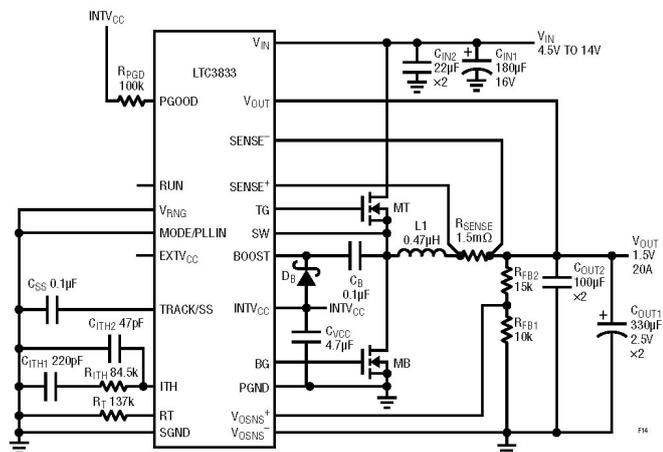


Figure 14. Fast, controlled-on-time current mode supply using the LTC3833

Consider the small-signal model of the buck converter: as explained above, a switching converter changes its operation mode as a function of the switch ON or OFF state. It is a discrete and nonlinear system. To analyse the feedback loop with the linear control method, linear small signal modelling is needed [Reference 1]. Because of the output L-C filter, the linear small signal transfer function of duty cycle D to output VO is actually a second-order system with two poles and one zero, as shown in Equation (16). There are double poles located at the resonant frequency of the output inductor and capacitor. There is a zero determined by the output capacitance and the capacitor ESR.

$$G_{DV}(s) = \frac{V_O}{D} = \frac{V_{IN} \cdot \left(1 + \frac{s}{S_{Z_ESR}} \right)}{1 + \frac{s}{\omega_0 \cdot Q} + \frac{s^2}{\omega_0^2}} \quad (16)$$

Where, $S_{Z_ESR} = 2\pi f_{Z_ESR} = 1 / ESR \cdot C_O$,

$$\omega_0 = 2\pi f_{W0} = \frac{1}{\sqrt{L \cdot C_O}} \cdot \sqrt{\frac{1 + \frac{DCR}{R}}{1 + \frac{ESR}{R}}} \approx \frac{1}{\sqrt{L \cdot C_O}} \quad (17)$$

VOLTAGE MODE VS. CURRENT MODE CONTROL

The output voltage can be regulated by a closed loop system shown in Figure 11. For example, when the output voltage increases, the feedback voltage VFB increases and the output of the negative feedback error amplifier decreases. So the duty cycle decreases. As a result, the output voltage is pulled back to make VFB = VREF. The compensation network of the error op amp can be a type I, type II or type III feedback amplifier network [Reference 4]. There is only one control loop to regulate the output. This scheme is referred to as voltage mode control. Linear Technology's LTC3775 and LTC3861 are typical voltage mode buck controllers.

Figure 12 shows a 5V to 26V input, 1.2V/15A output synchronous buck supply using the LTC3775 voltage mode buck controller. Due to the LTC3775's leading-edge PWM modulation architecture and very low (30 nsec) minimum on-time, the supply operates well for applications that convert a high voltage automotive or industrial power supply down to the 1.2V low voltage required by today's microprocessors and programmable logic chips. [Reference 9] High power applications require multi-phase buck converters with current sharing. With voltage mode control, an additional current sharing loop is required to balance current among parallel buck channels. A typical current sharing method for voltage mode control is the master-slave method. The LTC3861 is such a PolyPhase voltage mode controller. Its very low, ± 1.25 mV, current sense offset makes current sharing between paralleled phases very accurate to balance the thermal stress. [Reference 10]

Current mode control uses two feedback loops: an outer voltage loop similar to the control loop of voltage mode-controlled converters, and an inner current loop that feeds back the current signal into the control loop. Figure 13 shows the conceptual block diagram of a peak current mode control buck converter that directly senses the output inductor current.

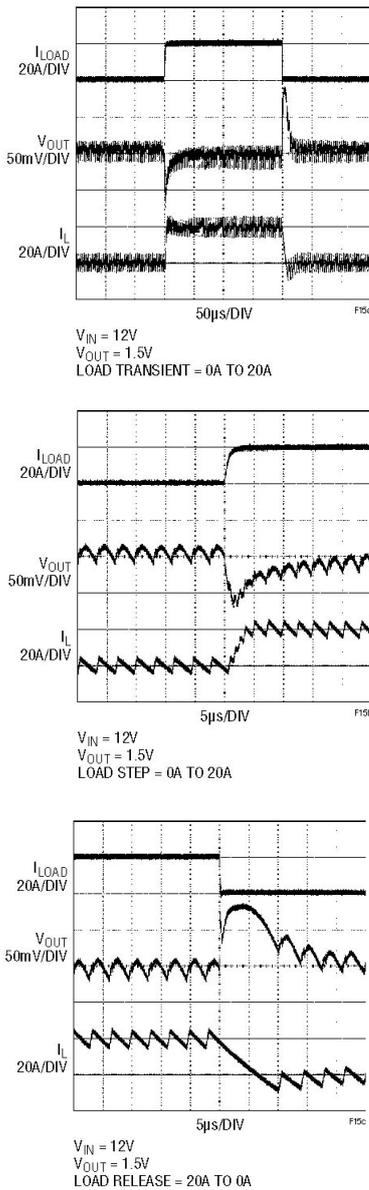


Figure 15. LTC3833 supply offers fast response during rapid load step transients

mode-controlled converter is more reliable than a voltage mode-controlled converter.

The current mode control scheme solution needs to sense the current precisely. The current sensing signal is usually a small signal at a level of tens of millivolts that is sensitive to switching noise. Therefore, proper and careful PCB layout is needed. The current loop can be closed by sensing the inductor current through a sensing resistor, the inductor DCR voltage drop, or the MOSFET conduction voltage drop. Typical current mode controllers include Linear Technology's LTC3851A and LTC3855.

CONSTANT FREQUENCY VS. CONSTANT ON-TIME CONTROL

Typical voltage mode and current mode schemes in the Voltage Mode Control vs. Current Mode Control section have constant switching frequency generated by controller internal clocks. These constant switching frequency controllers can be easily

With current mode control, the inductor current is determined by the error op amp output voltage. The inductor becomes a current source. Therefore, the transfer function from op amp output, VC, to supply output voltage VO becomes a single pole system. This makes loop compensation much easier. The control loop compensation has less dependency on the output capacitor ESR zero, so it is possible to use all-ceramic output capacitors.

There are many other benefits from current mode control. As shown in Figure 13, since the peak inductor current is limited by the op amp VC in a cycle-by-cycle fashion, the current mode-controlled system provides a more accurate and faster current limit under overload conditions. The in-rush inductor current is well controlled during start-up, too. Also, the inductor current does not change quickly when the input voltage changes, so the supply has good line transient performance. When multiple converters are paralleled, with current mode control, it is also very easy to share current among supplies, which is important for reliable high current applications using PolyPhase buck converters. In general, a current

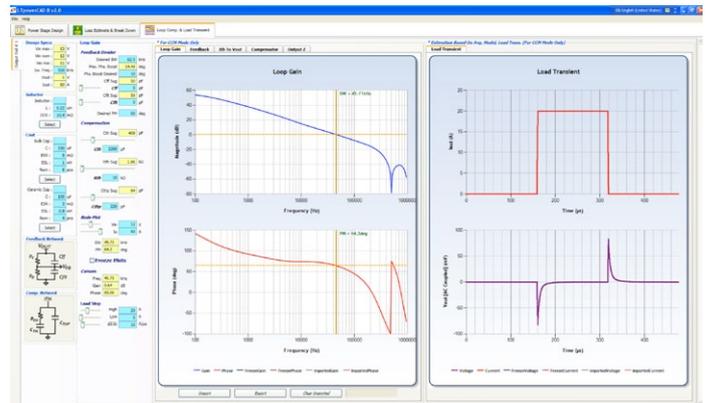


Figure 16. LTpowerCAD design tool provides an easy way to optimise the loop compensation and load transient response (3-phase, single-output LTC3829 buck converter example).

synchronised, an important feature for high current, PolyPhase buck controllers. However, if the load step-up transient occurs just after the control FET Q1 gate is turned off, the converter must wait the entire Q1 off-time until the next cycle to respond to the transient. In applications with small duty cycles, the worst-case delay is close to one switching cycle.

In such low duty cycle applications, constant on-time valley current mode control has shorter latency to respond to load step-up transients. In steady state operation, the switching frequency of constant on-time buck converters is nearly fixed. In the event of a transient, the switching frequency can vary quickly to speed up the transient response. As a result, the supply has improved transient performance and output capacitance and its related cost can be reduced.

However, with constant on-time control, the switching frequency may vary with line or load. The LTC3833 is a valley current mode buck controller with a more sophisticated controlled-on-time architecture—a variant of the constant on-time control architecture with the distinction that the on-time is controlled so that the switching frequency remains constant over steady stage conditions under line and load. With this architecture, the LTC3833 controller has 20 nsec minimum on-time and allows step-down applications from up to 38V VIN to 0.6V VO.

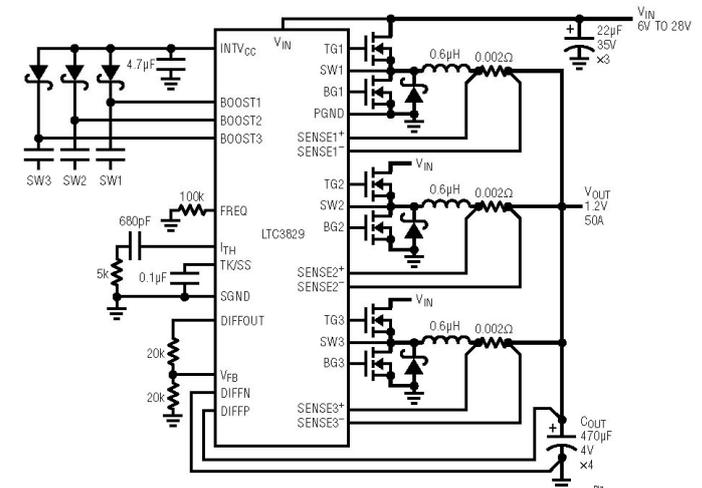


Figure 17. A 3-phase, single VO high current buck converter using the LTC3829

The controller can be synchronised to an external clock in the 200 kHz to 2 MHz frequency range. Figure 14 shows a typical LTC3833 supply with 4.5V to 14V input and 1.5V/20A output. [Reference 11] Figure 15 shows that the supply can respond quickly to sudden, high slew rate load transients. During the load step-up transient, the switching frequency increases to provide faster transient response. During the load step-down transient, the duty-cycle drops to zero. Therefore only the output inductor limits the current slew rate. In addition to the LTC3833, for multiple outputs or PolyPhase applications, the LTC3838 and LTC3839 controllers provide fast transient, multi-phase solutions.

LOOP BANDWIDTH AND STABILITY

A well-designed SMPS is quiet, both electrically and acoustically. This is not the case with an undercompensated system, which tends to be unstable. Typical symptoms of an undercompensated power supply include: audible noise from the magnetic components or ceramic capacitors, jitter in the switching waveforms, oscillation of output voltage, and so on. An overcompensated system can be very stable and quiet, but at the cost of a slow transient response. Such a system has a loop crossover frequency at very low frequencies, typically below 10 kHz. Slow transient response designs require excessive output capacitance to meet transient regulation requirements, increasing the overall supply cost and size. An optimum loop compensation design is stable and quiet, but is not overcompensated, so it also has a fast response to minimise output capacitance. There are numerous articles that discuss how to optimise loop compensation networks for both voltage mode-controlled and current mode-controlled SMPS [References 2-4]. Small signal modelling and loop compensation design can be difficult for inexperienced power supply designers. Linear Technology's LT-powerCAD design tool handles the complicated equations and makes loop compensation a much simpler task [Reference 6]. The LTspice simulation tool integrates all of Linear Technology's part models and provides additional time domain simulations to optimise the design. However, bench test/verification of loop stability and transient performance is usually necessary in the prototype stage.

In general, the performance of the closed voltage regulation loop is evaluated by two important values: the loop bandwidth and the loop stability margin. The loop bandwidth is quantified by the crossover frequency f_c , at which the loop gain $T(s)$ equals one (0 dB). The loop stability margin is typically quantified by the phase margin or gain margin. The loop phase margin Φ_m is defined as the difference between the overall $T(s)$ phase delay and -180° at the crossover frequency. The gain margin is defined by the difference between $T(s)$ gain and 0dB at the frequency where overall $T(s)$ phase equals -180° . For a buck converter, typically 45-degree phase margin and 10 dB gain margin is considered sufficient. Figure 16 shows a typical Bode plot of loop gain for a current mode LTC3829 12VIN to 1V0/60A 3-phase buck converter. In this example, the crossover frequency is 45 kHz and the phase margin is 64 degrees. The gain margin is close to 20 dB.

POLYPHASE BUCK CONVERTER FOR HIGH CURRENTS

As data processing systems become faster and larger, their processor and memory units demand more current at ever decreasing voltages. At these high currents, the demands on power supplies are multiplied. In recent years, PolyPhase (multiphase) synchronous buck converters have been widely used

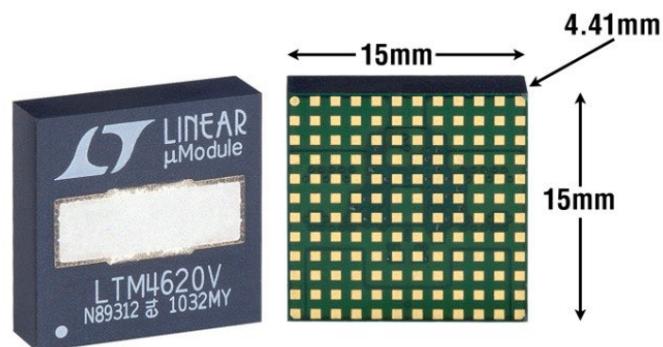
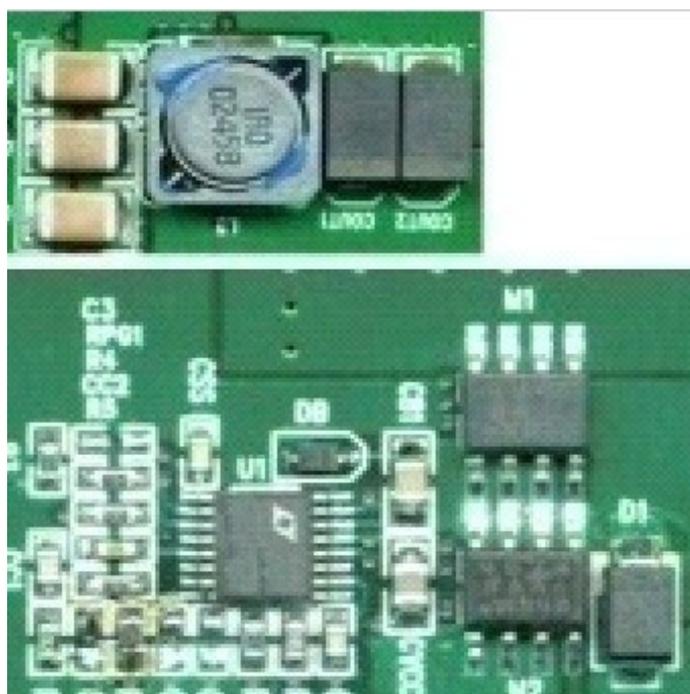


Figure 18. Examples of (a) a discrete 12VIN to 3.3V/10A LTC3778 supply; (b) a fully integrated 16VIN, dual 13A or single 26A LTM4620 μ Module step-down regulator

for high current, low voltage power supply solutions, due to their high efficiency and even thermal distribution. Besides, with interleaved multiple buck converter phases, the ripple current on both input and output sides can be significantly reduced, resulting in reduction of input and output capacitors and related board space and cost.

In PolyPhase buck converters, precise current sensing and sharing become extremely important. Good current sharing ensures even thermal distribution and high system reliability. Because of their inherent current sharing capability in steady state and during transients, current mode-controlled bucks are usually preferred. Linear Technology's LTC3856 and LTC3829 are typical PolyPhase buck controllers with precise current sensing and sharing. Multiple controllers can be connected in a daisy chain fashion for 2-, 3-, 4-, 6- and 12-phase systems with output current from 20A to over 200A.

OTHER REQUIREMENTS OF A HIGH PERFORMANCE CONTROLLER

Many other important features are required of a high performance buck controller. Soft-start is usually needed to control the inrush current during start-up. Overcurrent limit and short-circuit latchoff can protect the supply when the output is

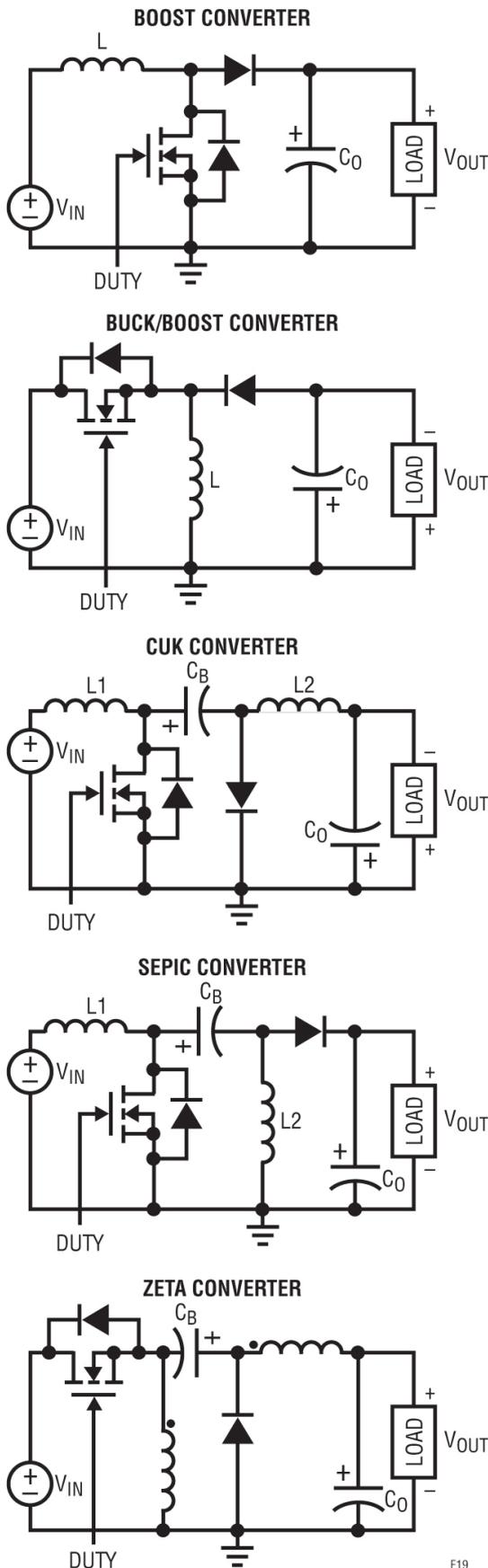


Figure 19. Other basic non-isolated DC/DC converter topologies.

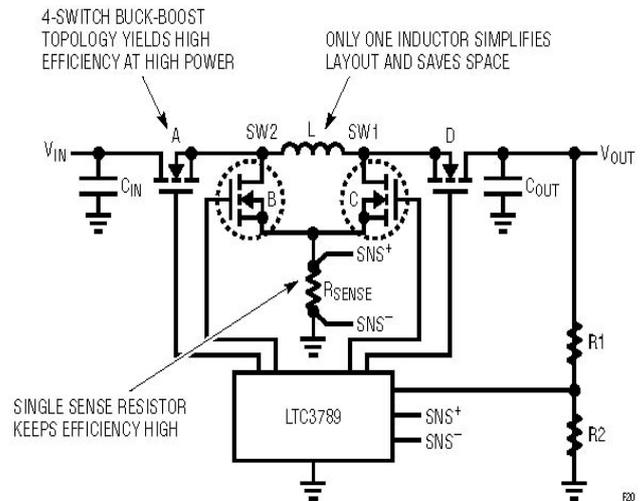


Figure 20. High efficiency 4-switch buck-boost converter operates with input voltage below, equal or above the output voltage

overloaded or shorted. Overvoltage protection safeguards the expensive load devices in the system. To minimise system EMI noise, sometimes the controller must be synchronised to an external clock signal. For low voltage, high current applications, remote differential voltage sensing compensates for the PCB resistance voltage drop and accurately regulates output voltage at the remote load. In a complicated system with many output voltage rails, sequencing and tracking among different voltage rails is also necessary.

PCB LAYOUT

Component selection and schematic design is only half of the supply design process. Proper PCB layout of a switching supply design is always critical. In fact, its importance cannot be overstated. Good layout design optimises supply efficiency, alleviates thermal stress, and most importantly, minimises noise and interactions among traces and components. To achieve this, it is important for the designer to understand the current conduction paths and signal flows in the switching power supply. It usually requires significant effort to gain the necessary experience. See Linear Technology Application Note 136 for detailed discussions. [Reference 7]

CHOICES: DISCRETE, MONOLITHIC AND INTEGRATED SUPPLIES

At the integration level, system engineers can decide whether to choose a discrete, monolithic or fully integrated power module solution. Figure 18 shows examples of discrete and power module solutions for typical point-of-load supply applications. The discrete solution uses a controller IC, external MOSFETs and passive components to build the power supply on the system board. A major reason to choose a discrete solution is low component bill of materials (BOM) cost. However, this requires good power supply design skills and relatively long development time. A monolithic solution uses an IC with integrated power MOSFETs to further reduce the solution size and component count. It requires similar design skills and time. A fully integrated power module solution can significantly reduce design effort, development time, solution size and design risk, but usually with a higher component BOM cost.

OTHER BASIC NON-ISOLATED DC/DC SMPS TOPOLOGIES

This article uses buck converters as a simple example to demonstrate the design considerations of SMPS. However, there are at least five other basic non-isolated converter topologies (boost, buck/boost, Cuk, SEPIC and Zeta converters) and at least five basic isolated converter topologies (flyback, forward, push-pull, half-bridge and full-bridge), which are not covered here. Each topology has unique properties that make it suited for specific applications. Figure 19 shows simplified schematics for the other non-isolated SMPS topologies.

There are still other non-isolated SMPS topologies, which are combinations of the basic topologies. For example, Figure 20 shows a high efficiency, 4-switch synchronous buck/boost converter based on the LTC3789 current mode controller. It can operate with input voltages below, equal, or above the output voltage. For example, the input can be in the range of 5V to 36V, and the output can be a regulated 12V. This topology is a combination of a synchronous buck converter and a synchronous boost converter, sharing a single inductor. When $V_{IN} > V_{OUT}$, switches A and B operate as an active synchronous buck converter, while the switch C is always off and switch D is always on. When $V_{IN} < V_{OUT}$, switches C and D operate as an active synchronous boost converter, while switch A is always on and switch B is always off. When V_{IN} is close to V_{OUT} , all four switches operate actively. As a result, this converter can be very efficient, with up to 98% efficiency for a typical 12V output application. [Reference 12] The LT8705 controller further extends the input voltage range up to 80V. To simplify the design and increase power density, the LTM4605, LTM4607 and LTM4609 further integrate a complicated buck/boost converter into a high density, easy-to-use power module. [Reference 13] They can be easily paralleled with load sharing for high power applications.

SUMMARY

In summary, linear regulators are simple and easy to use. Since their series regulation transistors are operated in a linear mode, supply efficiency is usually low when output voltage is much lower than input voltage. In general, linear regulators (or LDOs) have low voltage ripple and fast transient response. On the other hand, SMPS operate the transistor as a switch, and therefore are usually much more efficient than linear regulators. However, the design and optimisation of SMPS are more challenging and require more background and experience. Each solution has its own advantages and drawbacks for specific applications.

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About the Author

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The logo for EDN Europe features the letters 'EDN' in a large, bold, red, sans-serif font with a grid-like texture. To the right of 'EDN' is a large, light blue circle. Below 'EDN' and the circle, the word 'europe' is written in a white, lowercase, sans-serif font with a slight drop shadow, set against a dark blue horizontal bar.

A true op-amp made from inverters

by Colin Weltin-Wu

Ever-increasing demand for smaller, more efficient CPUs has driven CMOS fabrication deep into the nanometer scale. The supply scaling and device leakage of these fine processes adversely affects precision analogue circuits, leading researchers to find highly-digital alternative architectures for traditionally analogue-intensive functions [References 1, 2]. This “digitisation” of the analogue domain will eventually trickle down to the home hobbyist, who will face increasing difficulty finding simple analogue components. This frightening trend was foreshadowed in 1973 by a Fairchild Semiconductor application note [Ref. 3]; however, none of the examples given for op-amp-like circuits provide differential inputs. This Design Idea attempts to fill this void, demonstrating a two-stage op-amp with true differential inputs and near rail-rail output swing, operating from a single 5V supply.

Figure 1 shows the complete implementation of a two-stage op-amp using only four CD4049UBE [4] hex inverters, a resistor, and a capacitor. Note that pin 8 of U2 (Gnd) is left floating, while pin 1 of U3 (VCC) is left floating. The output of the parallel inverters in U2 is connected to the VCC pin of U1, while the output of the inverter in U3 is connected to the Gnd pin of U1. Figure 2 shows the functional transistor-level schematic of the resulting circuit, with extraneous transistors removed. The first

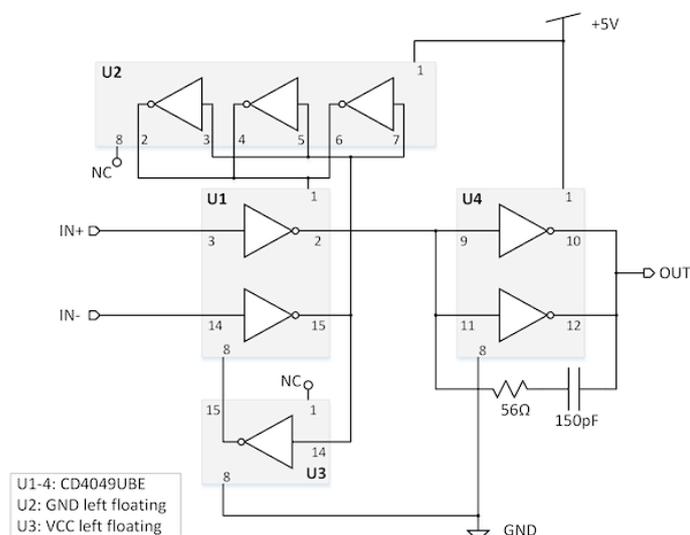


Figure 1. Two-stage op-amp.

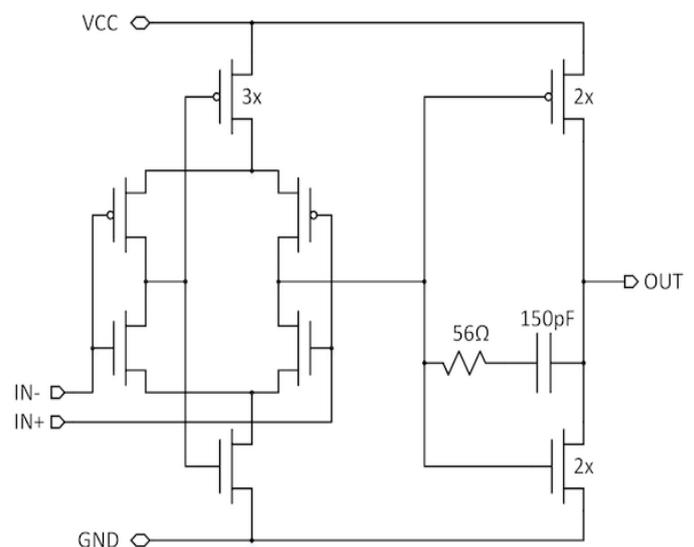


Figure 2. Transistor-level schematic.

stage is a circuit taken from [5], and implements the differential-to-single-ended conversion. The PMOS devices from the inverters in U2 behave as current sources, while NMOS in the inverter from U3 is a current sink. Unequal numbers of sources and sinks were used to pull the common mode range near mid-scale, due to the unequal NMOS and PMOS strengths. The inverters in U1 behave as a gm-doubled differential pair. Since the first stage only has between 25dB and 30dB of gain, a second stage is added. Standard compensation techniques are used to ensure overall stability, since both stages by themselves have similar bandwidths. Note that any reasonable feedback configuration forces the second stage into its linear range, obviating the need for a gain-reducing local shunt resistor. Table 1 is a brief summary of the op-amp specifications, as prototyped. Although it has differential inputs, it does not have great common mode rejection. On the other hand, it has a larger gain-bandwidth than the classic LM741. Figures 3 to 5 show the performance of the circuit, as fabricated in Figure 6. This design should work equally well with CD4069UB as well as 74HCU04 devices, although the ratio of devices in U2 and U3 may change to re-center the common-mode range with different drive strength transistors. The only critical aspect is that the inverters are unbuffered, otherwise each gain stage becomes a three-stage ring oscillator.

Parameter	Value	Units
Supply Voltage	5	V
Supply Current	6.2	mA
Differential Gain	67	dB
Common Mode Rejection Ratio	26	dB
Input Common Mode Range	1.3-3.2	V
Output Swing	0.5-4.5	V
Gain Bandwidth	2	MHz
Phase Margin	50	degree
Slew Rate	10	V/ μ s

Table 1. Op-amp specifications, as prototyped.

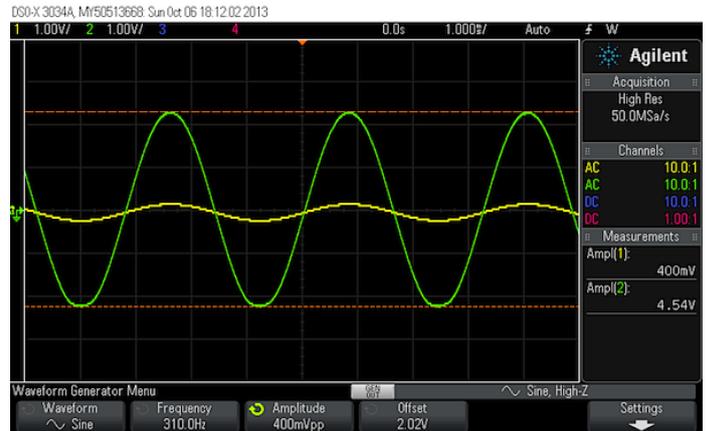


Figure 5. Almost true rail-rail operation from a single 5V supply (the op-amp configured with a non-inverting gain of 11).

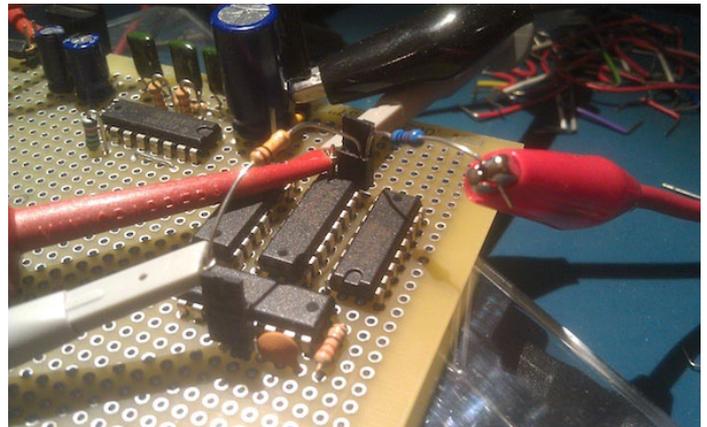


Figure 6. The prototype, built on perfbord.

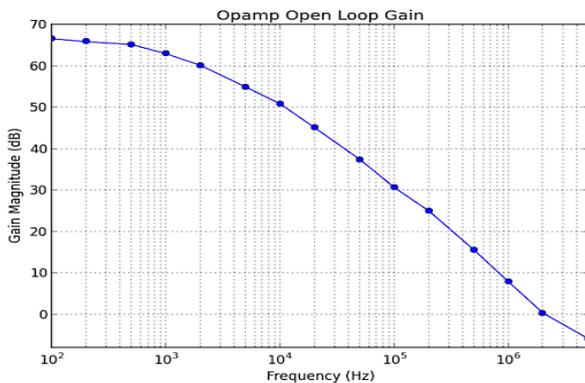


Figure 3. The measured gain magnitude response of the open-loop amplifier.

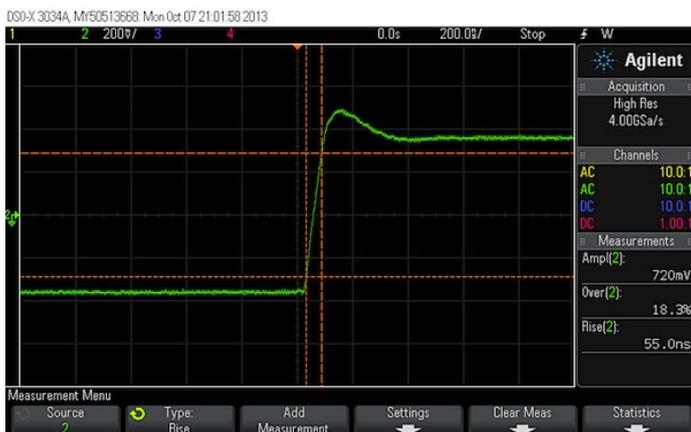


Figure 4. The large-signal step response for a voltage buffer configuration, which shows some overshoot characteristic of imperfect zero cancellation.

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Single-cycle logarithms & antilogs in FPGAs

By Michael Dunn (Editor, EDN (US))



Editor's note: Here's another contribution by myself. It's breaks the rules a bit, having been posted at Opencores.org, but I thought it deserved wider exposure.

My FPGA project needed fast logs – at video pixel rate – to make some wide-dynamic-range medical imaging data (24 bits) suitable for display. No problem. I'll just drop in the "log" block from the IP collection. Hmm...no log block. I did some online searching. No log blocks. I was on my own (porting a looping software algorithm would have been too slow, and pipelining it would have been too much trouble).

Within about 30 seconds, I had the design of a very crude log function in my head. All you need is a priority encoder. The log of a binary number is equal to the bit number of the most significant '1' bit. Done. Why did I bother with all that searching? Oh. Apparently, higher accuracy than this was required.

I continued to mull the problem over as I worked on other things. It finally dawned on me (as my high school maths returned) that the problem could be broken into two parts. The original crude encoder idea could make up the first part. But what to do with the bits below that uppermost '1'?

Eureka! Inspiration finally struck (or my brain finally switched on) with the result shown in Figure 1. If I shifted the input value so those lower bits were always in the same position (left-justified), I could use them to index into a lookup table. The encoder output could be viewed as the integer part of the result, and the LUT output as the fractional part.

The priority encoder output drives the barrel shifter's shift-count input, which normalises the input so that the most significant '1' bit of the input is now the msb of the barrel-shifter output (unless that '1' bit is in the lowest 8 bits of the input).

If you don't require full accuracy, you can remove the LUT and use the barrel shifter output directly. This provides a piecewise linear approximation. Figure 2 shows a bit of the simulation output.

Although my project didn't need antilog, I later wrote the code for it too (below is the schematic generated by Altera Quartus). In this example, the lower six bits of the 10 bit input index into an antilog table, and the upper four bits determine how much to shift the LUT's 24-bit output.

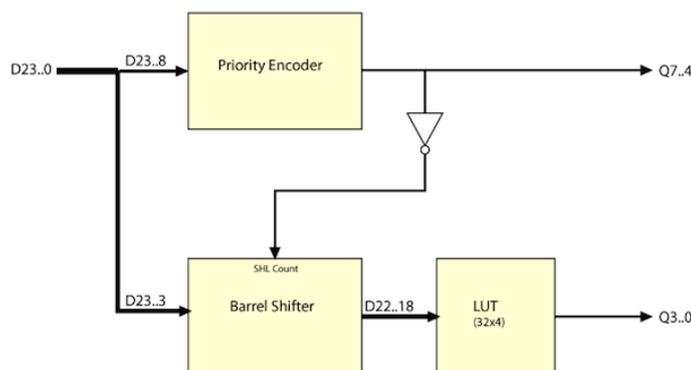


Figure 1. Block structure of the log function generators

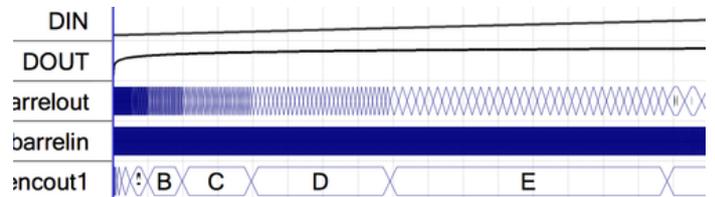


Figure 2. Simulation results

Downloads are available from the link below.

A nice upshot of having both log and antilog available is that it opens the door to many other operations, all of which can be executed in one cycle in a pipelined design.

Finding a square root is the first to come to my mind. Simply feed the logger's output into the antilog's input, but shifted one bit to the right. Any root or power of the 2, 4, 8, 16... variety can be done like this. Put a multiplier between the two blocks, and any arbitrary power or root can be generated, even fractional ones.

Need fast multiplication and division, but your hardware doesn't support it? Feed the operands into two log circuits. Add or subtract the outputs, and take the antilog of the result.

1960S TECHNOLOGY

A little extra: One of the stars (Figure 4) of my calculator collection is a Wang LOCI-2, circa 1966. It contains more than 1,200 discrete transistors and not a single IC. Nevertheless, it can do logs and antilogs. In fact, to multiply or divide, it takes the logs, adds or subtracts them, and then does an antilog. I have no clue how the logic works.

Appendix – Implementation notes:

Keep in mind that certain input widths will result in missed codes at the low end of the range. For example, as a 16-bit input changed from 1 to 2, the output would jump from 0x00 to 0x10. This example block diagram needs at least 21 bits for full accuracy.

To achieve maximum speed (at the expense of latency), sprinkle pipeline registers as required.

The LUT should have at least one more address bit than its data width to eliminate missing codes. Larger sizes will improve the accuracy of the output transition points.

If you have free multipliers in your FPGA, it may require fewer resources overall to use one in place of the barrel-shifter. But then you can't use the encoder output directly. You'll need to decode it to generate a 16-bit value.

For the "ultimate" in accuracy, use an adder to combine the LUT and encoder outputs instead of simply taking them directly. Why? When pre-computing the LUT entries, you'll find that one or more at the top end have a computed value that should ideally be rounded up. You can ignore this, round down, and forget the adder. Or, you can add one bit to the LUT's data width, round correctly, and use the adder to combine the (in this example) 5-bit LUT output and the 4-bit encoder output. This also means that the output will carry to the ninth bit at some point, so you must decide whether to use this, or to simply clip the output when this happens. Or perhaps the input

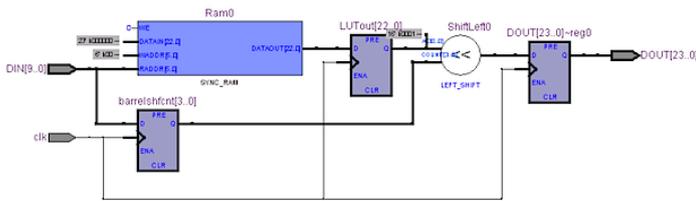


Figure 3. Block diagram of the functions as synthesised by Altera Quartus

is known to never go high enough to cause this. Downloads here; Log (three versions) and antilog code (System Verilog)

Michael Dunn is EDN Editor, Design Ideas, Automotive & Medical Design Centres

Michael Dunn has been messing with electronics almost as long as he's been walking, and got his first scope around age 15. Things have gone downhill since then. The scopes now vie with wine racks, harpsichords, calculators, and 19th century pianos for space. Over the years, he's designed for the automotive, medical, industrial, communications, and consumer industries, as both freelancer and employee, working with analog, digital, micros, and software. Since 2000, he's run the TekScopes Yahooogroup, now with over 5,000 members, and he was previously editor-in-chief of Scope Junction.

Measure inductance & capacitance over a wide range

by John Fattaruso - November 25, 2013



Most simple circuits you'll find for measuring reactive components cover only a limited range of component values. Here's a circuit built from a handful of inexpensive parts that will let you measure values of both capacitors and inductors over seven orders of magnitude. Capacitors from about 1 pF to 10 μF and inductors from about 200 nH to 4H can be characterised.

To cover this wide range, however, you'll need to give up a little convenience, as you find the DUT's value by adjusting a variable resistor and looking up a corresponding capacitance or inductance value on a calibration plot, rather than by a direct reading.

To understand circuit operation, start with the basics shown in Figure 1. In part a), a square wave voltage source drives the bottom terminal of the capacitor under test. The voltage at the top terminal

is a series of exponentially decaying positive- and negative-going pulses above and below the +5V rail. The time constant of the decay is of course the product $R \cdot C_{TEST}$. Similarly, in part b), a square wave current source feeds the test inductor, resulting in similar transients above and below the +5V rail, with the decay time constant equalling L_{TEST} / R . The portion of each half period of the square wave that is occupied by the exponential decay process depends on the relationship between the time constant and the oscillation period.

Now consider the complete schematic in Figure 2. A square wave is generated by IC1 wired as a simple Schmitt trigger RC oscillator and output buffer. The frequency is set by the variable resistor R9 and ranges A through F of six decade capacitors. R9 should have a linear taper and be wired so that the oscillator period increases with clockwise shaft rotation.

A DPDT switch selects between capacitor and inductor measurement modes. Following the basic scheme of Figure 1, either the voltage directly from the IC1 outputs or the current generated by Q1 is fed to the capacitor or inductor under test, respectively. The 510Ω resistor R2 functions as the decay resistance R of Figure 1 in 'L' mode, and the series connection of R5 and R2 forms the decay resistance in 'C' mode. (R5 is present to keep the voltage excursions at the base of Q2 low

enough to avoid saturation.) Bias resistor R7 and diodes D3 and D4 hold the base of Q3 at about $2V_{BE}$ below the +5V rail. At this bias point, Q2, R3, and Q3 form a rectifying transconductance block with a small idling current that is sensitive only to the positive going transients above the +5V rail from the component under test. The pulses of collector current from Q3 are dropped across R4, and the resulting voltage, averaged by C2 and C3, is measured by an external voltmeter.

Transients with an exponential decay that extend over a particular portion of the square wave period will produce a corresponding output DC voltage, but the exact nonlinear relationship between the duty cycle and the output voltage is not important. Since Q2 and Q3 are in high speed common collector and common base configurations respectively, the response of this circuit is fast, and the duty cycle measurement is approximately independent of frequency.

By tuning the oscillation period with R9 so that the output voltage ends up at some fixed reference level, for instance, 1.00V, you will be keeping a fixed relationship between the exponential time constant and the period. Since the decay time con-

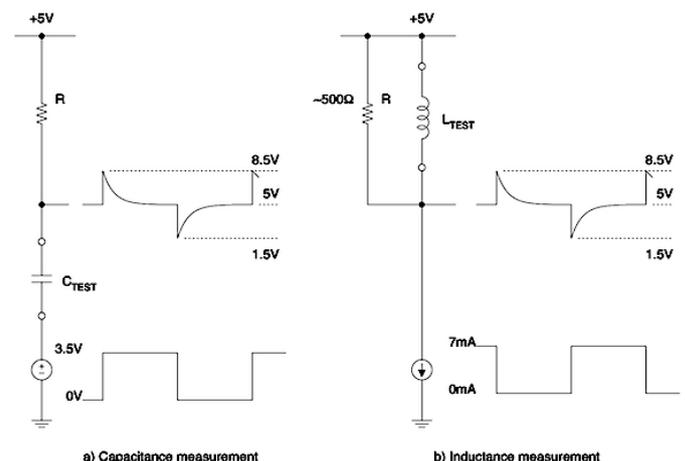


Figure 1. Basic scheme for measuring capacitors and inductors with variable frequency square waves

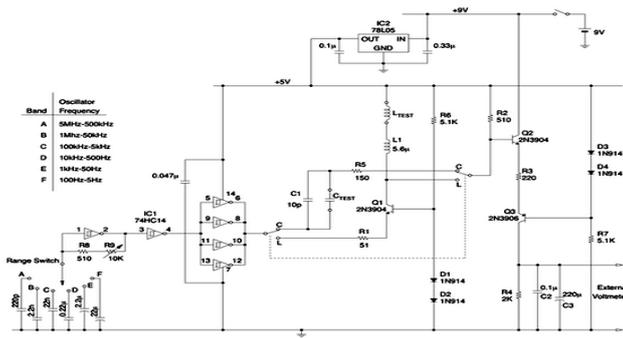


Figure 2. Complete schematic of C and L meter

stant varies linearly with the reactive test component value, the measured capacitance or inductance values will turn out to be linear with respect to the oscillator period, and therefore linear with respect to the shaft angle of R9. By applying a suitable dial marking on R9 and calibrating the circuit with a few known capacitor and inductor values, calibration charts can be plotted that will allow you to determine any test component value. Figure 3 shows the dial marking graphic for R9 that is included in the downloadable example calibration package. The oscillator range switch will cover six decades, although the minimum period is limited by the propagation delay of IC1. This will let you cover the top six orders of magnitude of capacitance or inductance, from low to high values for ranges A through F. Clip the test component into the circuit, find the settings of the range switch and the variable resistor that give 1.00V at the output, and look up the value on the plot corresponding to each range. Range A will let you measure down to about 10 pF or 2 μ H, and range F up to about 10 μ F or 4H. To extend measurements down to about 1 pF and 200 nH, you can use an additional trick. The small offset components C1 and L1 are always contributing a minimum time constant in either 'C' or 'L' mode, and by comparing the change in the voltage read by the external voltmeter when a test device is added to these small offsets, an additional calibration chart can be plotted for the very lowest range of values. The measurement technique for this lowest range is to leave

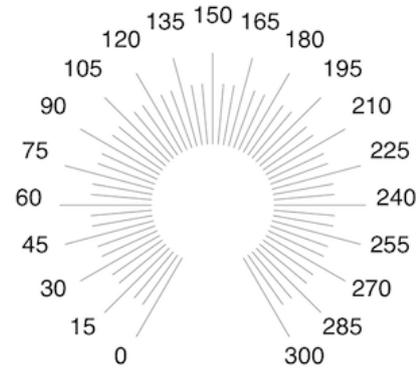
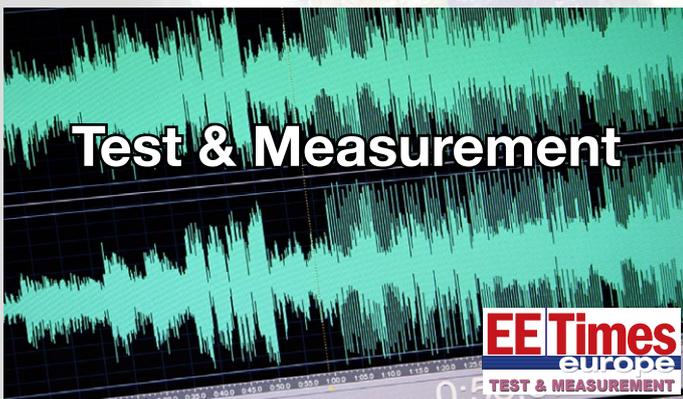


Figure 3. Example dial marking graphic for R9

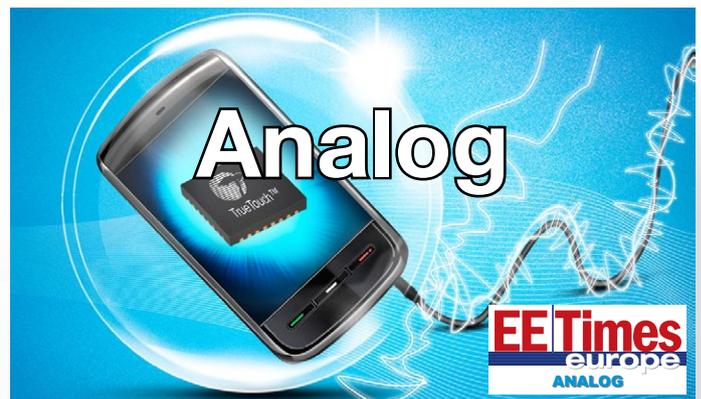
the component under test out of the circuit at first, by either leaving the capacitor test clips open or the inductor test clips shorted. Then set the oscillator to range 'A' and adjust the oscillator period with R9 until you see the target voltage of 1V with only the offset component in the circuit. Finally, insert the test component in the circuit and observe the change in the voltmeter reading. Look up this offset voltage on the calibration chart to determine the small component values. The download [here] contains an example dial scale, some sample calibration plots, and the gnuplot data and script files used to generate them. Within a least squares fit that removes the typical $\pm 10\%$ variation in reactive components, you can see the linearity of the measurements with respect to dial reading over all the ranges. Your calibration will probably vary with different parts, but you can edit the data files and generate your own plots.

Dr. John Fattaruso earned B.S., M.S. and Ph.D. degrees in Electrical Engineering all from the University of California, Berkeley, through 1986. He served Texas Instruments in Dallas as an analogue design engineer from 1987 through 2009, and was elected to Distinguished Member of the Technical Staff. He is now teaching at Southern Methodist University in Dallas as Adjunct Professor of EE and Adjunct Lecturer of Physics.

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www.tm-eetimes.com

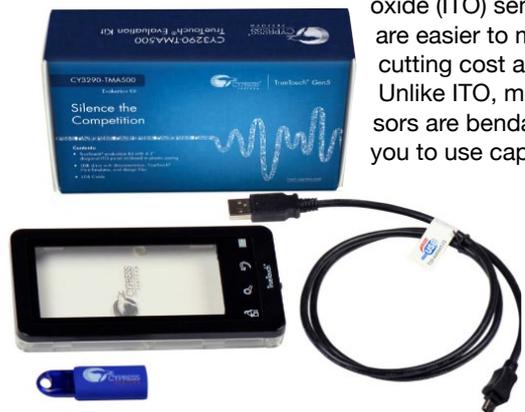


www.analog-eetimes.com

productroundup

Touch sensing on flexible and curved surfaces

CYPRESS SEMICONDUCTOR'S TrueTouch capacitive touch-screen controllers now support metal mesh sensors from Fujifilm. Metal mesh sensors deliver better scanning performance than traditional indium tin oxide (ITO) sensors, and they are easier to manufacture, cutting cost and design time. Unlike ITO, metal mesh sensors are bendable, allowing you to use capacitive touch capability with flexible displays and curved surfaces. Cypress' CY3290-TMA500 and CYTK58 TrueTouch



Evaluation Kits enable you to design with Fujifilm metal mesh sensors and to add the features of the TrueTouch portfolio.

More here, or;
Cypress;
www.cypress.com and
<http://touch.cypress.com>

6A regulator has wired or PMBus setup

INTERSIL'S ZL2102 IS A 6A DIGITAL SYNCHRONOUS step-down DC/DC power regulator, a fully-integrated, auto compensated DC/DC regulator able to support adjustable output voltages of 0.54V to 5.5V operating from input voltages from 4.5V up to 14V with a high level of integration and ease of configurability. The ZL2102 occupies a 6 x 6mm footprint.



Integrated synchronous power MOSFETs deliver continuous loads up to 6A from 4.5V to 14V with high efficiency. The ZL2102 can be completely configured with external pin-strap or resistor settings allowing for setup of all key parameters and adjustment of switching frequency, output voltage, soft-start ramp/delay settings and sequencing options. For more advanced setups, the ZL2102 supports over 70 PMBus commands and can be configured using Intersil's PowerNavigator GUI. In 6 x 6 mm 36-lead QFN package, the device costs \$3.10 (1,000). A demo board, the ZL2102DEMO1Z, is available for \$80.

More here, or;
Intersil;
www.intersil.com/products/ZL2102

Rugged accelerometers for consumer products

ST'S LIS2HH12 ACCELEROMETER INTRODUCES a new internal structure inherently more resilient to mechanical and thermal stress than preceding devices; enhanced robustness provides stability and high performance for advanced mobile functionality in fashionable form factors.

The LIS2HH12 is housed in a 2 x 2 x 1 mm package, giving designers extra flexibility to meet pc-board layout rules for wireless handsets, and helping achieve a low overall handset profile.

The accelerometer has selectable full-scale range of ± 2 , ± 4 or $\pm 8g$ and a 16-bit digital output, an integrated temperature sensor, industry-standard I2C and SPI interfaces, a wide analogue supply-voltage range of 1.71V to 3.6V, and two programmable interrupt generators that help streamline system design. With typical Zero-g level change versus temperature of ± 0.25 mg/C, the stability of the LIS2HH12 has doubled compared with previously announced devices. Also, the rejection versus bending with a typical offset accuracy of ± 30 mg has improved by 25% over the existing solutions.

High-performance
3-axis accelerometer

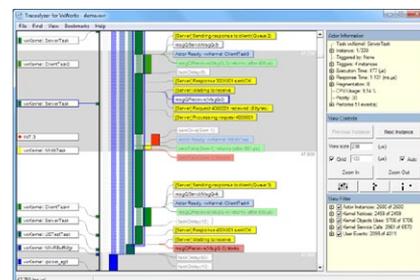


More here, or;
STMicroelectronics;
www.st.com

Tracealyzer for VxWorks and Linux

PERCEPIO (SWEDEN), developer of the visualisation and analysis tool Tracealyzer, has announced versions of the software targeting VxWorks and Linux. Tracing is a common technique for analysing bugs or performance issues in multi-threaded software systems. Tracealyzer visualises traces, providing a level of understanding that allows for faster troubleshooting as well as improved software quality and performance. Tracealyzer for VxWorks visualises traces from the built-in tracing in Wind River VxWorks and is compatible with all VxWorks versions from v5.5. Tracealyzer for Linux visualises traces from LTTng v2.x, supporting most Linux systems from kernel v2.6.32. Tracealyzer for Linux also supports Wind River Linux 5.

Tracealyzer is also available for several other real-time operating systems targeting microcontroller systems, including FreeRTOS, SafeRTOS and Micrium μ C/OS-III.



More here, or;
Percepio;
www.percepio.com

Bluetooth Smart for compact wearable accessories

CSR'S CSR1012 USES CSR μ Energy silicon to create a Bluetooth Smart platform with a small form factor for developers looking to create low-power wearable accessories. CSR1012 is part of the CSR μ Energy range, in a smaller form factor package for smart watches and activity monitors. The platform provides a form factor small enough for wearable devices but still uses standard PCB technology, which allows developers to get a high-volume product to market quickly and cost effectively. It's also the first solution to support direct connection to a lithium-ion battery without the need for an external regulator. This not only saves cost and PCB area, but saves quiescent leakage current in the external regulator. In addition to wearable technology, the solution can also be used for other small form factor 'accessories' and HID accessories, such as slim smartphone or tablet styluses and small advertising beacons.



More here, or;
CSR;
www.csr.com/products/csr101x-product-family

Brushed DC motor drive ICs

TOSHIBA'S TB9101FNG AND TB9102FNG are small-sized brushed DC motor drivers for automotive applications including control of air-conditioner valves and door mirrors. Automotive applications that use small motors require low power consumption driver ICs. The new motor drivers are fabricated with a low power consumption, fine pitch



BiCD process, and have low on-resistance. The respective on-resistances are TB9101FNG: 0.6 Ω (typ.) and TB-9102FNG: 0.5 Ω (typ.). A small sized SSOP24 package (5.6 x 7.8mm) reduces the mounting area to approximately 1/3 that of equivalent products. The ICs integrate

multiple abnormality detection circuits, including overcurrent detection, overtemperature detection, overvoltage detection, and undervoltage detection. The TB9101FNG can drive two motors and TB9102FNG can drive up to six motors, allowing selection to meet the number of motors required for applications.

Toshiba;
www.toshiba-components.com

Safety-certification with Compiler Qualification kit

A KIT SIMPLIFIES COMPILER qualification when creating functionally safe systems; the ARM Compiler Qualification Kit is a documentation package specifically designed to help developers achieve certification against safety standards such as IEC 61508 and ISO 26262. The kit provides evidence of the robustness and maturity of the ARM Compiler toolchain, saving months of effort for users who would otherwise have to create their own evidence for justifying their toolchain selection. The ARM Compiler Qualification Kit can reduce the effort of certifying the software running on these types of products by providing usage guidelines for the safety-critical application developer and validation evidence demonstrating the appropriateness of the ARM Compiler toolchain for safety-related applications.

More here, or; ARM;
<http://ds.arm.com/arm-compiler-qualification-kit>

Soft IP core handles HDLC/SDLC transmission for MCUs

DIGITAL CORE DESIGN (Poland) has introduced the DHDLC soft IP Core, designed to control HDLC/SDLC transmission frame and optimised for a variety of 8, 16 and 32-bit MCUs. As with other DCD IP Cores, the DHDLC is a technology independent design, therefore can be implemented in both ASIC and FPGA. The DHDLC IP core is used for controlling HDLC/SDLC transmission frame, for 8-, 16- or 32-bit microcontrollers, relieving the processor of time spent for handling HDLC/SDLC features, such as bit stuffing, address recognition and CRC computation. To enable greater productivity, DHDLC has a FIFO buffer for both receiver and transmitter. The DHDLC IP Core is fully synchronous with a single clock domain design. All parameters are configurable by CPU, but there is also another option; you can set all the parameters by modification constants in a source file.

More here, or;
DCD:
<http://dcd.pl/ipcore/670/dh-dlc/>

Low RDS(on) 30V MOSFET below 1 mΩ

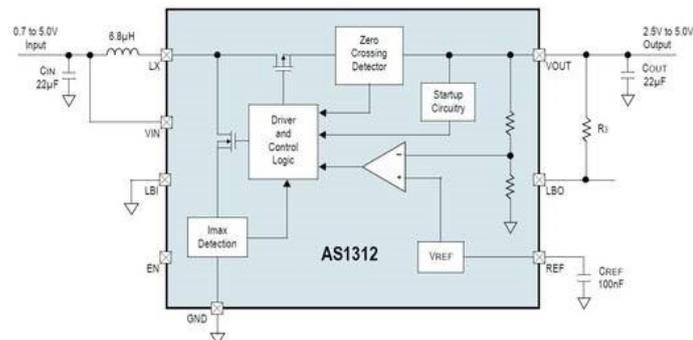
THE AP1A003GMT-HF-3 POWER MOSFET from Advanced Power Electronics (APEC) offers very low maximum on-resistance of only 0.99 mΩ for use in high current load switching. Provided in a PMPAK5x6 package with integrated thermal pad and with a standard SO-8 footprint compatible with other enhanced 5 x 6 mm power packages,

the AP1A003GMT-HF-3 power MOSFET features simple gate drive requirements, a breakdown voltage rating of 30V and a maximum drain-source current rating of 260A. It is fully RoHS-compliant and BFR/halogen-free. Samples are available now.

APEC;
www.a-powerusa.com/docs/AP1A003GMT-3.pdf

DC/DC boost converter has 1 μA quiescent current

AS1312, FROM AMS, is an ultra-low-IQ hysteretic step-up DC-DC converter that achieves an efficiency of up to 94% and is designed to operate from a +0.7V to +5.0V supply, with an output voltage fixed in 50 mV steps from +2.5V to 5.0V. Peak output current is 200mA; it features a shutdown mode, where it draws less than 100 nA and in which the battery is not connected to the output. If the input voltage exceeds the output voltage the device is in a feedthrough mode and the input is directly connected to the output voltage. In light load operation, the device enters a sleep mode, active approximately 50 μsec

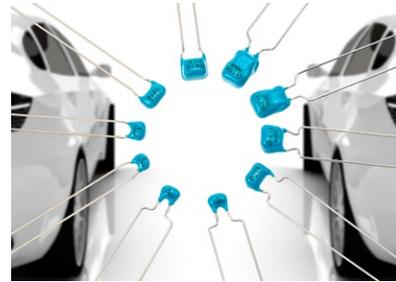


after a current pulse provided that the output is in regulation. The AS1312 also offers an adjustable low-battery detection. If the battery voltage decreases below a threshold defined by two external resistors, the LBO output is pulled to logic low: LBO functions as a power-OK indication when LBI is connected to GND. The AS1312 is available in a 8-pin (2 x 2 mm) TDFN and a 0.4 mm pitch 8-pin WL-CSP package.

ams;
www.ams.com

Automotive-qualified passives

ADDED TO MURATA'S AEC-Q200 qualified multi layer ceramic capacitors (MLCC) aimed at automotive applications are the RCE and RHE series radial leaded MLCCs that fully conform to the automotive environmental stress test requirement AEC-Q200 and conducted surge pulse immunity specification ISO7637-2. The RCE series comprises capacitors in the range 1 pF to 22 μF and working voltage from 25 to 1 kV. Operating temperature range is up to 125C.



With an operating temperature up to 150C the RHE series devices are available with 50 – 100 VDC working voltage and capacitance values from 100 pf to 10 μF. The RHE series is guaranteed to operate in temperatures up to 170C for 100 hours when a temperature mission profile is agreed with Murata in advance. Both series are aimed at high frequency EMI noise suppression in an X/Y filter arrangement.

Murata Europe;
www.murata.eu

3-phase BLDC motor drive IC

A THREE-PHASE BLDC MOTOR GATE DRIVER with power module provides all the power, sensing and protection functions needed to implement a robust, highly-efficient solution. Increased flexibility comes with configurable driver dead-time management, driver blanking-time control, and Over-Current Limit (OCL) for external MOSFETs; the device is suitable for



harsh conditions such as industrial and automotive engine-compartment applications, Microchip says. The MCP8024 operates across a voltage range of 6V to 28V and can withstand transient voltage up to 48V. The device provides high-integration analogue functions, such as three current-sensing operational amplifiers; an over-current comparator; MOSFET drivers and a bidirectional communication interface for a complete motor system design. An adjustable step-down DC-to-DC converter powers a broad range of microcontrollers.

More here, or;
Microchip;
www.microchip.com/get/RTAS

Coherent polymer fibres for remote imaging

OMC, SPECIALIST LED LIGHTING, backlighting and industrial fibre optic transmission component supplier, has a coherent polymer fibre which enables high resolution remote imaging, or the ability to “see around corners” for precise sensing, security and imaging applications. The bundle consists of thousands of individual polymer fibre cores which are arranged

coherently at each end such that the image incident on one fibre face is visible on the other face. OMC notes that the fibre is designed to provide a lower cost solution to remote imaging in applications where the extremely small diameters of coherent glass fibre (such as those used to image inside blood vessels) are not required. The resolution is very high, making the fibre suitable not only for high resolution imaging, but also high precision sensing, remote vision, passive surveillance, and imaging in inaccessible areas. The high tensile strength coherent polymer fibre consists of over 7000 individual pixels for high resolution imaging. 2.0mm and 2.5mm cable diameters are available and the cores are protected by a robust outer protection layer.

OMC;
www.omc-uk.com

1200V, compact gate driver

INFINEON'S 1EDI EICEDRIVER is a compact single-channel gate driver for applications with isolation voltages of up to 1200V. The galvanically isolated driver components are based on the Coreless Transformer Technology, developed by Infineon,

which enables output currents of up to 6A on separate output pins. Infineon aims the driver component at the mass market both in the consumer as well as the industrial area; 1EDI driver ICs are offered in eight variants that can be operated at up to voltages of 1200V and are

designed for use in applications with either IGBTs or MOS-FETs. These EiceDRIVER components are the first driver ICs to achieve a value of 100 kV/ μ sec for the CMTI (common mode transient immunity). Both the MOSFET, as well as one IGBT, drivers supply 6A output current.

More here, or;
Infineon;
www.infineon.com/eicedriver

Safety-compliant tools for Renesas' RX MCUs

IAR EMBEDDED WORKBENCH for RX is now available with certification from TÜV SÜD according to IEC 61508 and ISO 26262. The build chain of IAR Embedded Workbench for RX has been tested and approved according to the requirements on support tools embodied in IEC 61508, as well as the ISO 26262 standard for automotive safety-

related systems. The quality assurance measures applied by IAR Systems and the associated Safety Manual allow application developers to use IAR Embedded Workbench for RX in safety-related software development for each Safety Integrity Level (SIL) according to IEC 61508 and each Automotive Safety Integrity Level (ASIL) of ISO 26262 without further tool qualification. IAR Embedded Workbench for RX is certified by TÜV SÜD.

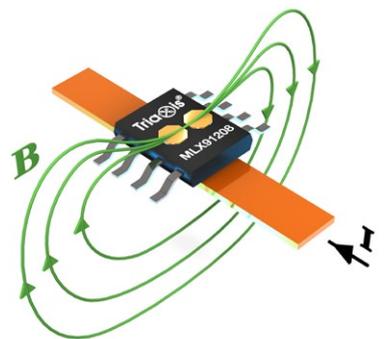


More here, or;
IAR Systems;
www.iar.com/safety
Renesas Electronics Europe;
www.renesas.eu

Programmable Hall effect current sensor for electric vehicles

MELEXIS HAS ADDED TO its customer-programmable Triaxis Hall effect sensor IC range, with a device intended for use in electric vehicles (EVs), hybrid electric vehicles (HEVs) and renewable energy systems; the high speed devices in the MLX91208 series each offer a response time of 3 μ sec.

Accuracy is stable over operational lifespan and temperature, with typical thermal sensitivity drift of ± 150 ppm/ $^{\circ}$ C. The transfer characteristics of the MLX91208 devices are fully adjustable, with parameters such as sensitivity, gain and offset stored on the built-in EEPROM memory. Operational temperature range is -40° C to $+150^{\circ}$ C: the MLX91208 devices are suited to precision DC and AC current measurements up to 200 kHz. Current sensing systems based on the MLX91208 series exhibit accuracy levels exceeding $\pm 0.5\%$ at room temperature or $\pm 2\%$ at the extremes of the specified temperature range.



More here, or;
Melexis;
www.melexis.com/MLX91208

32.768 kHz oscillator quartz replacement technology

SILEGO TECHNOLOGY has introduced its third generation Green-CLK3TM 32.768 kHz oscillator family. At 1x1.6 mm the oscillators are the smallest available in standard plastic packaging. The product family is also available in die form with a total area of less than 0.6 sq mm or 50% smaller than competitive devices. The GCLK3 generation is 50% lower power, 50% improved in ppm accuracy, and greater than a 10 dB improvement in phase noise as compared previous generations. In the lowest power mode with only the 32.768 kHz clock output active, this new generation IC consumes just 0.75 μ A (typical) at tighter ppm accuracy over temperature as compared to tuning fork quartz crystals. In full active mode with both MHz clock and 32.768 kHz outputs active the IC consumes around 0.9 mA with a MHz phase noise of less than -135 dBc/Hz at 1 kHz offset.



consumes just 0.75 μ A (typical) at tighter ppm accuracy over temperature as compared to tuning fork quartz crystals. In full active mode with both MHz clock and 32.768 kHz outputs active the IC consumes around 0.9 mA with a MHz phase noise of less than -135 dBc/Hz at 1 kHz offset.

More here, or;
Silego;
www.silego.com

PMIC for Intel Atom E3800

ROHM SEMICONDUCTOR now has Power Management ICs (PMICs) designed to serve the needs of the Intel Atom processor E3800 family; the BD9596MWW integrates an intelligent power supply core with fast transient load response, along with a 16-channel system power supply consisting of a 2-channel DC/DC controller, 3-channel DC/DC regulator, 2-channel IMVP7 Lite controller, 8-channel LDO, and 1-channel Load switch – in a single 10mm² package. This eliminates the need for users to develop and verify their own complex power solution that requires complicated sequences and associated circuit design, with multiple analogue components, in a larger PCB area.



More here, or;
Rohm;
www.rohm.co/eu

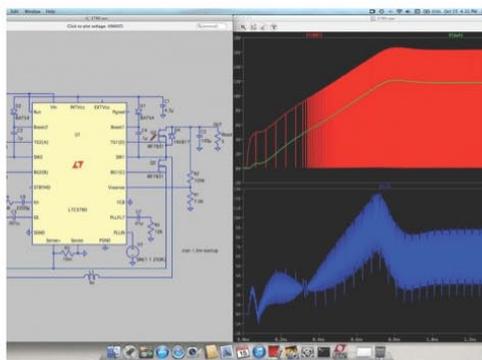
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ANALOG

LTspice IV runs native on Mac OS X

Linear Technology has a native Mac OS X release of its LTspice IV simulation program. This new release of LTspice supports Mac OS X 10.7+ platforms and has similar capabilities and features to those of its Windows counterpart.

Floating switch architecture simplifies offline LED drive

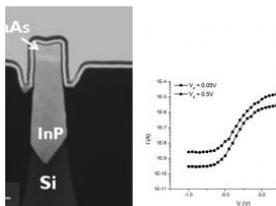
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Xbox One hardware costs less to make than retail price – but not by much

A teardown by industry analysts IHS has concluded that the combined hardware and manufacturing cost of Microsoft's new Xbox One amounts to \$471, suggesting that Microsoft is subsidising the cost of the video game console at the time of launch.

IHS' teardown estimates the bill of materials (BOM) for the Xbox One at \$457, with manufacturing estimated at \$14, which means the console's total cost of \$471 is only \$28 less than the retail price of \$499.

This is very similar, IHS continues, to the new PlayStation 4 from Sony, which carries a hardware and manufacturing cost of only \$18 lower than its retail price, according to the preliminary IHS teardown information on that product. And just like the PlayStation 4, Microsoft initially will take a loss on each Xbox One sold when other expenses are added into the equation – with sales of games providing profitability.

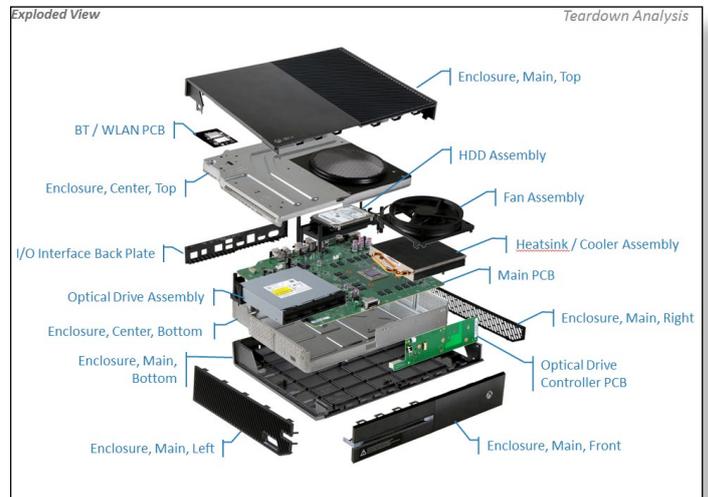
"The Xbox One is designed to serve as a beachhead in the home for Microsoft, with the console's capability to interact with—and interface to—other devices, such as televisions, set-top boxes, smartphones and tablets," Steve Mather, senior principal analyst for IHS noted. "Gaining such a strategic advantage in the battle to control the connected home and Internet-enabled living room is well worth having the Xbox One act as a loss leader for Microsoft."

Table 1 presents the preliminary BOM and manufacturing cost estimate of the Xbox One and the PlayStation 4. Note that these teardown assessments are preliminary in nature, and account only for hardware and manufacturing costs.

AMD TAKES THE LEAD IN GAMING

The Xbox One's core architecture is very similar to the PlayStation 4, with most of the functionality of the two systems residing in highly integrated system-on-chip (SOC) devices supplied by Advanced Micro Devices.

According to Andrew Rassweiler, senior director, IHS teardown service, "Although the AMD chips are unique in the two consoles, they appear very similar in many ways. Both chips are built in 28-nanometer-process geometry, have the same number of CPU cores, and possess similar silicon die surface area between the two, suggesting similar amounts of functionality and processing power. Even the net power requirements for the



two consoles are very much alike, which further underscores functional similarity. The two consoles are not clones, but are definitely related."

KINECT: THE XBOX ONE'S NOT-SO-SECRET SAUCE

The biggest factor increasing the hardware cost of the Xbox One compared to the PlayStation 4 is Microsoft's inclusion of the new-generation Kinect system as a standard feature of its console. The Kinect adds an estimated \$75 to the Xbox One's BOM and manufacturing cost.

IHS has determined that Microsoft has made significant advances in the Kinect hardware since the first version of the device examined by its Teardown Analysis Service in 2010.

In the intervening years, Microsoft has added new features, including new optics for the system's two cameras that are larger and more sophisticated than for the previous generation. The more advanced optics should provide better images to the sensor, but are more expensive. The three infrared emitters in the new version of the Kinect also contain some elaborate optics that IHS is still analysing.

AMD INSIDE

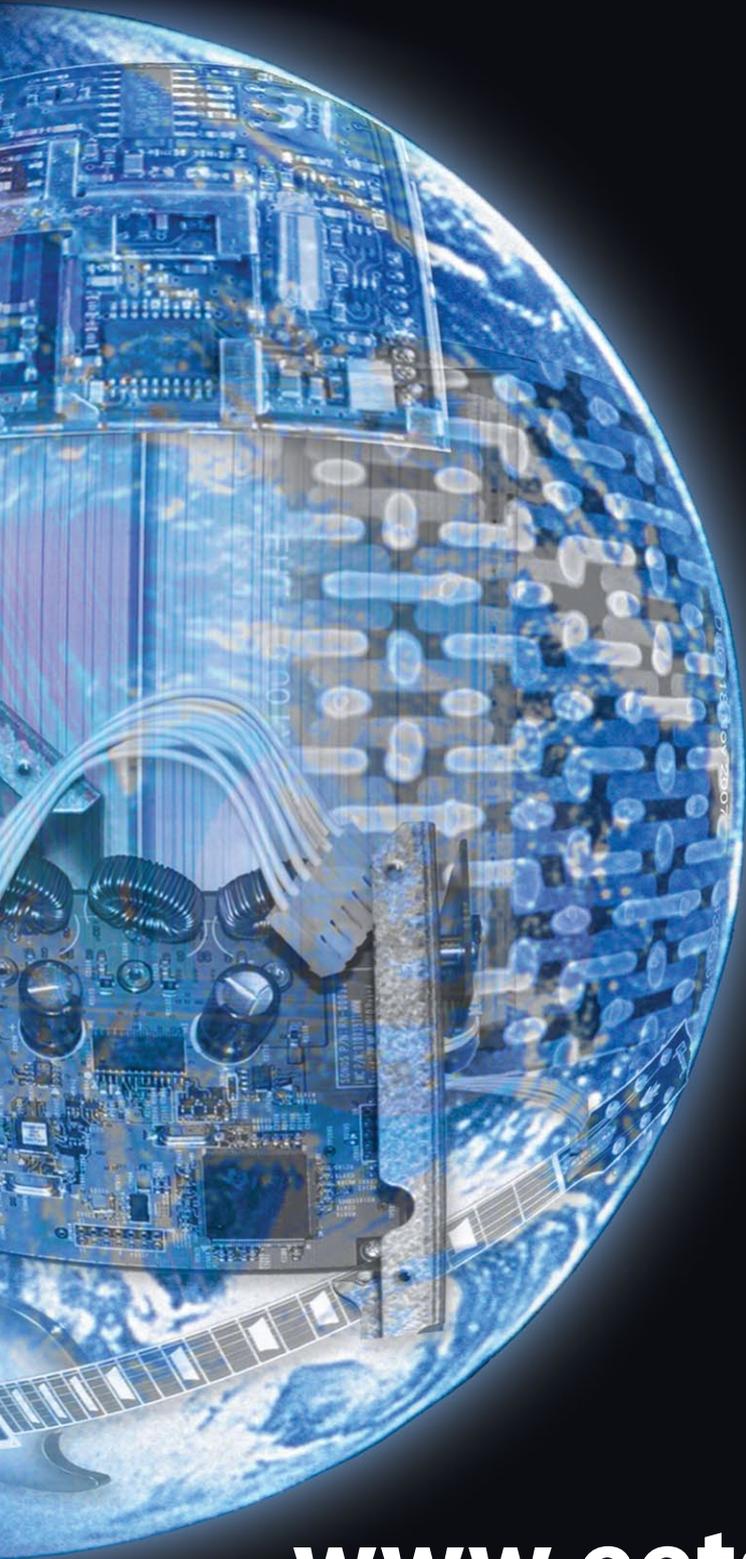
Like the PlayStation 4, the Xbox One is based on a highly integrated SoC processor from AMD that performs the vast majority of the functions in the console. In each system, the AMD processor is essentially a "console-on-a-chip," combining the CPU and GPU into a single device, as well as integrating other functions.

And just as the Xbox One and PlayStation 4 are related but aren't clones: the two chips in the two consoles are not exactly alike.

Preliminary modelling from IHS suggests that the AMD chip in the Xbox One should cost about 10% more than the device it sells to Sony for the PS4. The AMD processor in the Xbox One is estimated at \$110, compared to \$100 for the PlayStation 4.

A longer version of this item, with more graphics, is here. IHS; www.ihs.com

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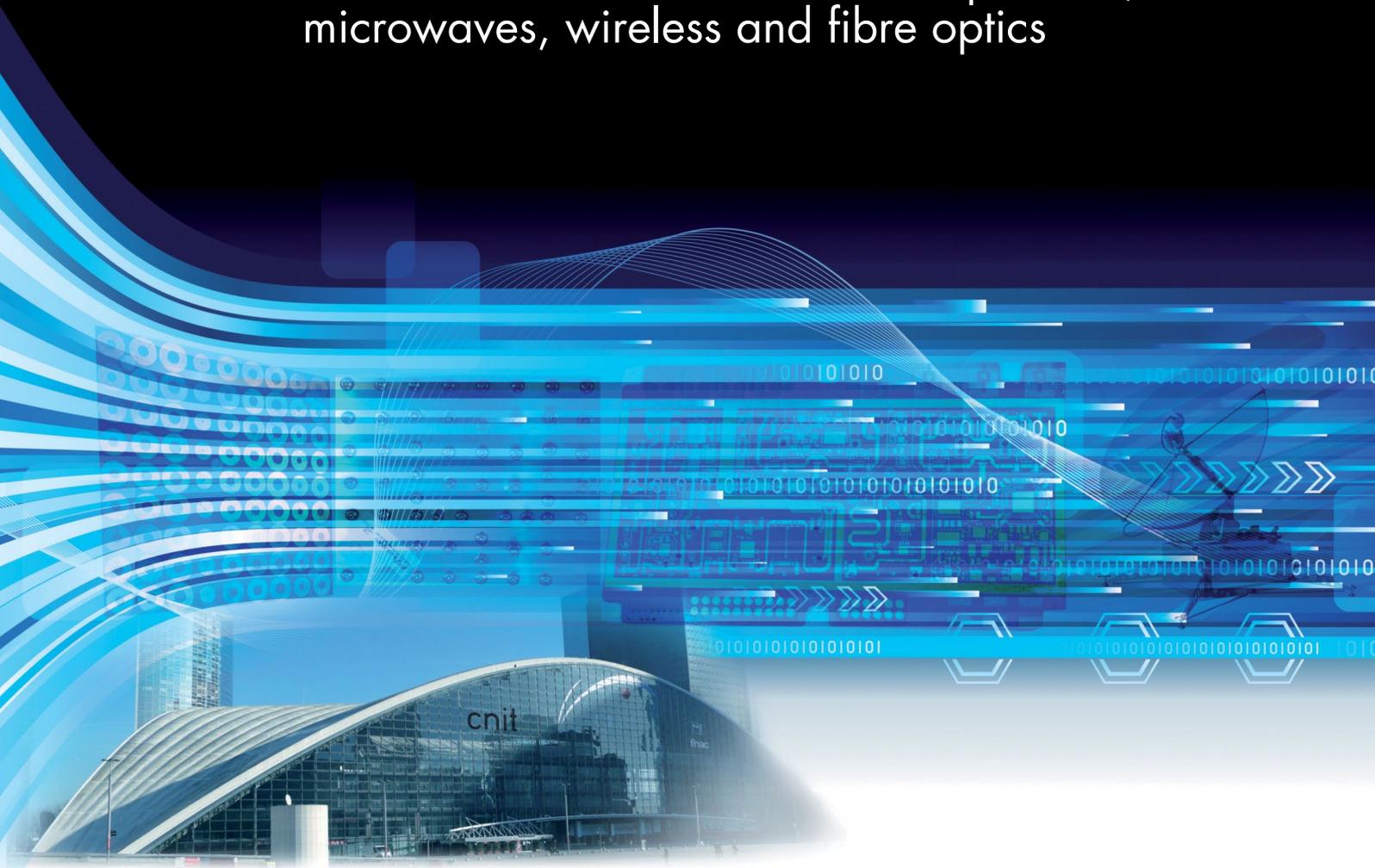
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