Design Example Report

Title	***Low Profile, Low Standby Consumption 27 W Power Supply Using TNY380PN***
Specification	90 VAC – 265 VAC Input; 5 V, 2.5 A and 14.5 V, 1 A Outputs
Application	LCD Monitor
Author	Applications Engineering Department
Document Number	DER-229
Date	August 17, 2009
Revision	1.0

Summary and Features

- Low cost, low parts count solution
  - TinySwitch®-PK TNY380PN-based solution
  - No heatsink required
- Highly energy efficient
  - Very low standby consumption
    - Input power of 82 mW with 30 mW output load, 264 VAC input
  - Input power <100 mW at no-load, 230 VAC input
  - High full-load efficiency
    - >80% efficiency at 90 VAC
- Temperature rise meets requirements of LCD monitors
  - TNY380PN plastic <78°C (90 VAC, 60 Hz, 25°C ambient)
- Conducted EMI margin >8 dB

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a two-output (5 V, 2.5 A, and 14.5 V, 1 A) power supply utilizing a TNY380PN from the TinySwitch-PK family of ICs.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

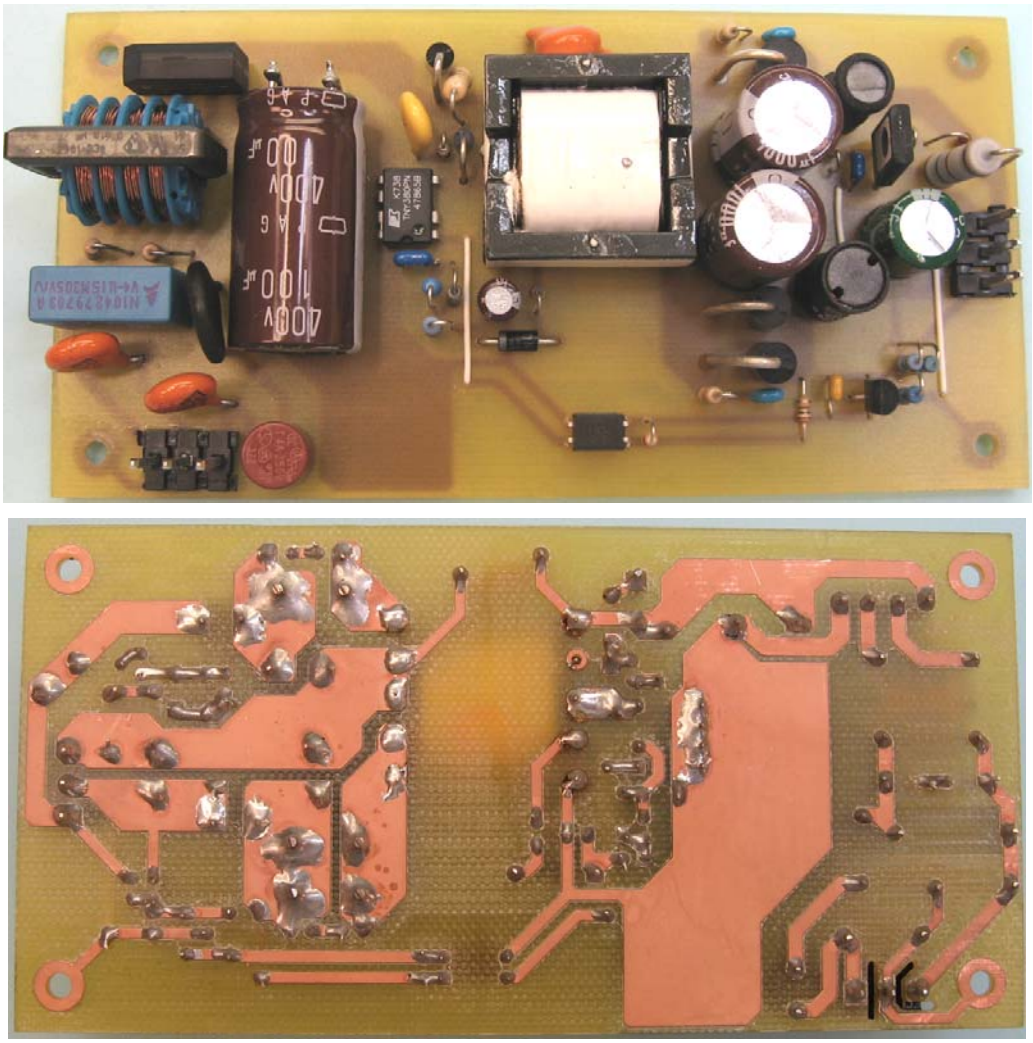

Figure 1 – Populated Board.

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire – with P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (264 VAC)			110	<0.2	W	
Output						
Output Voltage 1	V_{OUT1}		5		V	
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	
Output Current 1	I_{OUT1}	0		2.5	A	
Output Voltage 2	V_{OUT2}		14.5		V	
Output Ripple Voltage 2	$V_{RIPPLE2}$			200	mV	20 MHz bandwidth
Output Current 2	I_{OUT2}	0		1	A	
Total Output Power						
Continuous Output Power	P_{OUT}			27	W	
Efficiency						
Full Load (90VAC)	η	80			%	Measured at P_{OUT} 25°C
Required Average Efficiency at 25, 50, 75, and 100 % of P_{OUT}	η_{CEC}	N/A			%	Per California Energy Commission (CEC) / Energy Star requirements
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				Output return connected to PE (chassis)
Safety		Designed to meet IEC950, UL1950 Class II				
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

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3 Schematic

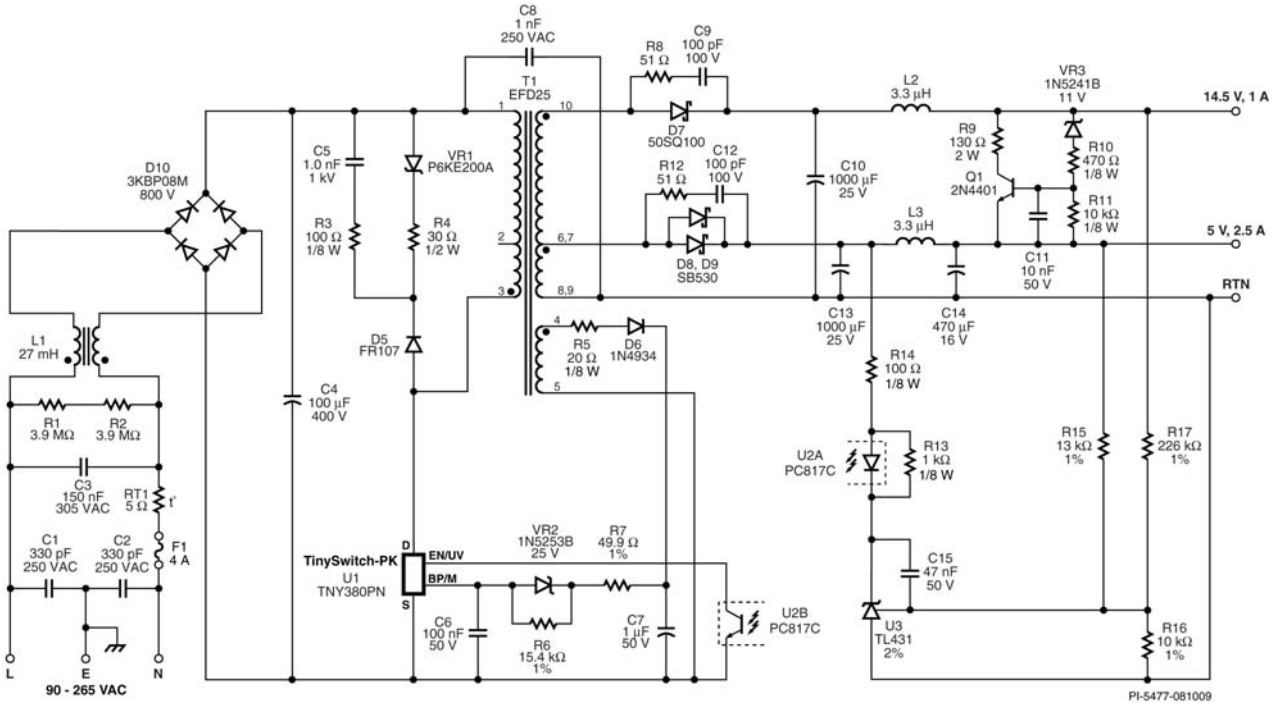

Figure 2 – Schematic.

4 Circuit Description

The power supply employs a TinySwitch-PK TNY380PN device (U1) with an integrated high-voltage MOSFET and a controller in a flyback configuration.

4.1 Input EMI Filtering and Rectification

Capacitors C1, C2, and C3, together with common-mode choke L1, form an RC filter that attenuates both common-mode and differential-mode conducted EMI. Diode Bridge D10 rectifies the AC input. For safety consideration, resistors R1 and R2 must be used to discharge the capacitor C3 when the AC input is disconnected.

4.2 TinySwitch-PK Primary

The TNY380PN device (U1) integrates an oscillator, a switch controller, startup and protection circuitry, and a power MOSFET, all on one monolithic IC. One side of the power transformer (T1) primary winding is connected to the positive side of the bulk capacitor C4, and the other side is connected to the DRAIN pin of U1. At the start of a switching cycle, the controller turns on the MOSFET and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold, the controller turns off the MOSFET. Due to phasing of the transformer windings and the output diode orientation, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor. When the MOSFET turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The amplitude of that spike is limited by an RCDZ clamp network that consists of D5, R3, R4, C5, and VR1. In this arrangement, VR1 limits the voltage across R3 and C5 and also prevents the voltage across C5 from discharging completely during light load operation, thereby reducing losses and improving efficiency.

Using ON/OFF control, U1 skips switching cycles to regulate the output voltage, based on feedback to its EN/UV pin. Prior to each switching cycle, the EN/UV pin current is sampled to determine if that switching cycle should be enabled or disabled. If the EN/UV pin current is <115 μA, the next switching cycle begins; the cycle is terminated when the current through the MOSFET reaches the internal current limit threshold or the DC_{MAX} signal is encountered. A state-machine within the controller adjusts the MOSFET current limit threshold, depending on the load being demanded from the supply. As the load on the supply drops, the current limit threshold is reduced. This ensures that the effective switching frequency stays above the audible range until the transformer flux density is low.

The TinySwitch-PK also has a peak power mode, at which it can supply additional output power to the load for short periods of time. If the MOSFET switching occurs for 14 consecutive clock cycles (132 kHz), the I_{LIMIT} increases and the MOSFET is enabled to switch at 264 kHz. While in peak power mode, if the MOSFET is disabled (via the feedback loop) for 12 consecutive clock cycles (264 kHz), then the TinySwitch-PK reverts back to its normal operating mode at 132 kHz. In this design, U1 is working at peak

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power mode most of the time with pulse skipping, so that the effective switching frequency with pulse skipping can still be sufficiently high to minimize the audible noise frequency components.

Audible noise is eliminated by packing the transformer gap with gap filler, gluing the core junction, and heating the transformer before dip varnishing.

The BP pin is also used for programmable current limit setting. With capacitor C6 of 0.1 μF connected at the BP pin, the TNY380PN is working at standard current limit mode.

4.3 Output Rectification

Diodes D8 and D9 rectify the 5 V secondary winding output of T1. Output voltage is filtered by C13, L3, and C14. Resistor R12 and capacitor C12 absorb the noise caused by the commutation of D8 and D9. Diode D7 rectifies the 14.5 V secondary winding output of T1. Output voltage is filtered by C10 and L2. Resistor R8 and capacitor C9 absorb the noise caused by the commutation of D7.

4.4 Output Feedback

The supply's output voltage regulation is set by voltage dividers formed by R15, R17, and R16, and the shunt regulator U3. When the output voltages rise above the set points, the LED in U2 becomes forward biased. On the primary side, the photo-transistor of U2 turns on and draws current out of the EN/UV pin of U1. Just before the start of each switching cycle, the controller checks the EN/UV pin current to determine whether the switching cycle should be enabled and disabled so that the output voltages are kept very close to the regulation set points.

To improve output cross regulation an active bleeder circuit was used. This is formed by R9, R10, R11, Q1, C11, and VR3. As the 14.5 V output rises, transistor Q1 is biased, which then feeds current from the 14.5 V output to the 5.1 V output. This limits the maximum voltage difference between 5.1 V and 14.5 V outputs.

4.5 Output Overvoltage Shutdown

The TinySwitch-PK family of ICs can detect overvoltage on the supply output and latch off. This protects the load in an open feedback loop fault condition, such as the failure of the optocoupler. Overvoltage on the output is detected through the BP/M pin and the bias winding on the transformer. The bias winding voltage is determined by the reflection of the output voltage through the turns ratio of the transformer. Therefore, an overvoltage on the output will be reflected onto the bias winding. The overvoltage threshold is the sum of the breakdown voltage of Zener diode VR2 and the BP/M pin voltage (25 V + 5.8 V). If the output voltage becomes abnormally high, the voltage on the bias winding will exceed the threshold voltage and excess current will flow into the BP/M pin. The latching shutdown feature is activated when current into the BP/M pin exceeds 7 mA.

4.6 TNY380 BP Pin Supply with Bias Winding

Besides overvoltage protection, the bias winding also supplies the IC consumption of U1 via the BP pin. Ultra-low no-load or very light load consumption was achieved by selecting the minimum number of bias winding turns to provide a bias voltage of 8 V at zero load and adjusting the value of resistors R6 and R7 to provide a current into the BP equal to or just above the IC consumption.

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5 PCB Layout

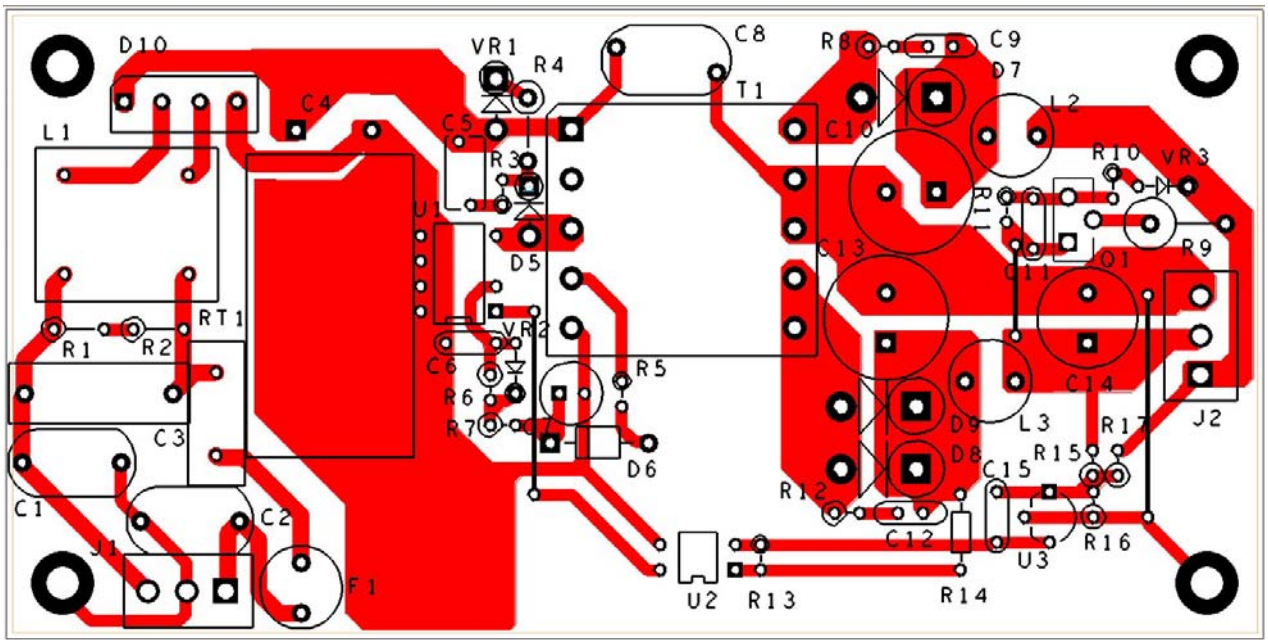

Figure 3 – PCB Layout (5 x 2.5 inches / 127 x 63.5 mm).

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	2	C1 C2	330 pF, 250 VAC, Film, X1Y1	CD70-B2GA221KYAS	TDK
2	1	C3	150 nF, 305 VAC, X2	B32922A2154M	Epcos
3	1	C4	100 µF, 400 V, Electrolytic, Low ESR (16 x 30)	EPAG401ELL101ML30S	Nippon Chemi-Con
4	1	C5	0.001 µF, 1 kV, Disc Ceramic	562R10TSD10	Vishay
5	1	C6	100 nF, 50 V, Ceramic, X7R	RPER71H104K2K1A03B	Murata
6	1	C7	1 µF, 50 V, Electrolytic, Gen. Purpose (5 x 11)	EKMG500ELL1R0ME11D	Nippon Chemi-Con
7	1	C8	1 nF, Ceramic, Y1	440LD10-R	Vishay
8	2	C9 C12	100 pF, 100 V, Ceramic, COG	B37979N1101J000	Epcos
9	2	C10 C13	1000 µF, 25 V, Electrolytic, Very Low ESR, 21 mΩ (12.5 x 20)	EKZE250ELL102MK20S	Nippon Chemi-Con
10	1	C11	10 nF, 50 V, Ceramic, COG	B37986G5103J054	Epcos
11	1	C14	470 µF, 16 V, Electrolytic, Very Low ESR, 53 mΩ (10 x 12.5)	EKZE160ELL471MJC5S	Nippon Chemi-Con
12	1	C15	47 nF, 50 V, Ceramic, X7R	B37981F5473K000	Epcos
13	1	D5	1000 V, 1 A, Fast Recovery Diode, DO-41	FR107-T-F	Diodes Inc.
14	1	D6	100 V, 1 A, Fast Recovery, 200 ns, DO-41	1N4934	Vishay
15	1	D7	100 V, 5 A, Schottky, DO-201AR	VS-50SQ100	Vishay
16	2	D8 D9	30 V, 5 A, Schottky, DO-201AD	SB530	Vishay
17	1	D10	800 V, 3 A, Bridge Rectifier, Glass Passivated	3KBP08M-E4/51	Vishay
18	1	F1	4 A, 250V, Slow, TR5	3721400041	Wickman
19	2	J1 J2	3 Position (1 x 3) Header, 0.156 Pitch, Vertical	26-48-1031	Molex
20	1	L1	27 mH, 0.9 A, Common Mode Choke	B82732-R2901-B30	Epcos
21	1	L2	3.3 µH, 5.7 A	ELC08D3R3E	Panasonic
22	1	L3	3.3 µH, 5.5 A	RL622-3R3K-RC	JW Miller
23	4	MTG_ HOLE	Mounting Hole No. 4		
24	1	Q1	NPN, Small Signal BJT, 40 V, 0.6 A, TO-92	2N4401	Vishay
25	2	R1 R2	3.9 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-3M9	Yageo
26	2	R3 R14	100 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-100R	Yageo
27	1	R4	30 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-30R	Yageo
28	1	R5	20 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-20R	Yageo
29	1	R6	15.4 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-15K4	Yageo
30	1	R7	49.9 Ω, 1%, 1/4 W, Metal Film	MFR-25FBF-49R9	Yageo
31	2	R8 R12	51 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-51R	Yageo
32	1	R9	130 Ω, 5%, 2 W, Metal Oxide	RSF200JB-130R	Yageo
33	1	R10	470 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-470R	Yageo
34	1	R11	10 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-10K	Yageo
35	1	R13	1 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-1K0	Yageo
36	1	R15	13 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-13K0	Yageo
37	1	R16	10 kΩ, 1%, 1/4 W, Metal Film	ERO-S2PHF1002	Panasonic
38	1	R17	226 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-226K	Yageo
39	1	RT1	NTC Thermistor, 5 Ω, 2.8 A	CL160	Thermometrics
40	1	T1	Bobbin, EFD25, Horizontal, 10 Pins	B66422-B1010-D1	Epcos
41	1	U1	TinySwitch-PK, TNY380PN, DIP-8C	TNY380PN	Power Integrations
42	1	U2	Optocoupler, 35 V, CTR 200-300%, 4-DIP	PC817C	Sharp
43	1	U3	2.495 V Shunt Regulator IC, 2%, 0 to 70 °C, TO-92	TL431CLPG	On Semiconductor
44	1	VR1	200 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE200ARLG	On Semiconductor
45	1	VR2	25 V, 5%, 500 mW, DO-35	1N5253B	Microsemi
46	1	VR3	11 V, 5%, 500 mW, DO-35	1N5241B	Microsemi

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7 Transformer Specification

7.1 Electrical Diagram

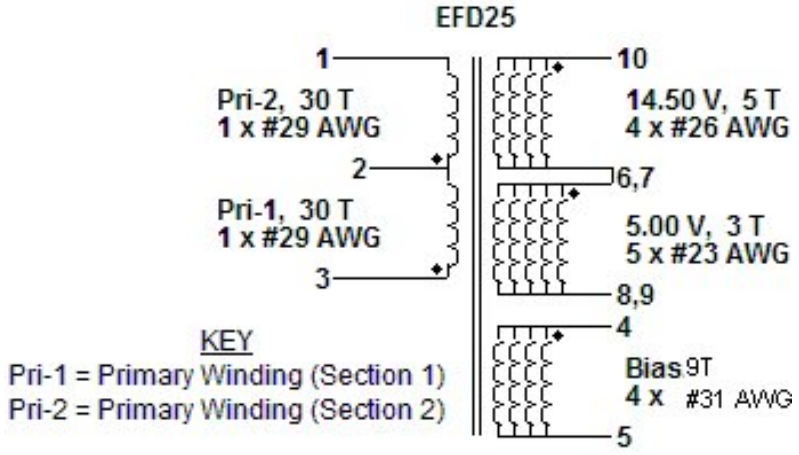

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-5 to pins 6-10	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 VRMS	518 µH, ±5%
Resonant Frequency	Pins 1-3, all other windings open	400 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins 6, 7, 8, 9, and 10 shorted, measured at 100 kHz, 0.4 VRMS	20 µH (Max.)

7.3 Materials

Item	Description
[1]	Core: EFD25, NC-2H (Nicera) or equivalent, gapped for ALG of 144 nH/t²
[2]	Bobbin 5+5 pins: Epcos part number B66422-B1010-D1
[3]	Tape: Polyester web 3.00 mm wide
[4]	Barrier tape: Polyester film (1 mil base thickness), 16.40 mm wide
[5]	Teflon tubing #22
[6]	Varnish
[7]	Magnet wire: #29 AWG, solderable double coated
[8]	Magnet wire: #31 AWG, solderable double coated
[9]	Magnet wire: #23 AWG, solderable double coated
[10]	Magnet wire: #26 AWG, solderable double coated
[11]	CHOMERICS T644 compound form-in-place gap filler
[12]	LOCTITE 409 glue

7.4 Transformer Build Diagram

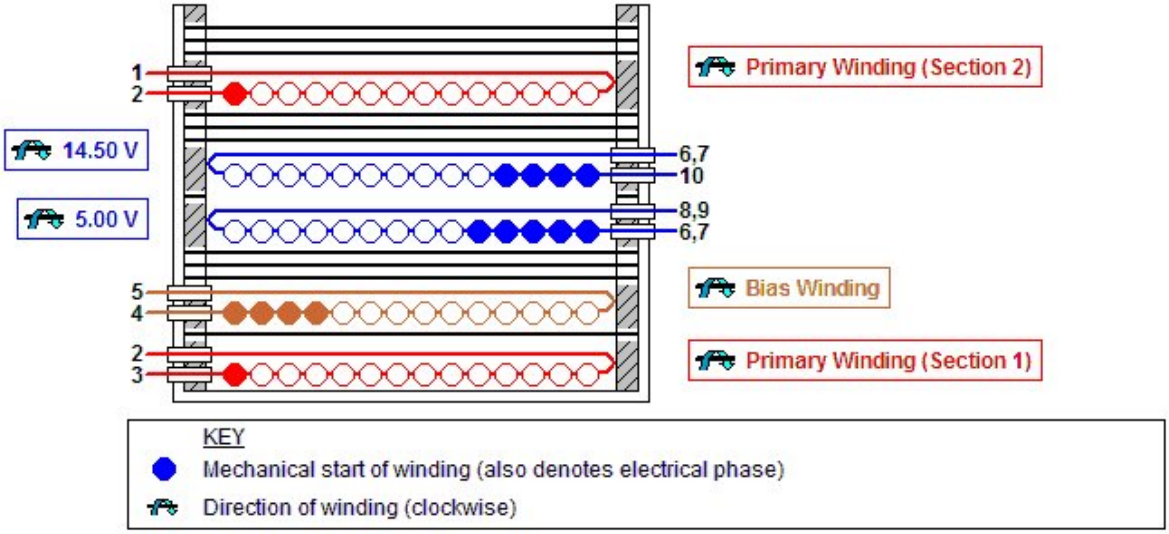

Figure 5 – Transformer Build Diagram.

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7.5 Transformer Construction

WD1 First Half of Primary	Use 3.00 mm margin (Item [3]) on the left side. Use 3.00 mm margin (Item [3]) on the right side. Start on pin 3 using Item [5] at the start leads and wind 30 turns (x 1 filar) of Item [7] in one layer from left to right. Spread the winding evenly across the entire bobbin. Finish this winding on pin 2 using Item [5] at the finish lead.
Basic Insulation	Add one layer of tape (Item [4]) for insulation.
WD2 Bias Winding	Use 3.00 mm margin (Item [3]) on the left side. Use 3.00 mm margin (Item [3]) on the right side. Start on pin 4 using Item [5] at the start leads and wind nine turns (x 4 filar) of Item [8]. Wind in the same rotational direction as the primary winding. Spread the winding evenly across the entire bobbin. Finish this winding on pin 5 using Item [5] at the finish leads.
Reinforced Insulation	Use three layers of tape (Item [4]) for insulation.
WD3 Secondary Winding 5 V	Use 3.00 mm margin (Item [3]) on the left side. Use 3.00 mm margin (Item [3]) on the right side. Start on pins 6 and 7 using Item [5] at the start leads and wind three turns (x 5 filar) of Item [9]. Spread the winding evenly across the entire bobbin. Wind in the same rotational direction as the primary winding. Finish this winding temporarily on pin 1. After WD4 Secondary Winding 14.5 V is finished, bring the wire back and finish at pins 8 and 9 using Item [5] at the finish leads.
WD4 Secondary Winding 14.5 V	Use 3.00 mm margin (Item [3]) on the left side. Use 3.00 mm margin (Item [3]) on the right side. Start on pin 10 using Item [5] at the start leads and wind five turns (x 4 filar) of Item [10]. Spread the winding evenly across the entire bobbin. Wind in the same rotational direction as the primary winding. Finish this winding on pins 6 and 7 using Item [5] at the finish leads.
Reinforced Insulation	Use three layers of tape (Item [4]) for reinforced insulation.
WD6 Second Half of Primary	Use 3.00 mm margin (Item [3]) on the left side. Use 3.00 mm margin (Item [3]) on the right side. Start on pin 2 using Item [5] at the start leads and wind 30 turns (x 1 filar) of Item [7] in one layer from left to right. On the final layer, spread the winding evenly across the entire bobbin. Finish this winding on pin 1 using Item [5] at the finish leads.
Outer Wrap	Wrap the windings with three layers of tape (Item [4]).
Core Preparation	Prepare the core to get the correct primary inductance.
Final Assembly	Apply Item [11] to fill the center gap area. Assemble and secure the core halves with tape and apply Item [12] at the sides of junctions of the core halves.
Varnishing	Heat the transformer to 100°C in oven for 30 minutes. Dip varnish the transformer in Item [6].

8 Transformer Design Spreadsheet

ACDC_ TinySwitch-PK_ 032608; Rev.1.5; © 2008 Power Integrations	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-PK_032608_ Rev1-5.xls; TinySwitch-PK Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					**Customer**
VACMIN	90			V	Minimum AC input voltage
VACMAX	265			V	Maximum AC input voltage
fL	60			Hz	AC mains frequency
VO	5.00			V	Output voltage (at continuous power)
Peak Load Current, IO	6.57			A	Power supply output current (corresponding to peak power)
Peak Power		***Warning***	32.85	W	!!! Warning. Output power exceeds maximum capability of the chosen device in the chosen configuration. Choose larger device or higher current limit.
Continuous / Average Power	27		27	W	Continuous/average output power. Used in estimation of core size.
n	0.80				Efficiency estimate at output terminals. Use 0.7 if no better data available.
Z	0.50		0.5		Z factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.6 if no better data available.
tC	3.00			ms	Bridge rectifier conduction time estimate
CIN	100.00		100	µF	Input capacitance
ENTER TinySwitch-PK VARIABLES					
TinySwitch-PK	**TNY380**		**TNY380**		User defined TinySwitch-PK
Chosen Device		*TNY380*			
Chose Configuration	**STD**		Standard Current Limit		Choose "RED" for reduced current limit (sealed adapters), "STD" for standard current limit, or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.907	A	Minimum current limit
ILIMITTYP			0.975	A	Typical current limit
ILIMITMAX			1.043	A	Maximum current limit
fSmin			248000	Hz	Minimum device switching frequency
I^2fmin			225.87	A^2kHz	Minimum I^2f (current limit squared and frequency trimmed for tighter tolerance)
PO_132kHz			26.26	W	Estimated maximum power while still in 132 kHz operation
VOR	110.00		110	V	Reflected output voltage (VOR < 135 V recommended)
VDS			10	V	TinySwitch-PK on-state drain–to-source voltage
VD			0.5	V	Output winding diode forward voltage drop
KP			0.42		Ripple to peak current ratio (KP < 6)
KP_TRANSIENT			0.25		Transient ripple to peak current ratio; ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			17.00	V	Bias winding voltage
VDB			0.70	V	Bias winding diode forward voltage drop
NB			9.27		Bias winding number of turns
R_BIAS			7.15	kΩ	Bias winding resistor to externally power TinySwitch-PK
VZOV			23.00	V	Overvoltage protection Zener diode
UVLO VARIABLES					
V_UV_TARGET			119.59	V	Target undervoltage threshold, above which the power supply will start

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ACDC_ TinySwitch-PK_ 032608; Rev.1.5; © 2008 Power Integrations	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-PK_032608_ Rev1-5.xls; TinySwitch-PK Continuous/Discontinuous Flyback Transformer Design Spreadsheet
V_UV_ACTUAL			118.20	V	Typical start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			4.70	MΩ	Calculated value for UV Lockout resistor
RUV_ACTUAL			4.64	MΩ	Closest standard value of resistor to RUV_IDEAL
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EFD25**		**EFD25**		User-defined core size (verify thermal performance under continuous/average load conditions)
Core		*EFD25*		*P/N:*	EFD25-3F3
Bobbin		*EFD25_ BOBBIN*		*P/N:*	EFD25_BOBBIN
AE			0.58	cm^2	Core effective cross-sectional area
LE			5.7	cm	Core effective path length
AL			1800	nH/T^2	Ungapped core effective inductance
BW			16.4	mm	Bobbin physical winding width
M	3.00		3	mm	Safety margin width (half the primary–to-secondary creepage distance)
L	2.00		2		Number of primary layers
NS	3		3		Number of secondary turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			109	V	Minimum DC input voltage
VMAX			375	V	Maximum DC input voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.53		Duty ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.42	A	Average primary current
IP			0.91	A	Minimum peak primary current
IR			0.38	A	Primary ripple current
IRMS			0.61	A	Primary RMS current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			518	µH	Typical primary inductance. ±5% to ensure a minimum primary inductance of 493 µH
LP_TOLERANCE	5.00		5	%	Primary inductance tolerance
NP			60		Primary winding number of turns
ALG			144	nH/T^2	Gapped core effective inductance
BM			1854	Gauss	Maximum operating flux density at maximum primary inductance and maximum current limit; BM<3100 is recommended
BAC			389	Gauss	AC flux density for core loss curves (0.5 × peak-to-peak)
ur			1408		Relative permeability of ungapped core
LG			0.47	mm	Gap length (Lg > 0.1 mm)
BWE			20.8	mm	Effective bobbin width
OD			0.35	mm	Maximum primary wire diameter including insulation
INS			0.06	mm	Estimated total insulation thickness (= 2 * film thickness)
DIA			0.29	mm	Bare conductor diameter
AWG			29	AWG	Primary wire gauge (rounded to next smaller standard AWG value)
CM			128	Cmils	Bare conductor effective area in circular mils
CMA_PEAK			211	Cmils	Primary winding current capacity under peak load condition (200 < CMA < 500)
CMA			249	Cmils/A	Primary winding current capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS (LUMPED PARAMETERS)					

ACDC_ TinySwitch-PK_ 032608; Rev.1.5; © 2008 Power Integrations	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-PK_032608_ Rev1-5.xls; TinySwitch-PK Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ISP			18.14	A	Peak secondary current
ISRMS			11.47	A	Secondary RMS current
IRIPPLE			9.40	A	Output capacitor RMS ripple current
CMS			2294	Cmils	Secondary bare conductor minimum circular mils
AWGS			16	AWG	Secondary wire gauge (rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			626	V	Maximum drain voltage estimate (assumes 20% Zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			24	V	Output rectifier maximum peak inverse voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
First Output					
VO1	5.00		5	V	Main output voltage (if unused, defaults to single output design)
IO1	2.50		2.500	A	Output DC current (enter peak value)
PO1			12.50	W	Output power
VD1			0.5	V	Output diode forward voltage drop
NS1			3.00		Output winding number of turns
ISRMS1			4.364	A	Output winding RMS current
IRIPPLE1			3.58	A	Output capacitor RMS ripple current
PIVS1			24	V	Output rectifier maximum peak inverse voltage
Recommended Diodes			**SB530**		Recommended diodes for this output
CMS1			873	Cmils	Output winding bare conductor minimum circular mils
AWGS1			20	AWG	Wire gauge (rounded up to next larger standard AWG value)
DIAS1			0.81	mm	Minimum bare conductor diameter
ODS1			3.47	mm	Maximum outside diameter for triple-insulated wire
Second Output					
VO2	14.50			V	Output voltage
IO2	1.00			A	Output DC current (enter peak value)
PO2			14.50	W	Output power
VD2			0.7	V	Output diode forward voltage drop
NS2			8.29		Output winding number of turns
ISRMS2			1.745	A	Output winding RMS current
IRIPPLE2			1.43	A	Output capacitor RMS ripple current
PIVS2			66	V	Output rectifier maximum peak inverse voltage
Recommended Diode			**SB380**		Recommended diodes for this output
CMS2			349	Cmils	Output winding bare conductor minimum circular mils
AWGS2			24	AWG	Wire gauge (rounded up to next larger standard AWG value)
DIAS2			0.51	mm	Minimum bare conductor diameter
ODS2			1.25	mm	Maximum outside diameter for triple-insulated wire
Total Power		***Warning***	27	W	Total power does not match calculated PO at top of sheet
Negative Output			N/A		If negative output exists, enter output number (e.g., if VO2 is negative output, enter 2)

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NOTE:
The transformer was designed to deliver a peak power of 35 W, higher than the 27 W specification. This artificially increased the primary inductance value so that under peak load conditions the effective switching frequency was reduced (increased pulse skipping). This also resulted in a warning in the spreadsheet, as the output power is higher than recommended for a current limit selection of ‘standard,’ but can be ignored as the actual output power is within the recommended range.

9 Performance Data

All measurements performed at room temperature. Unless otherwise specified, all testing performed with a line frequency of 50 Hz except for 115 VAC where 60 Hz was used.

9.1 Full Load Efficiency

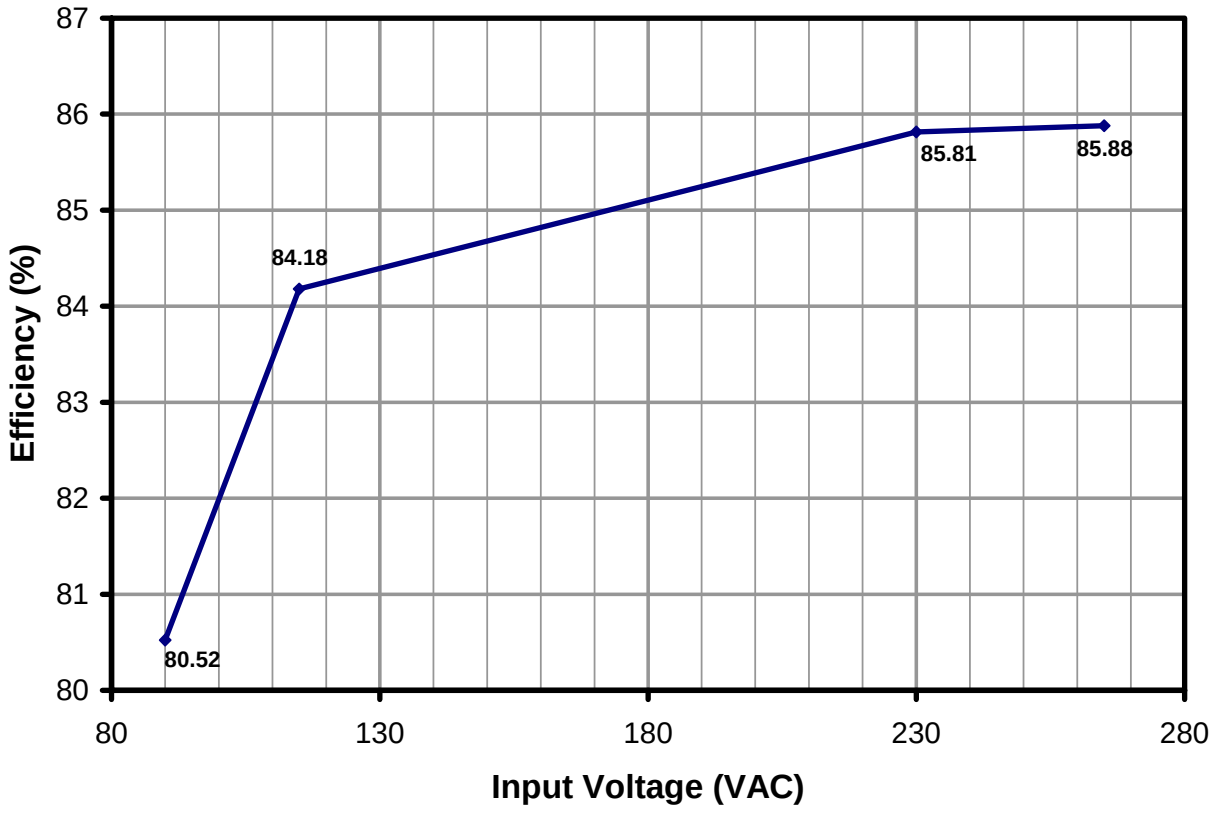

Figure 6 – Efficiency vs. Input Voltage, 60 Hz, Full Load, Room Temperature.

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9.2 Input Power with 25 mW, 30 mW, and 44 mW Load at 5.1 V Output

14.5 V output unloaded

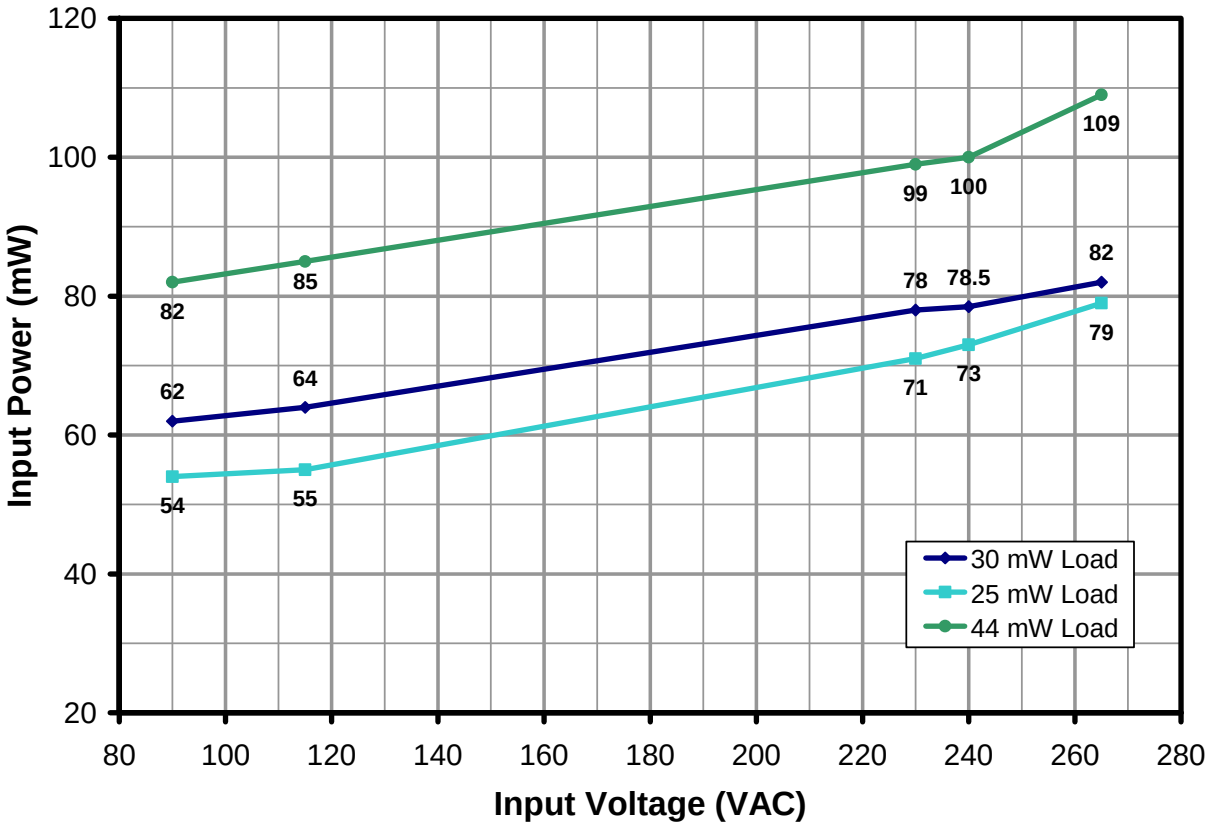

Figure 7 – Input Power with 25 mW, 30 mW, and 44 mW Load at 5 V Output vs. Line Voltage.

9.3 No-load Input Power

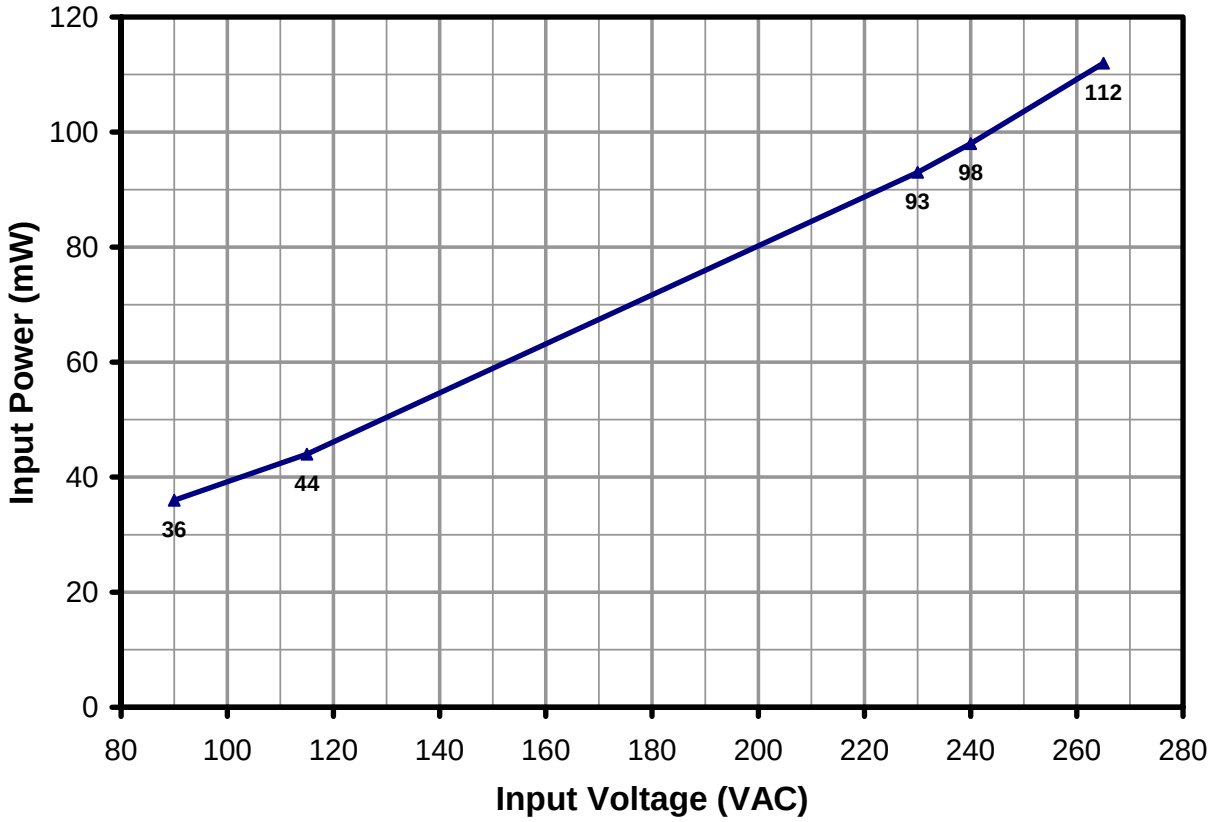

Figure 8 – No-load Input Power vs. Line Voltage.

The value of the no-load input power can be further reduced by optimizing the value of R6; the value as presented was optimized to give the lowest input power during standby operation when a small output load is present.

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9.4 Input Power vs. Available Output Power at 230 VAC

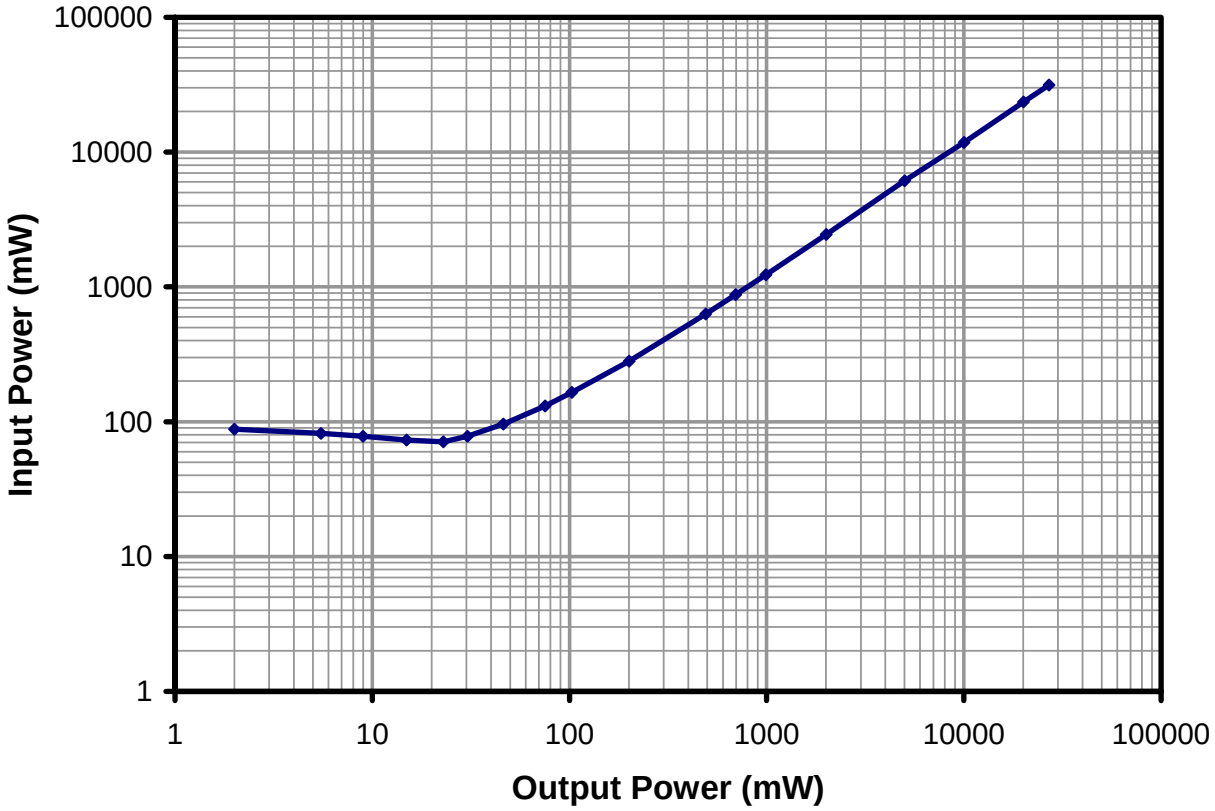

Figure 9 – Input Power vs. Available Output Power Measured at 230 VAC.

9.5 Regulation

9.5.1 Load

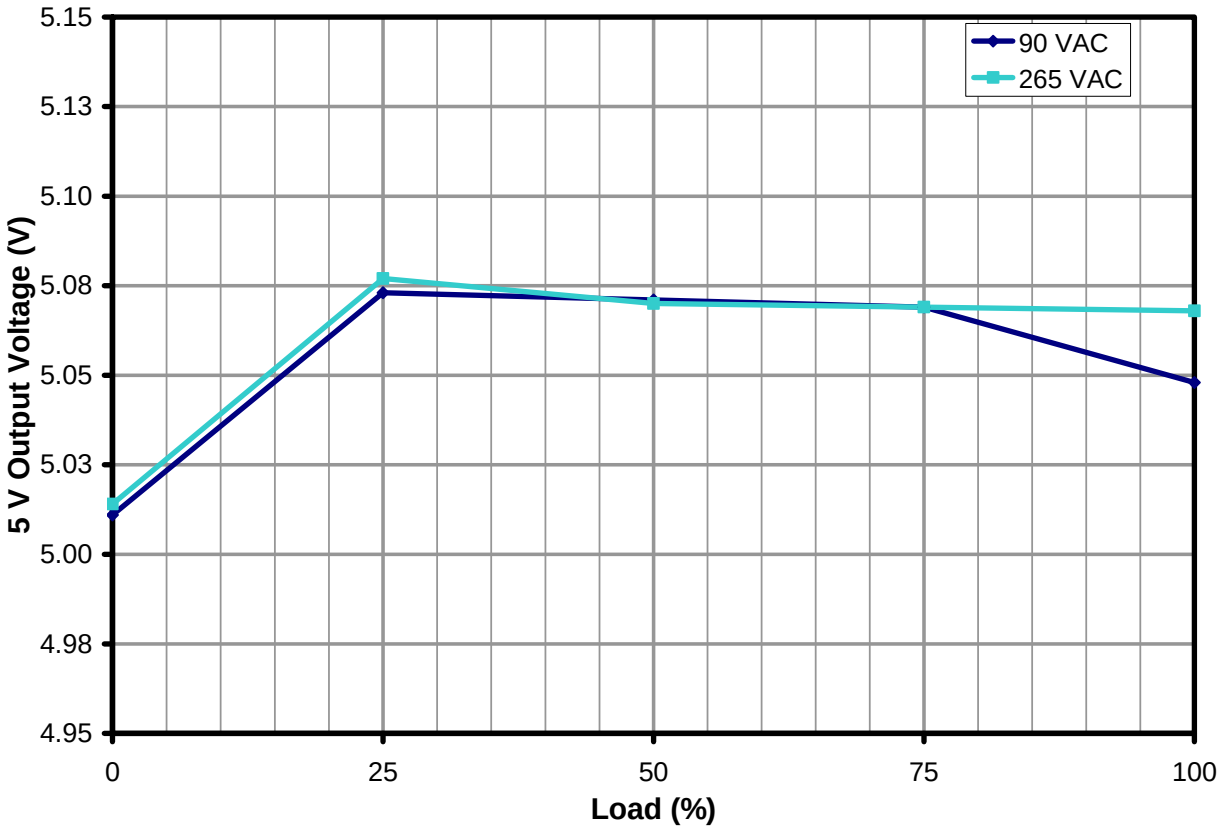

Figure 10 – 5 V Output Load Regulation, Room Temperature.

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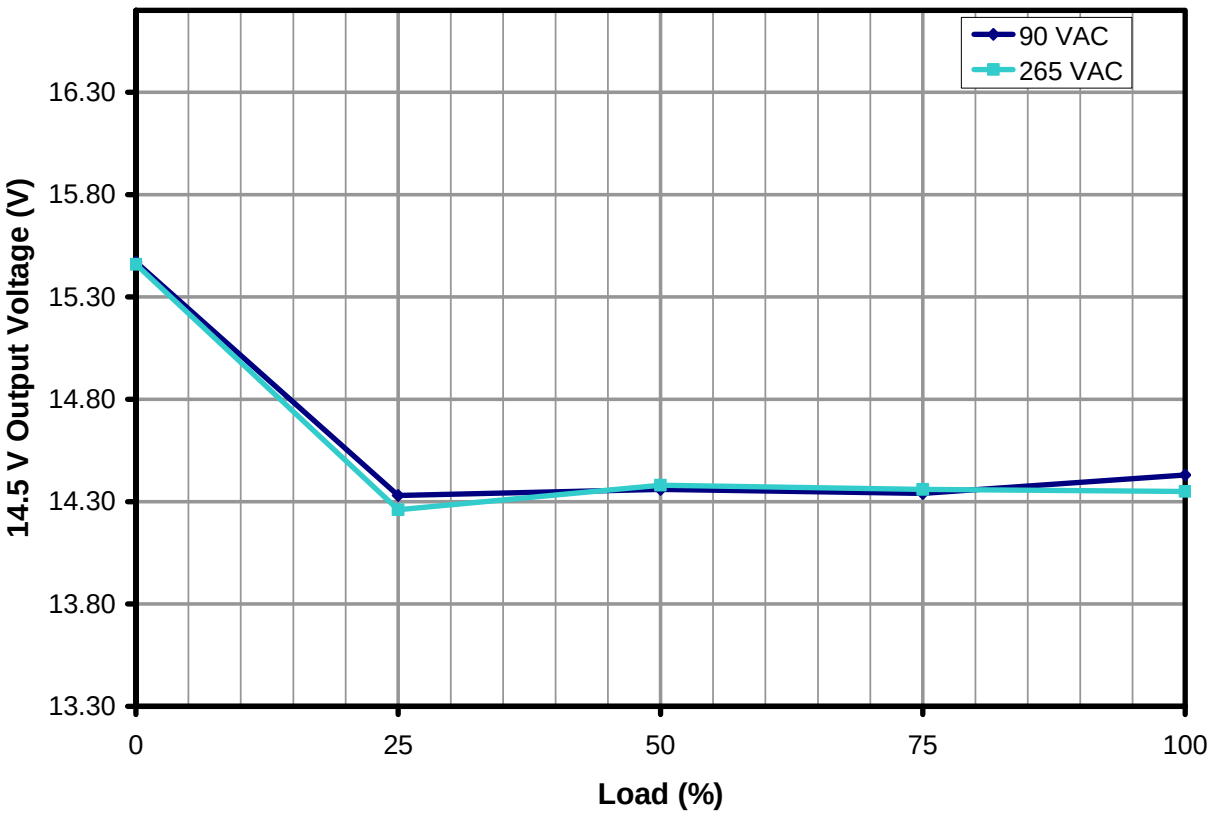

Figure 11 – 14.5 V Output Load Regulation, Room Temperature.

9.5.2 Line

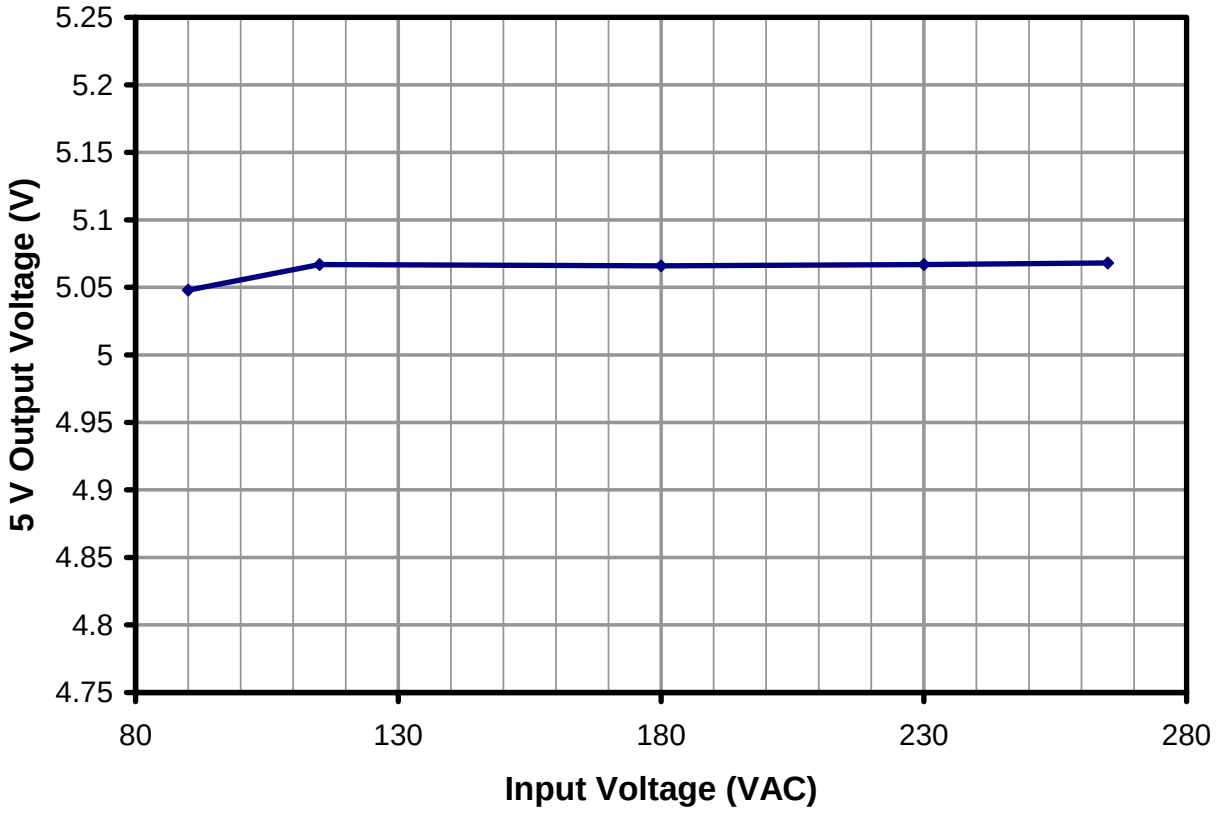

Figure 12 – 5 V Output Line Regulation, Room Temperature, Full Load.

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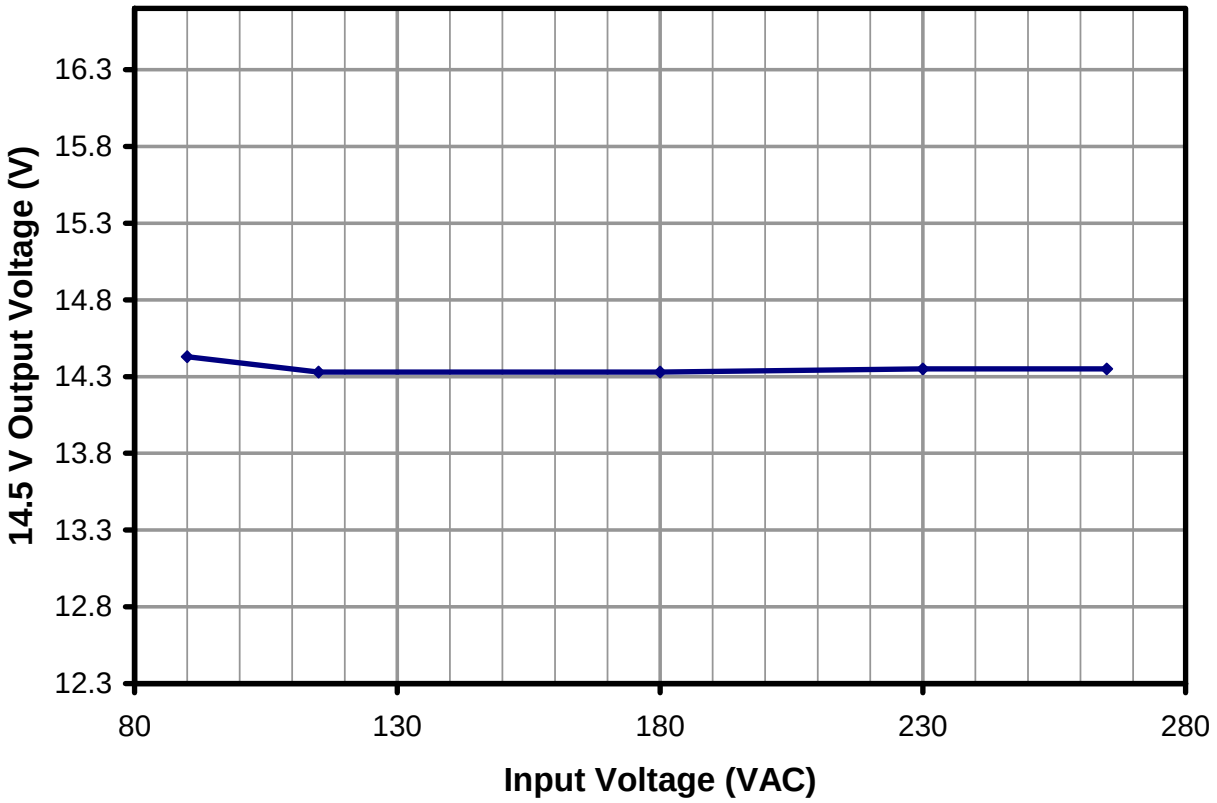

Figure 13 – 14.5 V Output Line Regulation, Room Temperature, Full Load.

9.5.3 Cross Regulation

	90 VAC		265 VAC	
	5 V OUT (V)	14.5 V OUT (V)	5 V OUT (V)	14.5 V OUT (V)
14.5 V / 1 A, 5 V / 2.5 A	5.05	14.43	5.07	14.35
14.5 V / 0 A, 5 V / 0 A	5.01	15.47	5.01	15.46
14.5 V / 0.1 A, 5 V / 2.5 A	5.02	15.10	5.01	15.44
14.5 V / 1 A, 5 V / 0.1 A	5.11	13.75	5.11	13.73

10 Thermal Performance

The unit ran for two hours at an output load of 27 W to warm-up prior to measurements being taken.

Item	Temperature (°C)
	90 VAC / 60 Hz
Ambient	25
Common-Mode Choke(L1)	63
Bridge (D10)	67
Transformer (T1) Core	55
Transformer (T1) Winding	58
***PI Device* (U1)**	77
Rectifier for 5 V (D8)	63
Rectifier for 14.5 V (D7)	58
Thermistor (RT1)	79

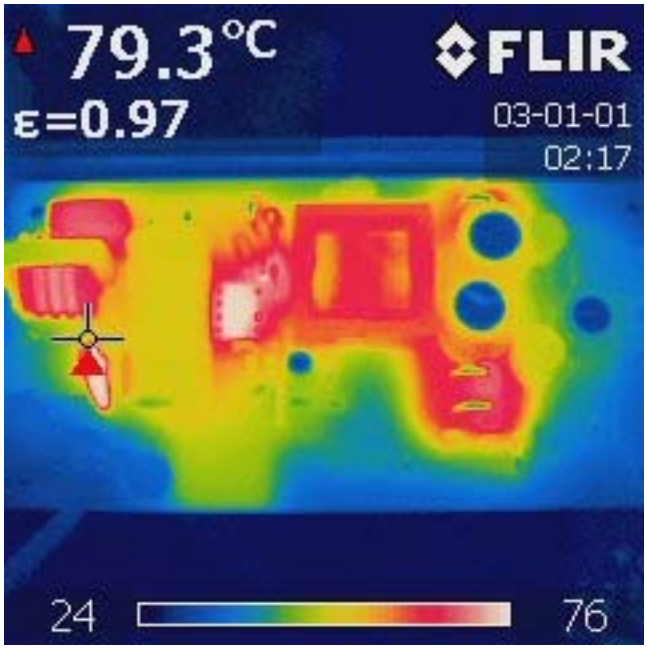

Figure 14 – Infrared Image of the Components Side After Two Hours Operation at Full Load, 90 VAC 60 Hz and Room Temperature Open Frame.

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

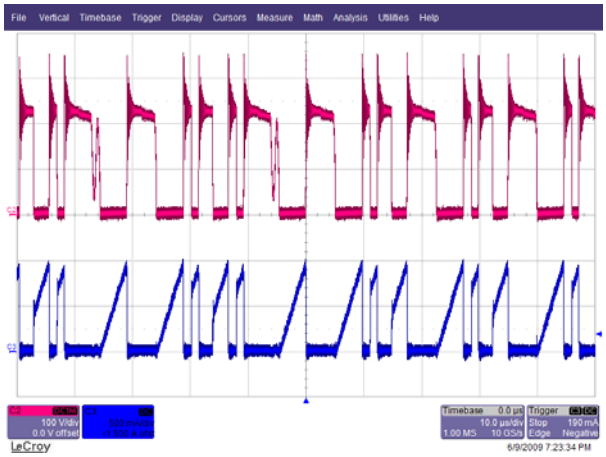

Figure 15 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.5 A, 10 µs / div.

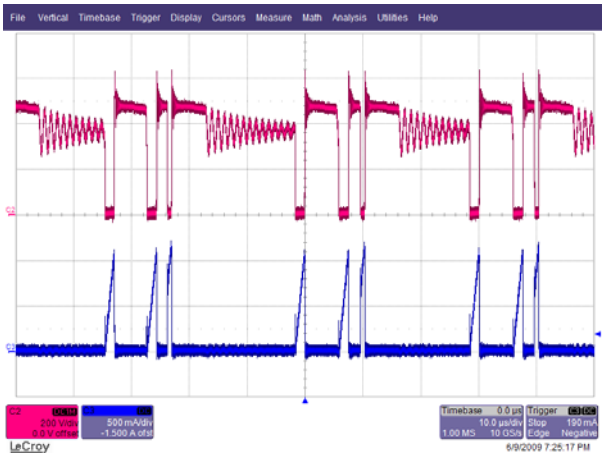

Figure 16 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A, 10 µs / div.

11.2 Output Voltage Start-up Profile

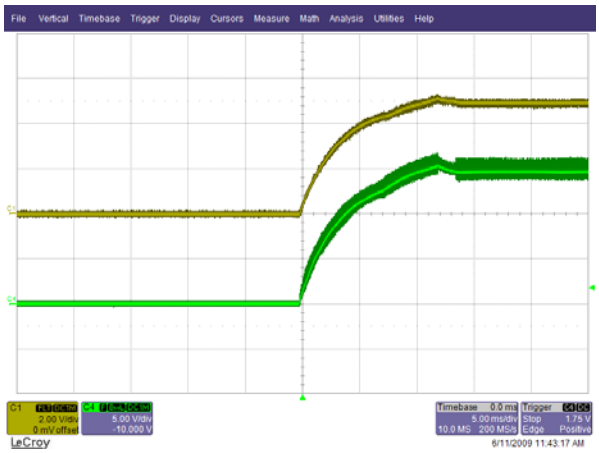

Figure 17 – Start-up Profile, 90 VAC.
Upper: $V_{5\,V}$, 2 V / div.
Lower: $V_{14.5\,V}$, 5 V, 5 ms / div.

Figure 18 – Start-up Profile, 265 VAC.
Upper: $V_{5\,V}$, 2 V / div.
Lower: $V_{14.5\,V}$, 5 V, 5 ms / div.

11.3 Drain Voltage and Current Start-up Profile

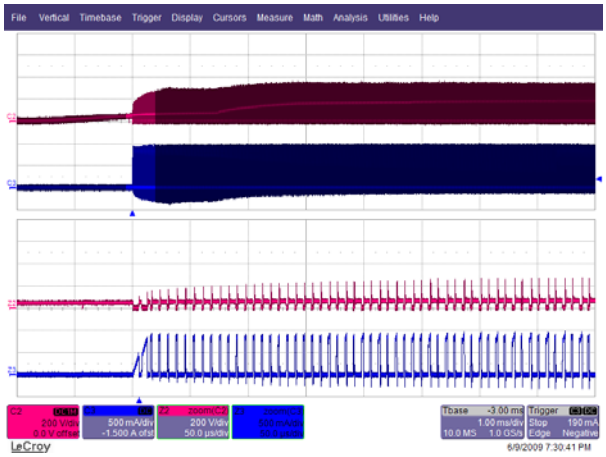

Figure 19 – 90 VAC Input and Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A ,1 ms / div.

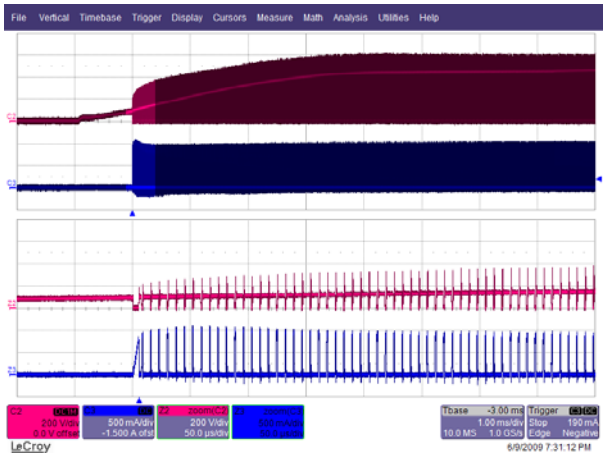

Figure 20 – 265 VAC Input and Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A ,1 ms / div.

11.4 Load Transient Response (75% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

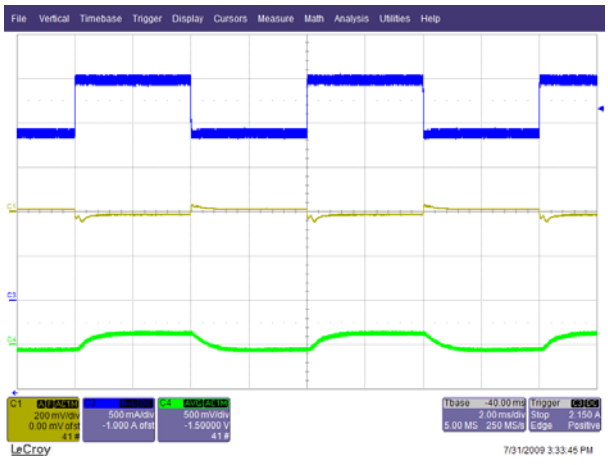

Figure 21 – Transient Response, 90 VAC,
75-100-75% Load Step at 5 V Output.
Top: Output Current, 500 mA / div.
Middle: 5 V Output, 200 mV / div.
Bottom: 14.5 V Output, 500 mV
2 ms / div.

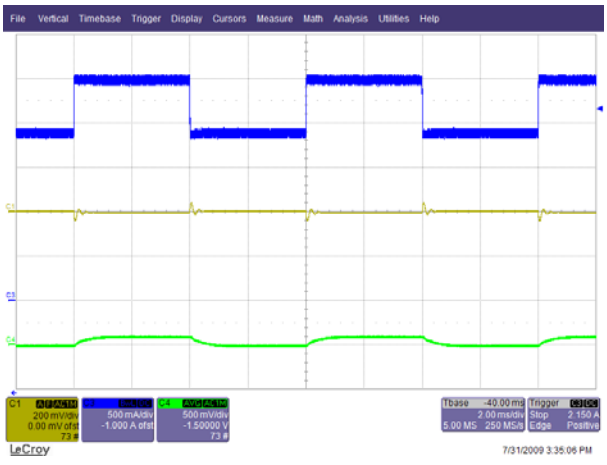

Figure 22 – Transient Response, 265 VAC,
75-100-75% Load Step at 5 V Output.
Top: Output Current, 500 mA / div.
Middle: 5 V Output, 100 mV / div.
Bottom: 14.5 V Output, 500 mV
2 ms / div.

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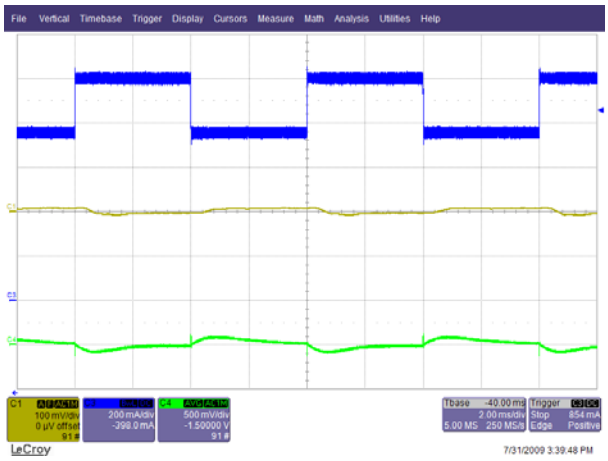

Figure 23 – Transient Response, 90 VAC,
75-100-75% Load at 14.5 V Output.
Top: Output Current, 200 mA / div.
Middle: 5 V Output, 100 mV / div.
Bottom: 14.5 V Output, 500 mV
2 ms / div.

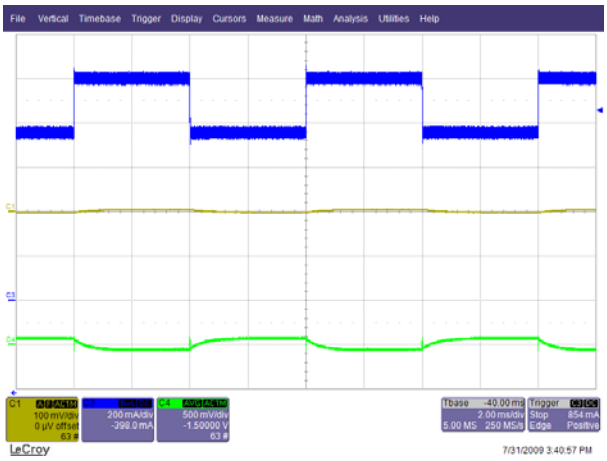

Figure 24 – Transient Response, 265 VAC,
75-100-75% Load at 14.5 V Output.
Top: Output Current, 200 mA / div.
Middle: 5 V Output, 100 mV / div.
Bottom: 14.5 V Output, 500 mV
2 ms / div.

11.5 Output Overvoltage Protection

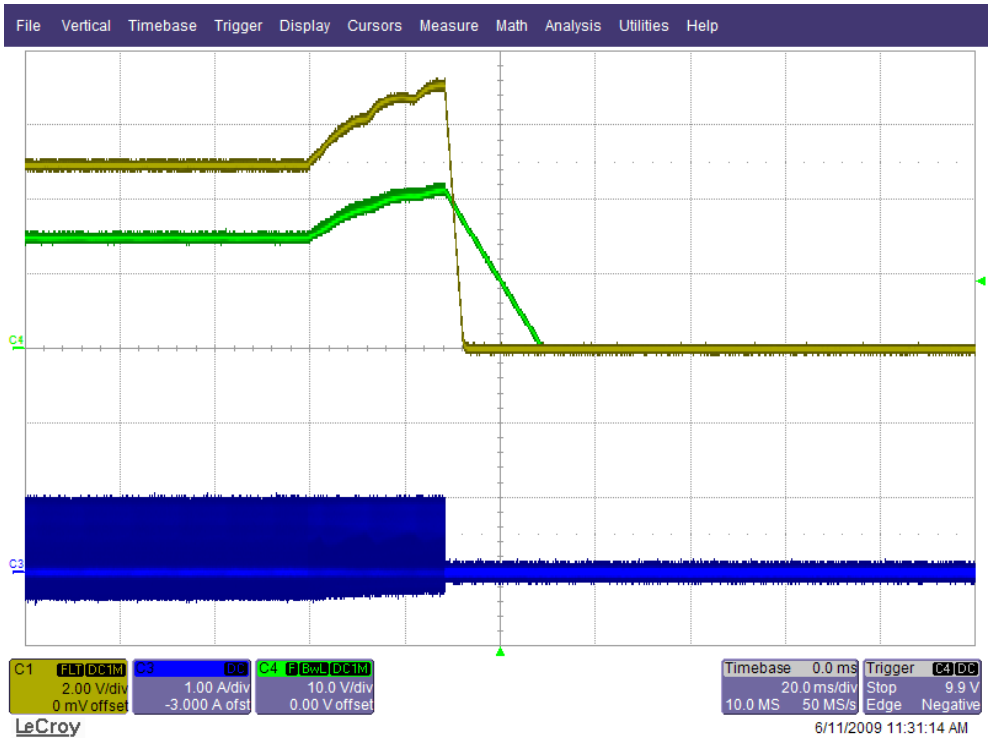

Figure 25 – Output Overvoltage Protection, 90 VAC, Full Load
Top: 5 V Output Voltage, 2 V / div.
Middle: 14.5 V Output Voltage, 10 V / div.
Bottom: Drain Current, 1 A, 20 ms / div.

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11.6 Output Ripple Measurements

11.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 1.0 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

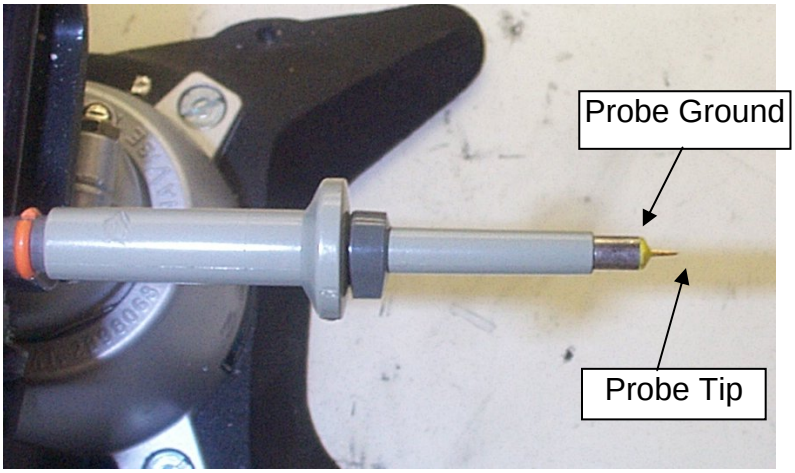

Figure 26 – Oscilloscope Probe Prepared for Ripple Measurement (end cap and ground lead removed).

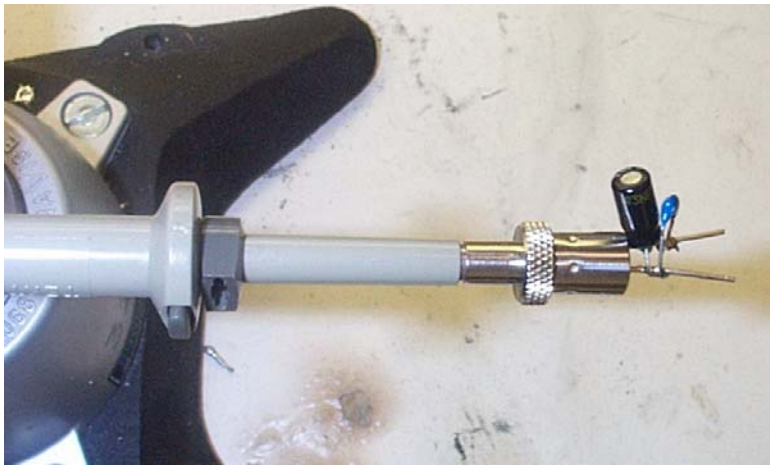

Figure 27 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter (modified with wires for ripple measurement and two parallel decoupling capacitors added).

11.6.2 Measurement Results

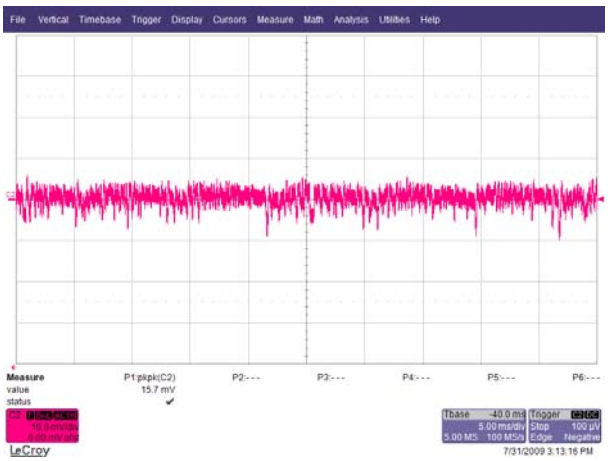

Figure 28 – 5 V Output Ripple,
90 VAC, Full Load.
10 mV, 5 ms / div.

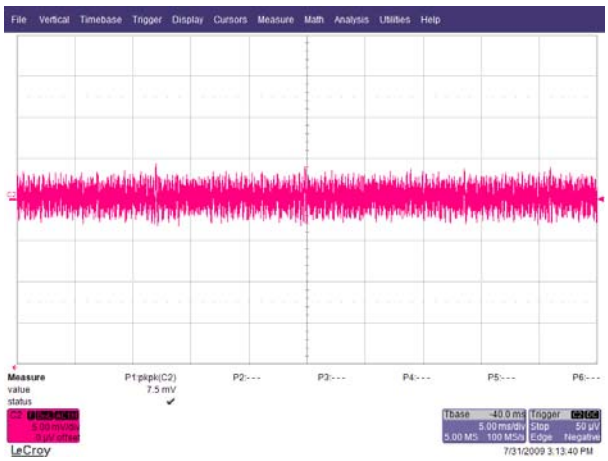

Figure 29 – 5 V Output Ripple,
265 VAC, Full Load.
5 mV, 5 ms / div.

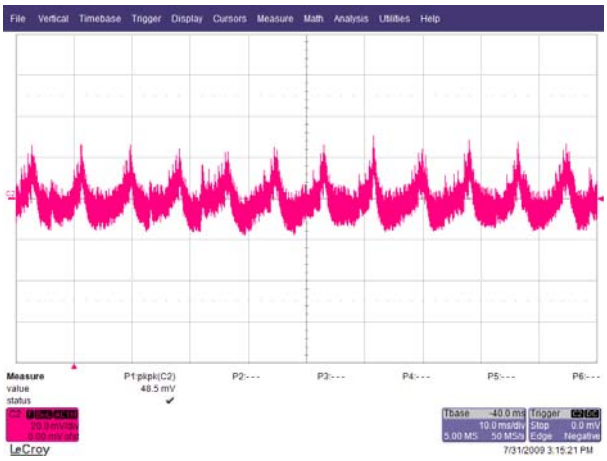

Figure 30 – 14.5 V Output Ripple,
90 VAC, Full Load.
20 mV, 10 ms / div.

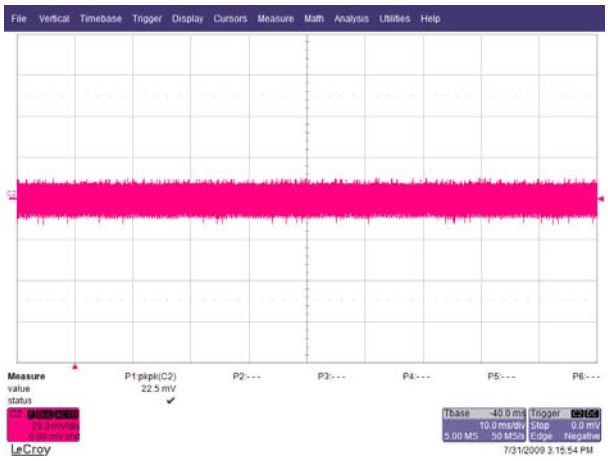

Figure 31 – 14.5 V Output Ripple,
265 VAC, Full Load.
20 mV, 10 ms / div.

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12 Audible Noise

12.1 Measurement Set-up

The unit was placed inside a test chamber which was filled with sound-deadening material to reduce the background ambient noise level.

A calibrated microphone was then positioned above the test unit, directly above the location of the internal transformer, at a fixed distance. The output of the microphone was fed into an audio analyzer by Audio Precision Inc. (Audio Precision System II + DSP audio analyzer; Model #: SYS2222).

The output of the supply was connected to an electronic load (outside the chamber) which was swept at a rate of 10 mA / second from no load to full load during testing at 90 V, 115 V, 230 V, and 265 VAC.

Figure 32 – In-House Audio Test Chamber (L: 20” x W: 13” x H: 13”).

12.2 Measurement

Audible noise was measured at room temperature with a distance of 4 cm between the microphone and transformer surface. This is an equivalent situation to measuring when the power supply is assembled inside a monitor where the microphone is 3 cm away from the LCD monitor case.

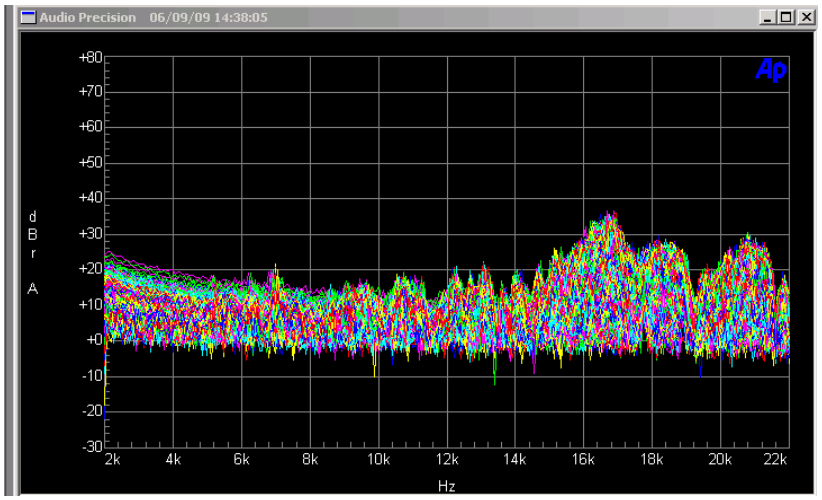

Figure 33 – Composite Audible Noise Profile with the Load Swept from Zero to Maximum at 90 VAC.

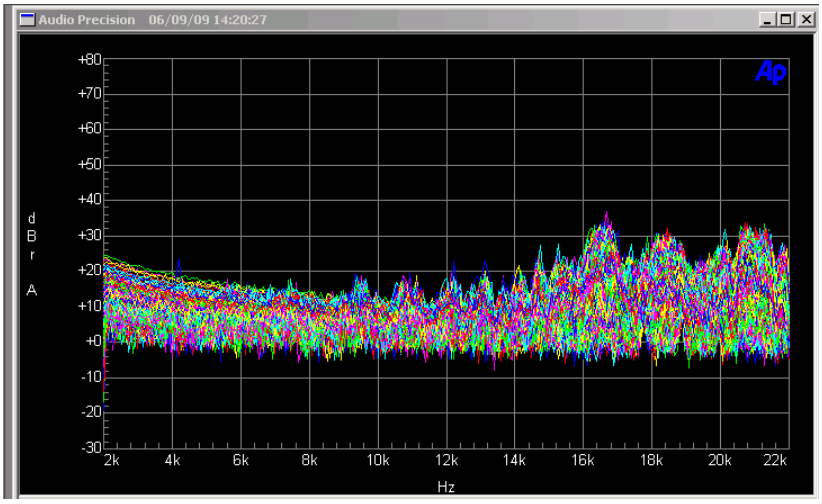

Figure 34 – Composite Audible Noise Profile with the Load Swept from Zero to Maximum at 115 VAC.

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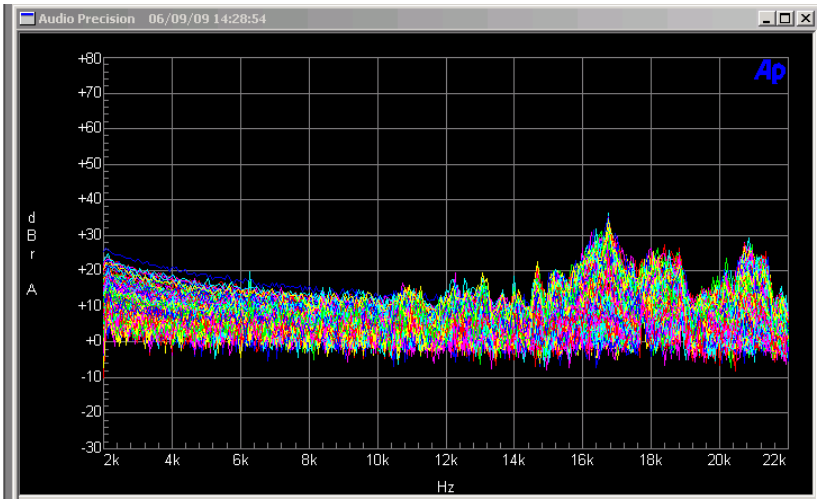

Figure 35 – Composite Audible Noise Profile with the Load Swept from Zero to Maximum at 230 VAC.

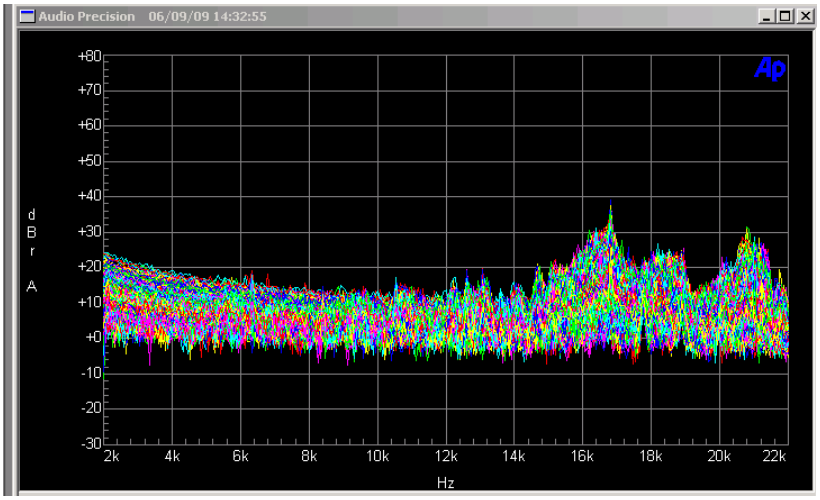

Figure 36 – Composite Audible Noise Profile with the Load Swept from Zero to Maximum at 265 VAC.

13 Conducted EMI

Radiated EMI has been tested with the board mounted on a ground plane while the output return is also grounded.

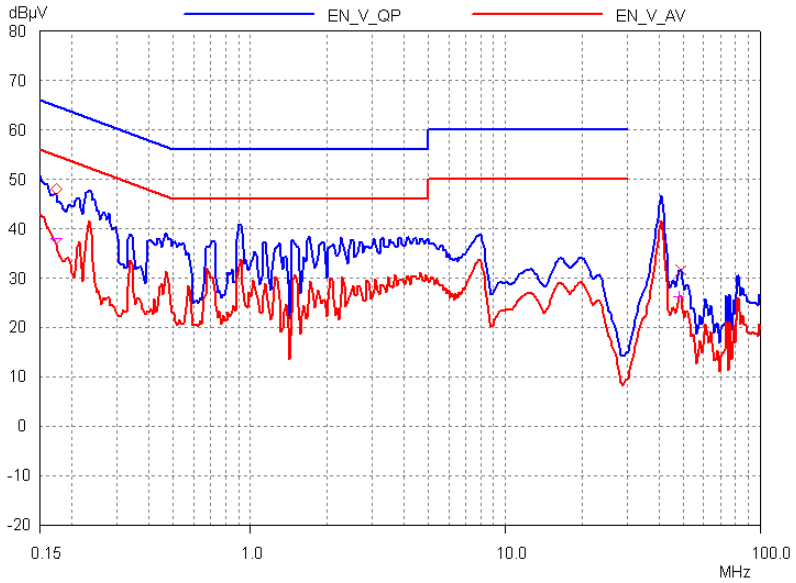

Figure 37 – Conducted EMI, Full Load, 115 VAC, 60 Hz.

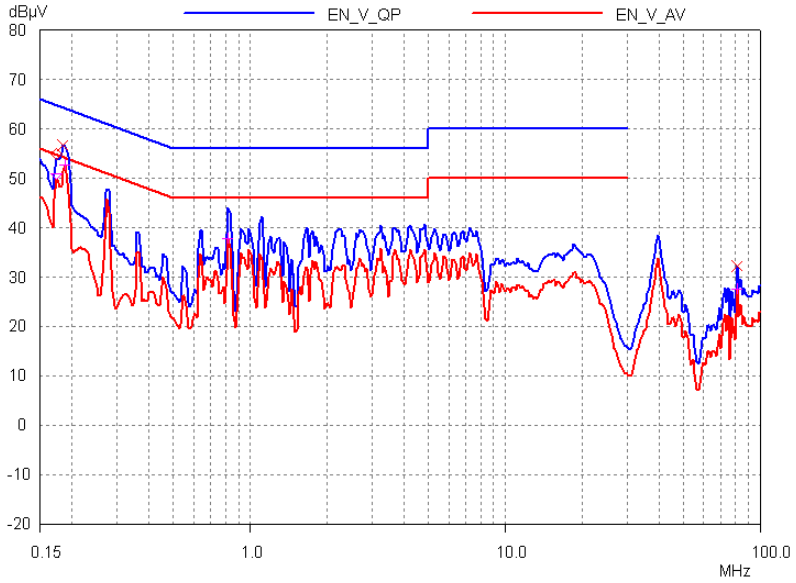

Figure 38 – Conducted EMI, Full Load, 230 VAC, 60 Hz.

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14 Revision History

Date	Author	Revision	Description & changes	Reviewed
17-Aug-09	JY	1.0	Initial release	Apps & Mktg

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm.

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