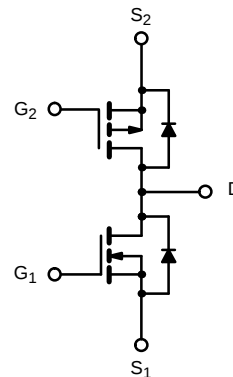
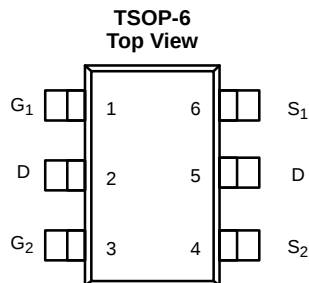




Complementary MOSFET Half-Bridge (N- and P-Channel)

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.500 @ $V_{GS} = 4.5$ V	± 1.2
		0.750 @ $V_{GS} = 3.0$ V	± 1.0
P-Channel	-20	1.00 @ $V_{GS} = -4.5$ V	± 0.85
		1.30 @ $V_{GS} = -3.0$ V	± 0.75



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	−20	V
Gate-Source Voltage		V _{GS}	± 12	± 12	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	± 1.2	± 0.85	A
	T _A = 70 °C		± 0.95	± 0.65	
Pulsed Drain Current		I _{DM}	± 3.5	± 2.5	
Continuous Source Current (Diode Conduction)		I _S	1	−1	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T _A = 25 °C	P _D	1.25		W
	T _A = 70 °C		0.8		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P- Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board, $\pm \leq 10$ sec)	R_{thJA}	100	$^\circ\text{C/W}$

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6			V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.6			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V				±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	μA
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch			-1	
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C	N-Ch			10	
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 70 °C	P-Ch			-10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	N-Ch	3.0			A
		V _{DS} = -5 V, V _{GS} = -4.5 V	P-Ch	-2.0			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 0.5 A	N-Ch		0.38	0.500	Ω
		V _{GS} = -4.5 V, I _D = -0.5 A	P-Ch		0.70	1.00	
		V _{GS} = 3.0 V, I _D = 0.5 A	N-Ch		0.55	0.750	
		V _{GS} = -3.0 V, I _D = -0.5 A	P-Ch		1.10	1.30	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 1.2 A	N-Ch		2.7		S
		V _{DS} = -10 V, I _D = -0.85 A	P-Ch		1.2		
Diode Forward Voltage ^a	V _{SD}	I _S = 1 A, V _{GS} = 0 V	N-Ch			1.2	V
		I _S = -1 A, V _{GS} = 0 V	P-Ch			-1.2	
Dynamic ^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 1.2 A P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V I _D = -0.85 A	N-Ch		0.8	2.0	nC
Gate-Source Charge	Q _{gs}		P-Ch		1.10	2.5	
			N-Ch		0.25		
Gate-Drain Charge	Q _{gd}		P-Ch		0.50		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω	N-Ch		10	20	ns
			P-Ch		8	15	
Rise Time	t _r		N-Ch		20	40	
			P-Ch		20	40	
Turn-Off Delay Time	t _{d(off)}		N-Ch		20	40	
			P-Ch		10	20	
Fall Time	t _f		N-Ch		16	30	
			P-Ch		8	15	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1 A, di/dt = 100 A/μs	N-Ch		40	80	
		I _F = -1 A, di/dt = 100 A/μs	P-Ch		40	80	

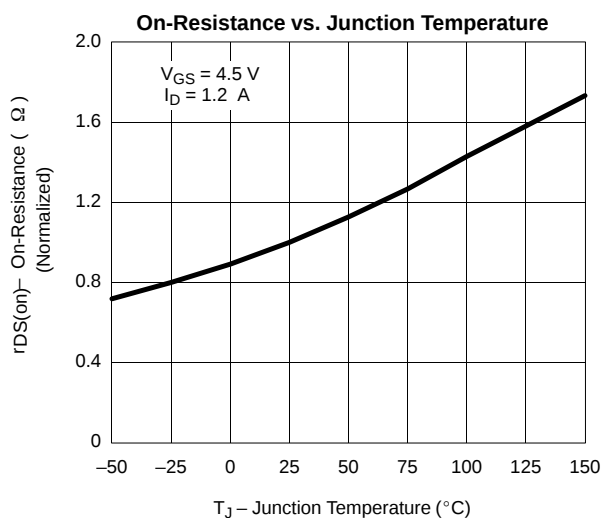
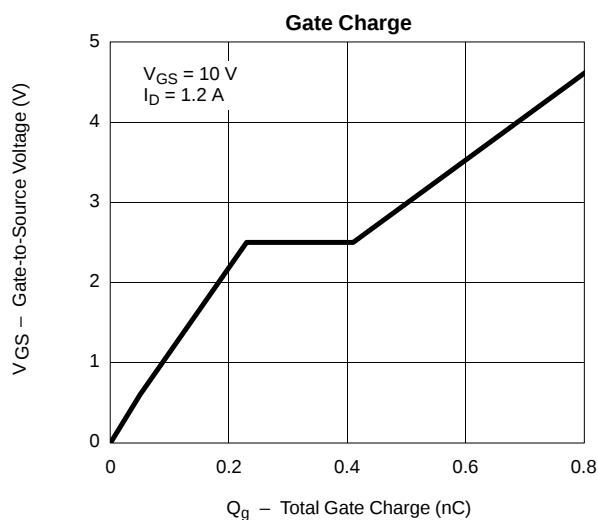
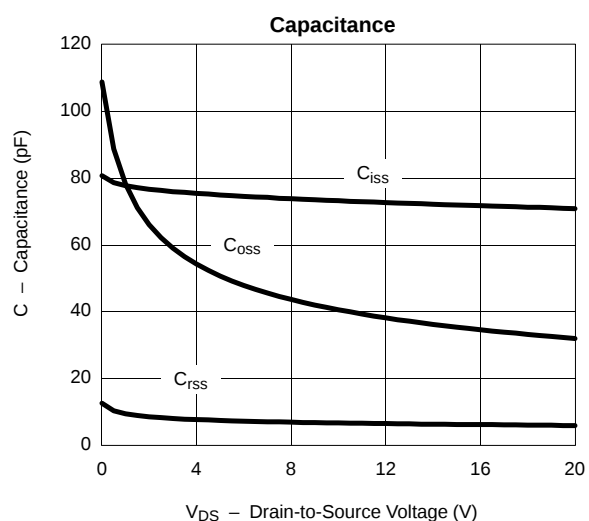
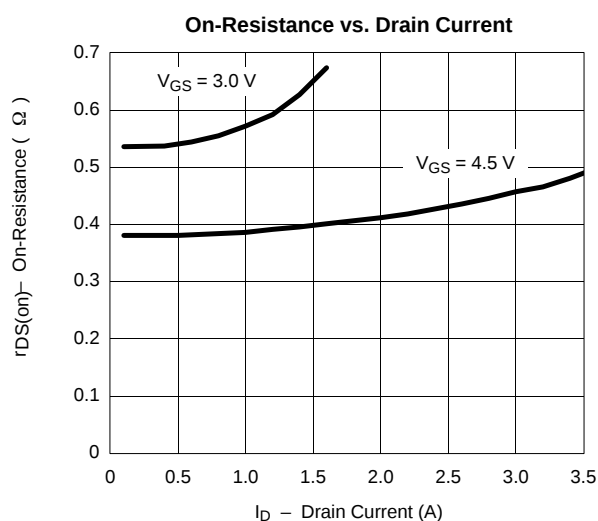
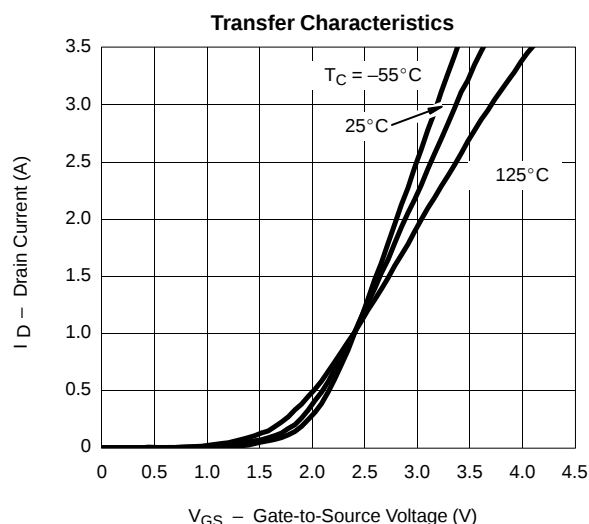
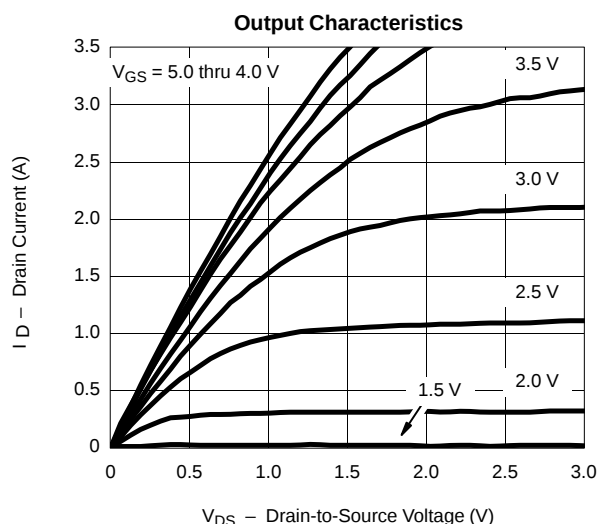
Notes

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



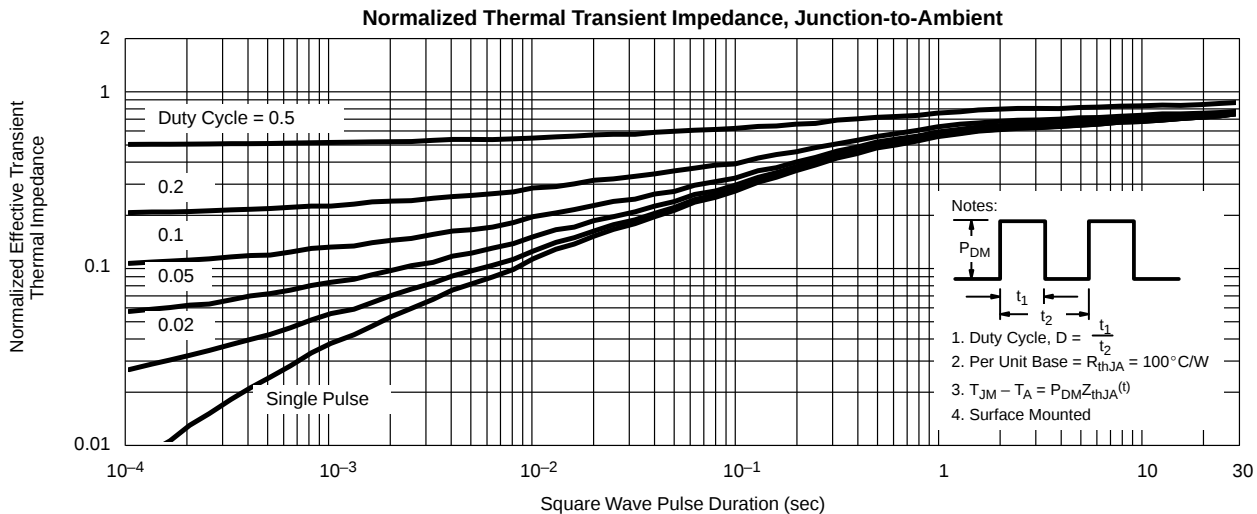
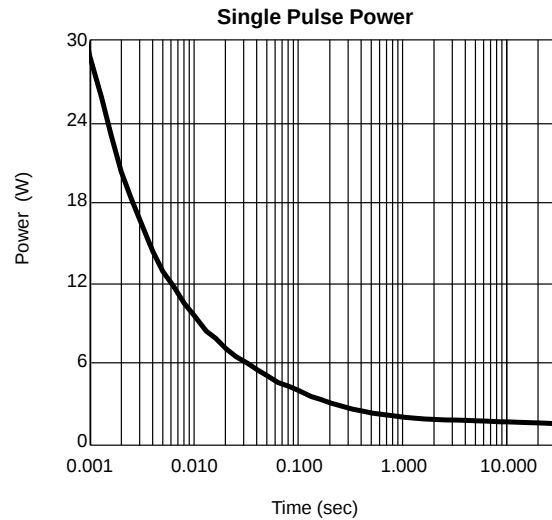
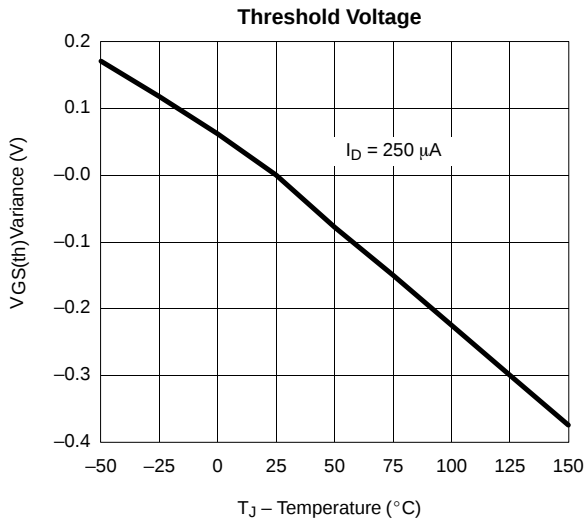
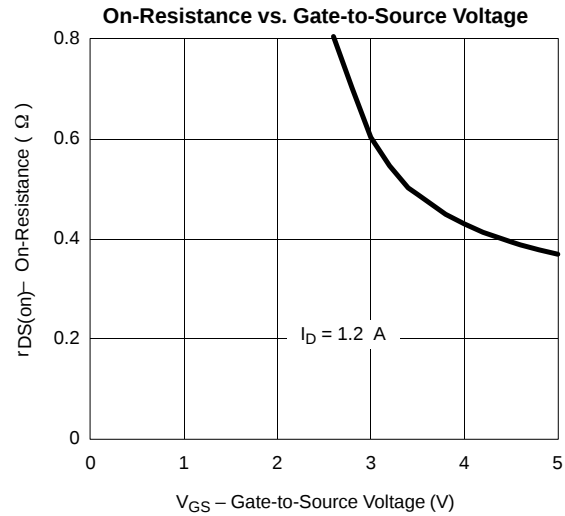
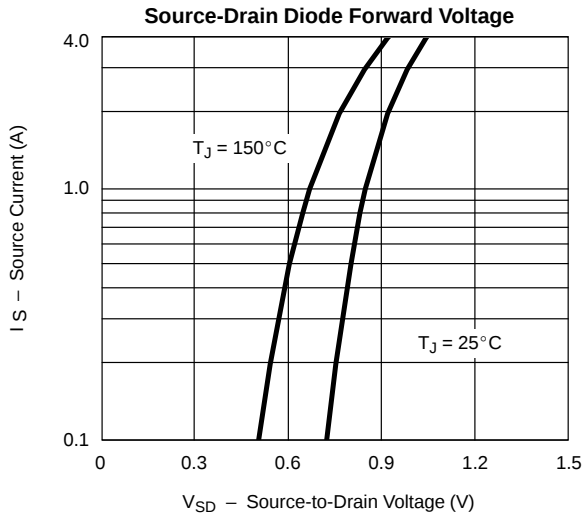
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

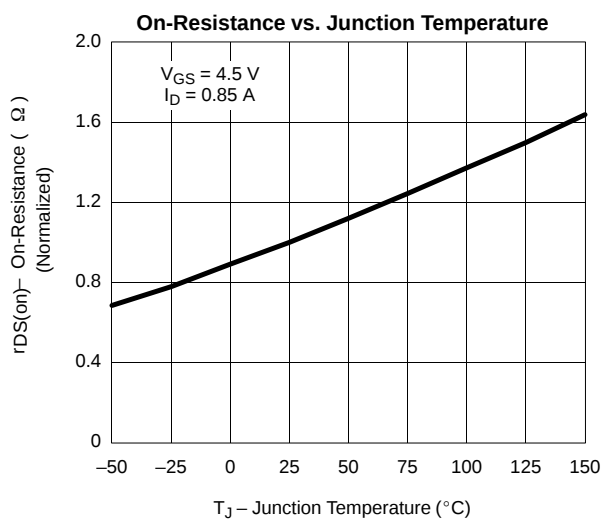
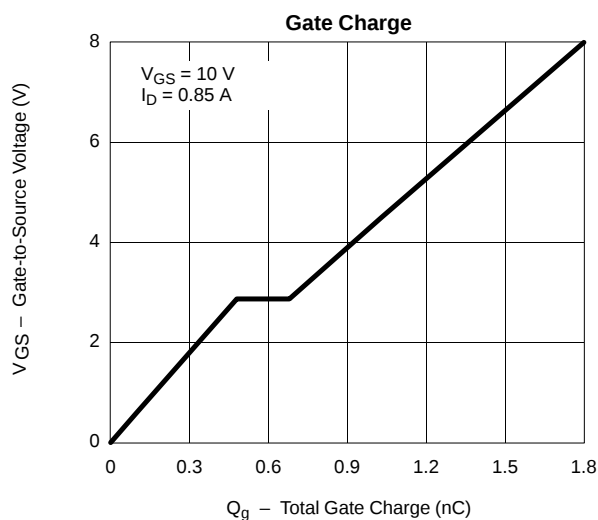
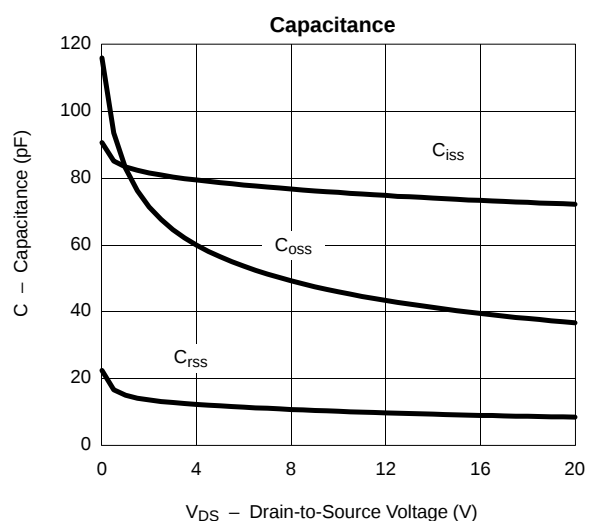
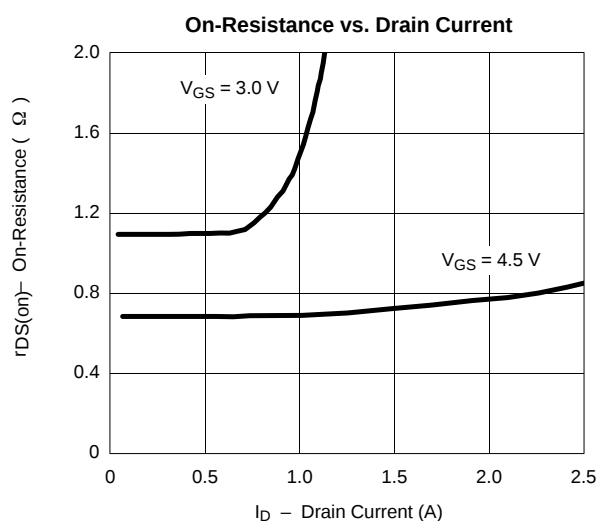
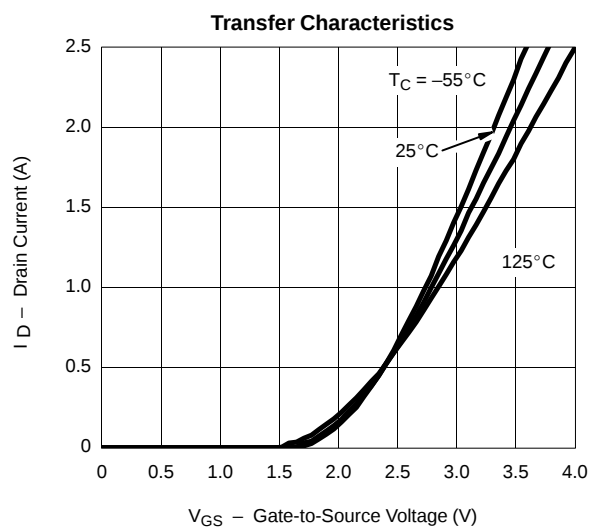
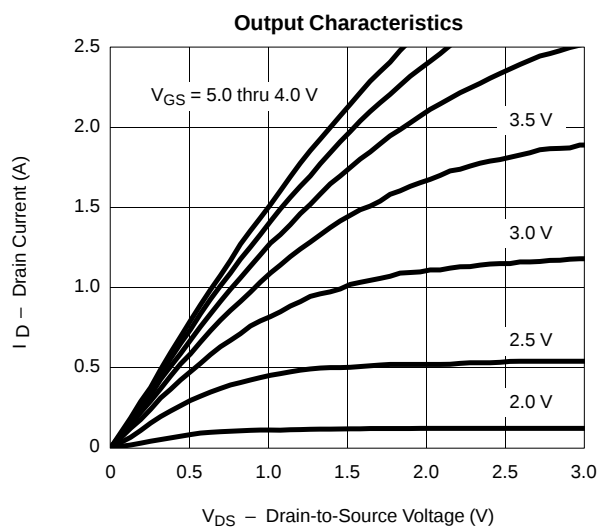
N-CHANNEL





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL

