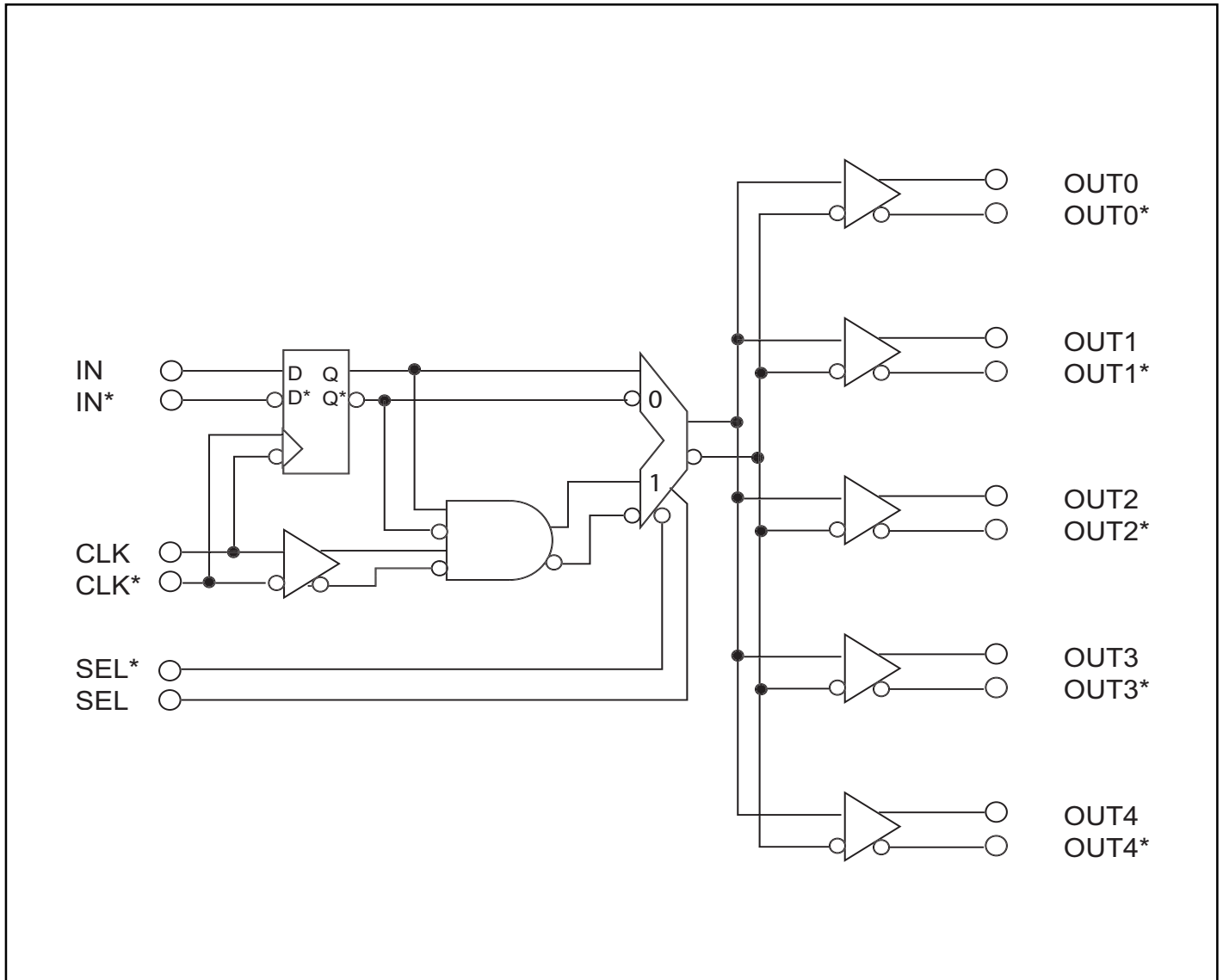


**SK15XX Family Functional Block Diagram**


### SK15XX Family Product Selection Guide

1:5 Signal Distribution

3 GHz

Synch / Asynch Operation

#### Logic Family

Product	Power Supply		Output Configuration				Output	Availability
	3.3V	5.5V	Open Emitter	50 $\Omega$ Double Termination	50 $\Omega$ Source Termination	Internal Current Sink (Double Termination)		
SK1500	●	●	●				ECL / PECL	Now
SK1501		●	●				Double Swing	Now
SK1502	●	●		●			ECL / PECL	Now
SK1503	●	●				●	ECL / PECL	Now
SK1504	●	●			●		ECL / PECL	Now

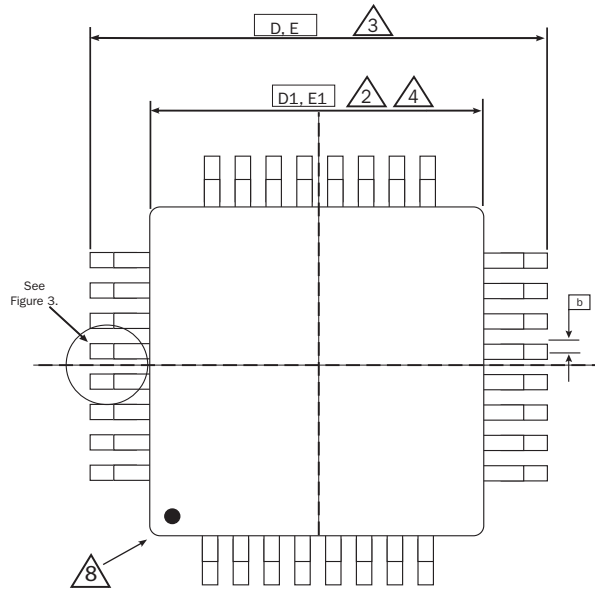
#### Logic / Translation Family

Product	Translation	Output Configuration			Availability
		Open Emitter	50 $\Omega$ Double Termination	50 $\Omega$ Source Termination	
SK1525	Anything to PECL	●			Now
SK1526	Anything to ECL	●			Now
SK1527	Anything to PECL		●		Now
SK1528	Anything to ECL		●		Now
SK1529	Anything to PECL			●	Now
SK1530	Anything to ECL			●	Now

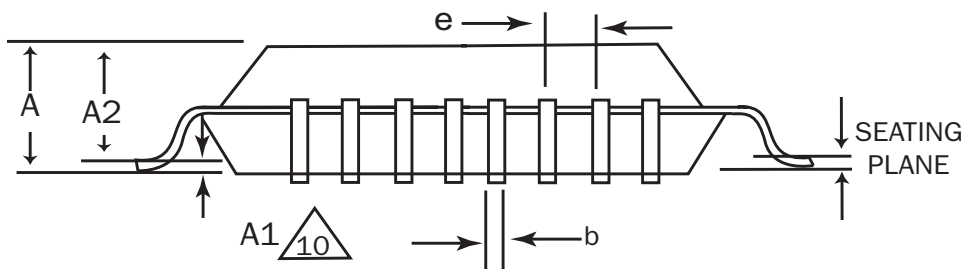
#### Open Collector Logic Family

Product	Output Configuration	Output Current	Availability
SK1599	Open Collector ●	12 mA	Now

*SK15XX Family Package Information*  
*5mm x 5mm TQFP*



Top View



Side View

### TEST AND MEASUREMENT PRODUCTS

### SK15XX Family Package Information (continued)

#### 5mm x 5mm TQFP

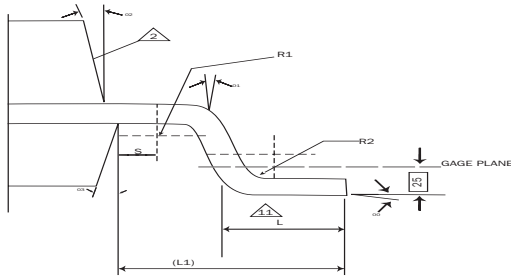


Figure 1.

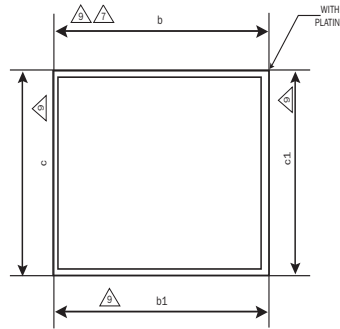


Figure 2.

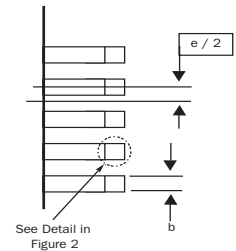


Figure 3.

- All dimensions and tolerancing conforms to ANSI Y14.5M-1982.
- The top package body size may be smaller than the bottom package body size by as much as 0.15 mm.
- To be determined at seating plane.
- Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
- Details of Pin 1 identifier optional, but must be located within the zone indicated.
- All dimensions are in millimeters.
- Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
- Exact shape of each corner is optional.
- These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
- A1 is defined as the distance from the seating plane to the lowest point of the package body.

JEDEC Variation					
All Dimensions in Millimeters					
Symbol	MIN	NOM	MAX	Note	Comments
A	1.00	1.10	1.20		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	0.95	1.00	1.05		Package Body Thickness
D	7.00 BSC			3	
D1	5.00 BSC			4, 2	Package Body Length
E	7.00 BSC			3	
E1	5.00 BSC			4, 2	Package Body Width
N	32				Lead Count
e	0.50 BSC				Lead Pitch
b	0.17	0.22	0.27	7	Lead Thickness
b1	0.17	0.20	0.23		
R1	0.08	-	-		
R2	0.08	-	0.20		
00	0°	3.5°	7°		
01	0°	-	-		
02	11°	12°	13°		
03	11°	12°	13°		
S	0.20	-	-		
c	0.09	-	0.20		
c1	0.09	-	0.16		
L	0.45	0.60	0.75		
L1	1.00 REF				
aaa	0.20				
bbb	0.20				
ccc	0.08				
ddd	0.08				

### TEST AND MEASUREMENT PRODUCTS

#### Absolute Maximum Ratings\*

Symbol	Parameter	Value	Unit
V <sub>EE</sub>	Power Supply (V <sub>CC</sub> = 0V)	-8.0 to 0	V
V <sub>CC</sub>	Power Supply (V <sub>EE</sub> = 0V)	+8.0 to 0	V
V <sub>I</sub>	Input Voltage	V <sub>CC</sub> ≥ V <sub>I</sub> ≥ V <sub>EE</sub>	V
I <sub>OUT</sub>	Output Current Continuous Surge	50 100	mA mA
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>sol</sub>	Solder Temperature (<2 to 3 seconds: 245°C desired)	265	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

**Note:**

1. Device is ESD sensitive and requires protective handling.

### TEST AND MEASUREMENT PRODUCTS

#### Description

The SK1500 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1500 uses standard open emitter ECL outputs optimized for:

- General purpose ECL compatible applications
- Multiple destination applications (daisy chain).

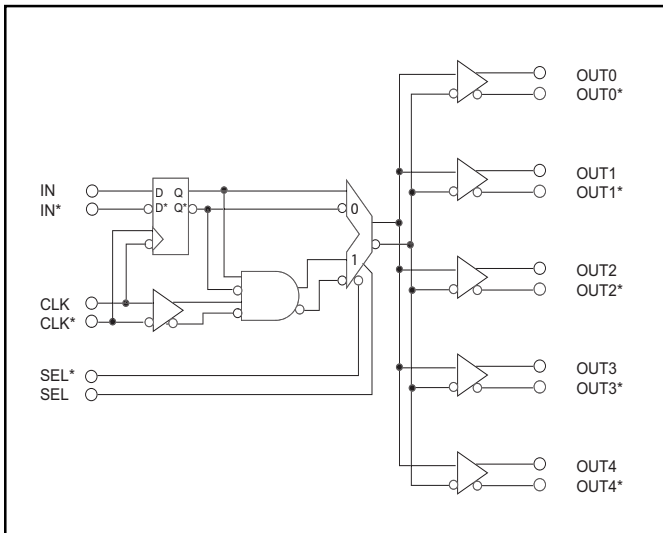
#### Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.5V Compatible
- Available in 32 pin, 5mm X5mm, TQFP Package

#### Application Notes

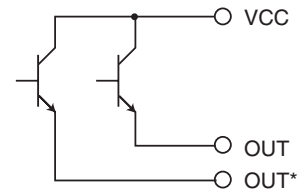
- AN1001** - EPIC Family Product Line
- AN1003** - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

#### Functional Block Diagram

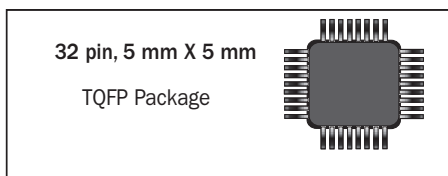


#### Output Option

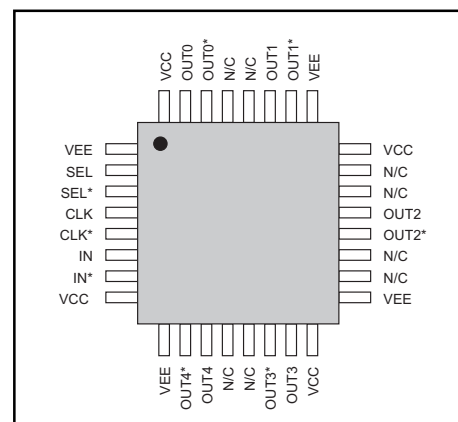
##### Open Emitter



#### Package Information



#### Pin Description



### TEST AND MEASUREMENT PRODUCTS

#### DC Characteristics

( $V_{CC} - V_{EE} = 3.0V$  to  $5.5V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	$V_{IH}$	$V_{EE} + 2.0$		$V_{CC}$	V
Input Low	$V_{IL}$	$V_{EE}$		$V_{CC} - 0.2$	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	$ V_{IH} - V_{IL} $	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current	$I_{IH}$	-5		+30	$\mu A$
Input Low Current	$I_{IL}$	-6		+6	$\mu A$
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	$I_{IH}, I_{IL}$	-500		+500	$\mu A$
Outputs					
Digital Output Voltage	$ OUT - OUT^* $	600	700	$V_{CC} - 1.1$	mV
Output Common Mode Range	$(OUT + OUT^*) / 2$	$V_{CC} - 1.5$	$V_{CC} - 1.3$		V
Power Supply					
Power Supply Current	$I_{EE}$			132	mA

Test Conditions: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

#### AC Characteristics

( $V_{CC} - V_{EE} = 3.0V$  to  $5.5V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0)	$T_{pd}$	485	630	785	ps
CLK to OUT (SEL = 1)	$T_{pd}$	300	450	600	ps
SEL to OUT	$T_{pd}$	300	450	600	ps
Channel to Channel Skew	$t_{SKEW}$			20	ps
Maximum Operating Frequency (Note 1)	$F_{max}$	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time	$T_s$	100			ps
Hold Time	$T_h$	100			ps
Output Rise and Fall Times (20% / 80%) (Note 1)	$T_r / T_f$		125	175	ps
Temperature Coefficient (Note 1)	$\Delta T_{pd} / \Delta T$		<1		ps / $^{\circ}C$

AC TEST CONDITIONS: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2.0V$

Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

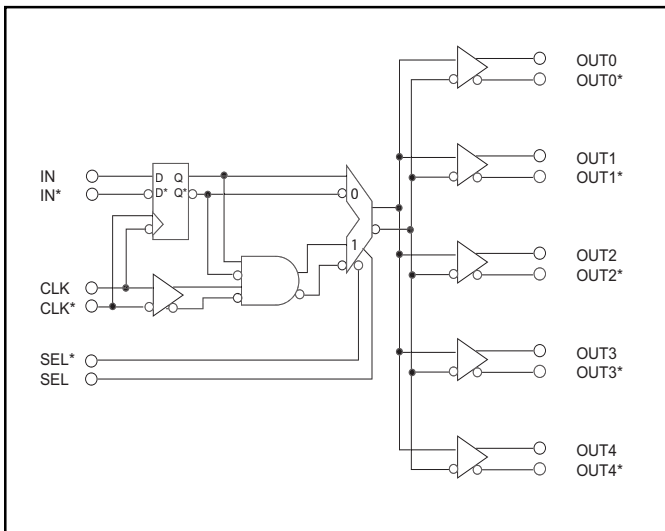
#### Description

The SK1501 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

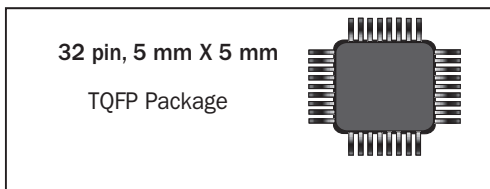
The SK1501 uses open emitter outputs with a double amplitude swing suitable for the following applications:

- Double termination situations that require a full swing at the destination
- Long cables

#### Functional Block Diagram



#### Package Information

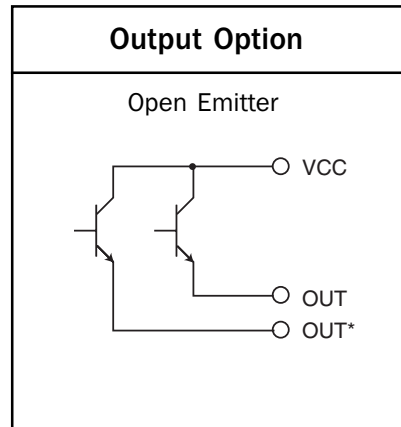


#### Features

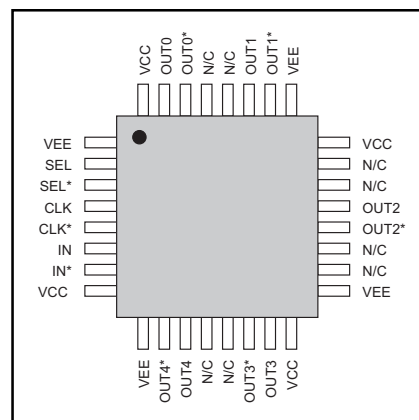
- 1:5 Clock/Data Driver
- 2 GHz Fmax
- 4.2V / 5.5V Compatible
- Available in 32 pin, 5mm X5mm, TQFP Package

#### Application Notes

- AN1001** - EPIC Family Product Line
- AN1003** - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL



#### Pin Description



### TEST AND MEASUREMENT PRODUCTS

#### DC Characteristics

( $V_{CC} - V_{EE} = 4.2V$  to  $5.5V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High	$V_{IH}$	$V_{EE} + 2.0$		$V_{CC}$	V
Input Low	$V_{IL}$	$V_{EE}$		$V_{CC} - 0.2$	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	$ V_{IH} - V_{IL} $	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	$I_{IH}$	-5		+30	$\mu A$
Input Low Current	$I_{IL}$	-6		+6	$\mu A$
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	$I_{IH}, I_{IL}$	-500		+500	$\mu A$
<b>Outputs</b>					
Digital Output Voltage	$ OUT - OUT^* $	1.2	1.4		V
Output Common Mode Range	$(OUT + OUT^*) / 2$	$V_{CC} - 2.2$	$V_{CC} - 1.9$	$V_{CC} - 1.7$	V
<b>Power Supply</b>					
Power Supply Current	$I_{EE}$			132	mA

Test Conditions: Outputs terminated with  $50\Omega$  to  $V_{CC} - 3.3V$ .

#### AC Characteristics

( $V_{CC} - V_{EE} = 4.2V$  to  $5.5V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay					
CLK to OUT (SEL = 0)	$T_{pd}$	500	760	1020	ps
CLK to OUT (SEL = 1)	$T_{pd}$	400	650	900	ps
SEL to OUT	$T_{pd}$	350	625	900	ps
Channel to Channel Skew	$t_{SKEW}$			100	ps
Maximum Operating Frequency (Note 1)	$F_{max}$	2.0			GHz
Minimum Pulse Width (Note 1)	PW min	350			ps
IN to CLK					
Set Up Time	$T_s$	100			ps
Hold Time	$T_h$	100			ps
Output Rise and Fall Times (20% / 80%) (Note 1)	$T_r / T_f$		200	475	ps
Temperature Coefficient (Note 1)	$\Delta T_{pd} / \Delta T$		<3		ps / $^{\circ}C$

AC TEST CONDITIONS: Outputs terminated with  $50\Omega$  to  $V_{CC} - 3.3V$ .

Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

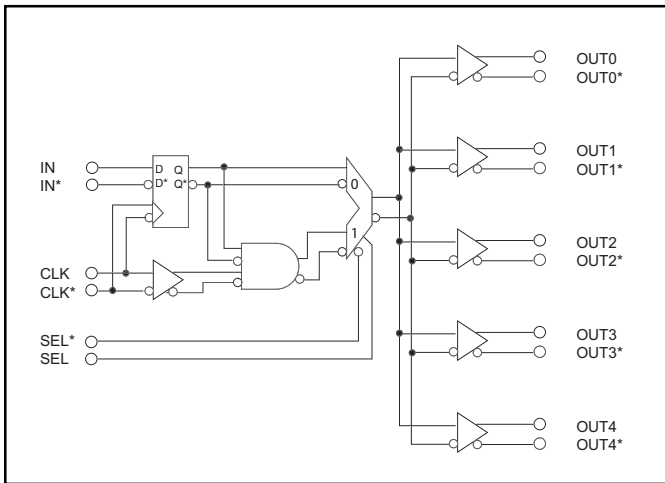
#### Description

The SK1502 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1502 uses 50Ω outputs with source /sink capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines

#### Functional Block Diagram



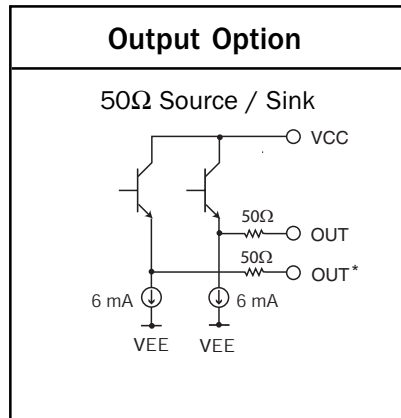
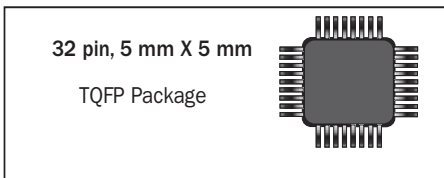
#### Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.5V Compatible
- Available in 32 pin, 5mm X5mm, TQFP Package

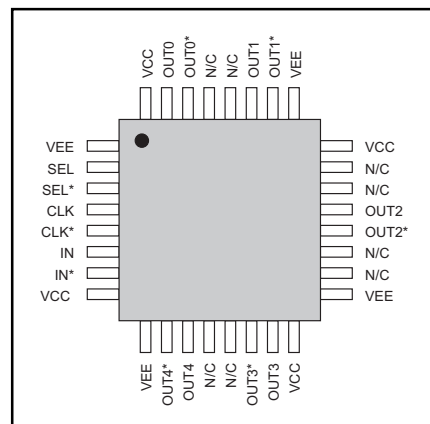
#### Application Notes

- AN1001 - EPIC Family Product Line
- AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

#### Package Information



#### Pin Description



### TEST AND MEASUREMENT PRODUCTS

#### DC Characteristics

( $V_{CC} - V_{EE} = 3.0V$  to  $5.5V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High	$V_{IH}$	$V_{EE} + 2.0$		$V_{CC}$	V
Input Low	$V_{IL}$	$V_{EE}$		$V_{CC} - 0.2$	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	$ V_{IH} - V_{IL} $	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	$I_{IH}$	-5		+30	$\mu A$
Input Low Current	$I_{IL}$	-6		+6	$\mu A$
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	$I_{IH}, I_{IL}$	-500		+500	$\mu A$
<b>Outputs</b>					
Digital Output Voltage	$ OUT - OUT^* $	600	700		mV
Output Common Mode Range	$(OUT + OUT^*) / 2$	$V_{CC} - 1.4$	$V_{CC} - 1.2$	$V_{CC} - 1.0$	V
Internal Current Source	ISINK	4	6	7.5	mA
Output Impedance	ROUT	40	50	60	$\Omega$
<b>Power Supply</b>					
Power Supply Current	IEE			240	mA

Test Conditions: Outputs unterminated.

#### AC Characteristics

( $V_{CC} - V_{EE} = 3.0V$  to  $5.5V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay					
CLK to OUT (SEL = 0)	$T_{pd}$	485	630	785	ps
CLK to OUT (SEL = 1)	$T_{pd}$	300	450	600	ps
SEL to OUT	$T_{pd}$	300	450	600	ps
Channel to Channel Skew	$t_{SKEW}$			20	ps
Maximum Operating Frequency (Note 1)	$F_{max}$	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK					
Set Up Time	$T_s$	100			ps
Hold Time	$T_h$	100			ps
Output Rise and Fall Times (20% / 80%)(Note 1)	$T_r / T_f$		125	175	ps
Temperature Coefficient(Note 1)	$\Delta T_{pd} / \Delta T$		<1		ps / $^{\circ}C$

AC TEST CONDITIONS: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2.0V$ .

Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

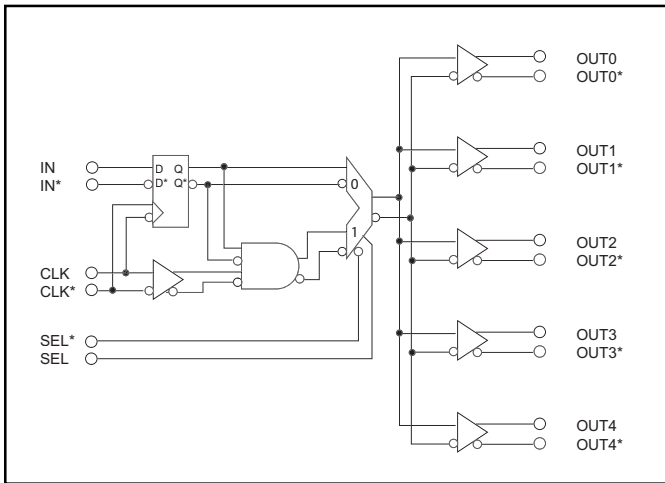
#### Description

The SK1503 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

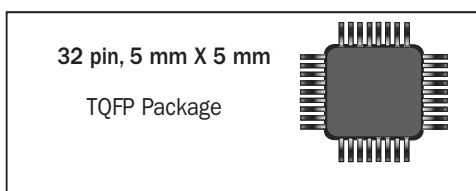
The SK1503 outputs are open emitter with an internal current source, optimized for applications that are:

- Point to point, double terminated, timing critical lines
- Non-50Ω transmission lines

#### Functional Block Diagram



#### Package Information

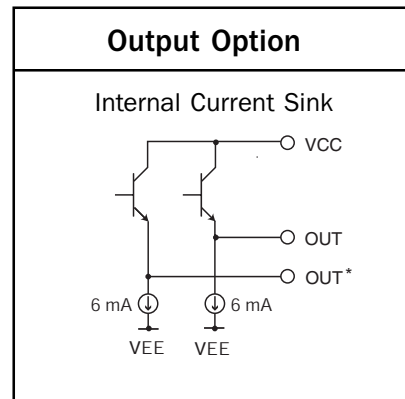


#### Features

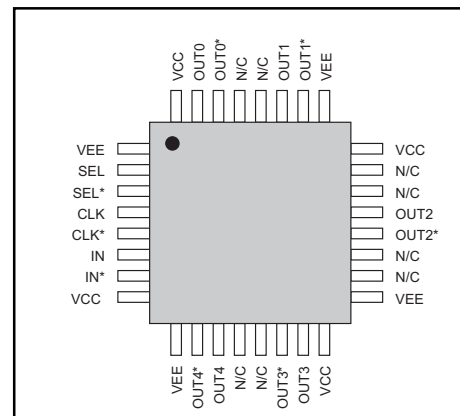
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.0V / 5.5V Compatible
- Available in 32 pin, 5mm X5mm, TQFP Package

#### Application Notes

- AN1001** - EPIC Family Product Line
- AN1003** - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL



#### Pin Description



## TEST AND MEASUREMENT PRODUCTS

### DC Characteristics

(V<sub>CC</sub> - V<sub>EE</sub> = 3.0V to 5.5V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High Input Low	V <sub>IH</sub> V <sub>IL</sub>	V <sub>EE</sub> + 2.0 V <sub>EE</sub>		V <sub>CC</sub> V <sub>CC</sub> - 0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	V <sub>IH</sub> - V <sub>IL</sub>	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	I <sub>IH</sub> I <sub>IL</sub>	-5 -6		+30 +6	μA μA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	I <sub>IH</sub> , I <sub>IL</sub>	-500		+500	μA
<b>Outputs</b>					
Digital Output Voltage Output Common Mode Range Internal Current Source	OUT - OUT*   (OUT + OUT*) / 2 I <sub>SINK</sub>	600 V <sub>CC</sub> - 1.5 4	700 V <sub>CC</sub> - 1.3 6	V <sub>CC</sub> - 1.1 7.5	mV V mA
<b>Power Supply</b>					
Power Supply Current	I <sub>EE</sub>			240	mA

Test Conditions: Outputs unterminated.

### AC Characteristics

(V<sub>CC</sub> - V<sub>EE</sub> = 3.0V to 5.5V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	T <sub>pd</sub> T <sub>pd</sub> T <sub>pd</sub>	485 300 300	630 450 450	785 600 600	ps ps ps
Channel to Channel Skew	t <sub>SKEW</sub>			20	ps
Maximum Operating Frequency (Note 1)	F <sub>max</sub>	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	T <sub>s</sub> T <sub>h</sub>	100 100			ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	T <sub>r</sub> / T <sub>f</sub>		125	175	ps
Temperature Coefficient (Note 1)	ΔT <sub>pd</sub> / ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to V<sub>CC</sub> -2.0V.

Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

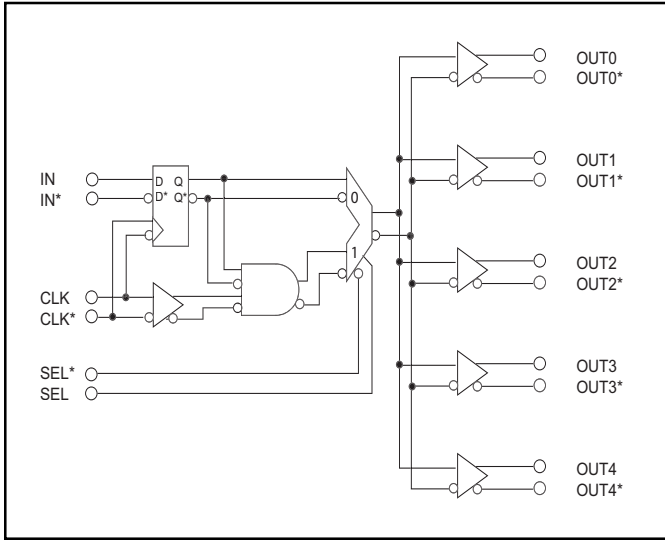
#### Description

The SK1504 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

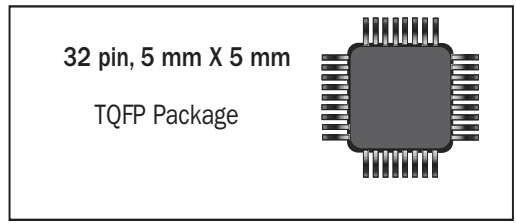
The SK1504 outputs are 50Ω with source and sink capability, optimized for:

- Point to point, series terminated, timing critical lines

#### Functional Block Diagram



#### Package Information



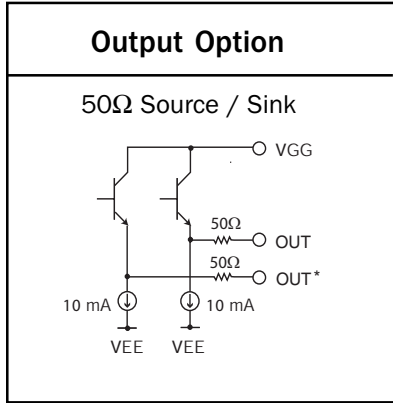
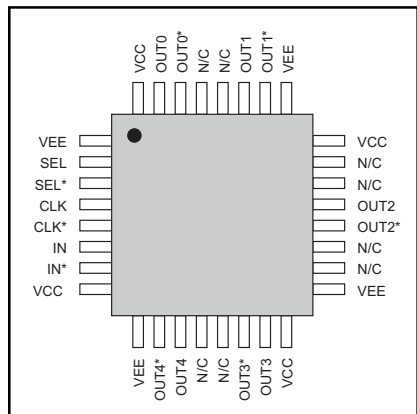
#### Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.5V Compatibles
- Available in 32 pin, 5mm X5mm, TQFP Package

#### Application Notes

- AN1001 - EPIC Family Product Line
- AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

#### Pin Description



### TEST AND MEASUREMENT PRODUCTS

#### DC Characteristics

( $V_{CC} - V_{EE} = 3.0V$  to  $5.5V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High	$V_{IH}$	$V_{EE} + 2.0$		$V_{CC}$	V
Input Low	$V_{IL}$	$V_{EE}$		$V_{CC} - 0.2$	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	$ V_{IH} - V_{IL} $	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	$I_{IH}$	-5		+30	$\mu A$
Input Low Current	$I_{IL}$	-6		+6	$\mu A$
Functional Inputs (IN / IN*, SEL / SEL*)					
Input Current	$I_{IH}, I_{IL}$	-500		+500	$\mu A$
<b>Outputs</b>					
Digital Output Voltage	$ OUT - OUT^* $	600	700		mV
Output Common Mode Range	$(OUT + OUT^*) / 2$	$V_{CC} - 1.4$	$V_{CC} - 1.2$	$V_{CC} - 1.0$	V
Internal Current Source	ISINK	7.5	10	13	mA
Output Impedance	ROUT	40	50	60	$\Omega$
<b>Power Supply</b>					
Power Supply Current	IEE			240	mA

Test Conditions: Outputs unterminated.

#### AC Characteristics

( $V_{CC} - V_{EE} = 3.0V$  to  $5.5V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay					
CLK to OUT (SEL = 0)	$T_{pd}$	485	630	785	ps
CLK to OUT (SEL = 1)	$T_{pd}$	300	450	600	ps
SEL to OUT	$T_{pd}$	300	450	600	ps
Channel to Channel Skew	$t_{SKEW}$			20	ps
Maximum Operating Frequency (Note 1)	$F_{max}$	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK					
Set Up Time	$T_s$	100			ps
Hold Time	$T_h$	100			ps
Output Rise and Fall Times (20% / 80%)(Note 1)	$T_r / T_f$		125	175	ps
Temperature Coefficient(Note 1)	$\Delta T_{pd} / \Delta T$		<1		ps / $^{\circ}C$

AC TEST CONDITIONS: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2.0V$ .

Note 1: Guaranteed by characterization. Not production tested.



## TEST AND MEASUREMENT PRODUCTS

### DC Characteristics

( $V_{CC} = 3.0V$  to  $3.6V$ ;  $V_{EE} = -3.6V$  to  $-3.0V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High	$V_{IH}$	$V_{EE} + 2.0$		$V_{CC}$	V
Input Low	$V_{IL}$	$V_{EE}$		$V_{CC} - 0.2$	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	$ V_{IH} - V_{IL} $	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	$I_{IH}$	-5		+30	$\mu A$
Input Low Current	$I_{IL}$	-6		+6	$\mu A$
Functional Inputs (IN / IN*, SEL / SEL*)					
Input Current	$I_{IH}, I_{IL}$	-500		+500	$\mu A$
<b>Outputs</b>					
Digital Output Voltage	$ OUT - OUT^* $	600	700		mV
Output Common Mode Range	$(OUT + OUT^*) / 2$	$V_{CC} - 1.5$	$V_{CC} - 1.3$	$V_{CC} - 1.1$	V
<b>Power Supply</b>					
Power Supply Current	$I_{EE}$			132	mA

Test Conditions: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

### AC Characteristics

( $V_{CC} = 3.0V$  to  $3.6V$ ;  $V_{EE} = -3.6V$  to  $-3.0V$ ;  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay					
CLK to OUT (SEL = 0)	$T_{pd}$	485	630	785	ps
CLK to OUT (SEL = 1)	$T_{pd}$	300	450	600	ps
SEL to OUT	$T_{pd}$	300	450	600	ps
Channel to Channel Skew	$t_{SKEW}$			35	ps
Maximum Operating Frequency (Note 1)	$F_{max}$	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK					
Set Up Time	$T_s$	100			ps
Hold Time	$T_h$	100			ps
Output Rise and Fall Times (20% / 80%) (Note 1)	$T_r / T_f$		125	175	ps
Temperature Coefficient (Note 1)	$\Delta T_{pd} / \Delta T$		<1		ps / $^{\circ}C$

AC TEST CONDITIONS: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2.0V$ .

Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

#### Description

The SK1526 is an extremely fast, stable and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1526 has standard open emitter ECL outputs.

Target applications:

- High speed clock / data lines that require translation
- Multiple destination (daisy chain) applications

#### Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to ECL Translation
- Available in 32 pin, 5mm X5mm, TQFP Package

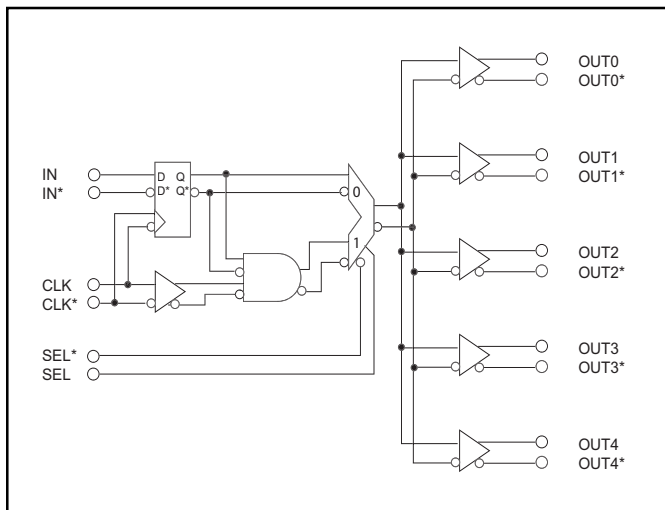
#### Application Notes

**AN1001** - EPIC Family Product Line

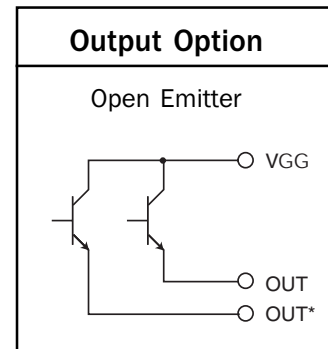
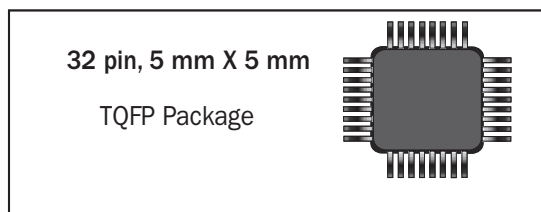
**AN1003** - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

**AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

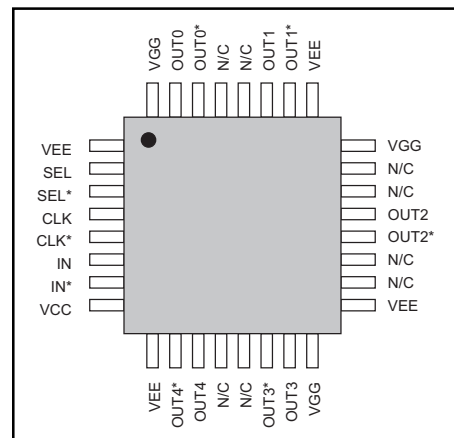
#### Functional Block Diagram



#### Package Information



#### Pin Description



## TEST AND MEASUREMENT PRODUCTS

### DC Characteristics

(V<sub>GG</sub> = - 0.1V to 2.0V; V<sub>CC</sub> = 2.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High	V <sub>IH</sub>	V <sub>EE</sub> + 2.0		V <sub>CC</sub>	V
Input Low	V <sub>IL</sub>	V <sub>EE</sub>		V <sub>CC</sub> - 0.2	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	V <sub>IH</sub> - V <sub>IL</sub>	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I <sub>IH</sub>	-5		+30	μA
Input Low Current	I <sub>IL</sub>	-6		+6	μA
Functional Inputs (IN / IN*, SEL / SEL*)					
Input Current	I <sub>IH</sub> , I <sub>IL</sub>	-500		+500	μA
<b>Outputs</b>					
Digital Output Voltage	OUT - OUT*	600	700		mV
Output Common Mode Range	(OUT + OUT*) / 2	V <sub>GG</sub> - 1.5	V <sub>GG</sub> - 1.3	V <sub>GG</sub> - 1.1	V
<b>Power Supply</b>					
Power Supply Current	I <sub>EE</sub> I <sub>CC</sub>			132 60	mA mA

Test Conditions: Outputs terminated with 50Ω to V<sub>GG</sub> - 2V

### AC Characteristics

(V<sub>GG</sub> = - 0.1V to 2.0V; V<sub>CC</sub> = 2.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay					
CLK to OUT (SEL = 0)	T <sub>pd</sub>	485	630	785	ps
CLK to OUT (SEL = 1)	T <sub>pd</sub>	300	450	600	ps
SEL to OUT	T <sub>pd</sub>	300	450	600	ps
Channel to Channel Skew	t <sub>SKEW</sub>			35	ps
Maximum Operating Frequency (Note 1)	F <sub>max</sub>	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK					
Set Up Time	T <sub>s</sub>	100			ps
Hold Time	T <sub>h</sub>	100			ps
Output Rise and Fall Times (20% / 80%)(Note 1)	T <sub>r</sub> / T <sub>f</sub>		125	175	ps
Temperature Coefficient(Note 1)	ΔT <sub>pd</sub> /ΔT		<2		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to V<sub>GG</sub> - 2.0V.

Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

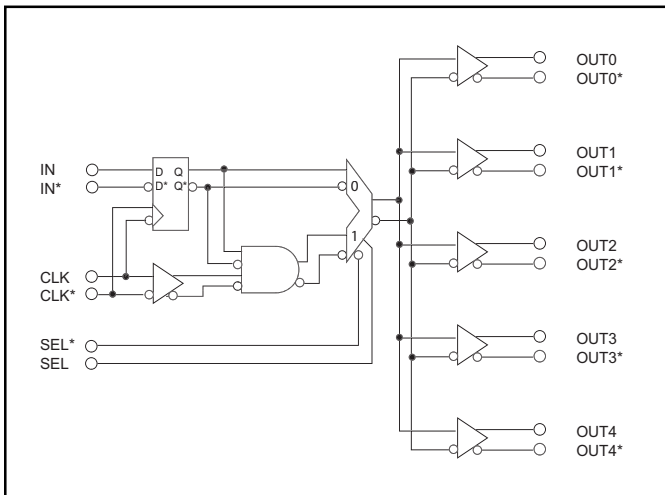
#### Description

The SK1527 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

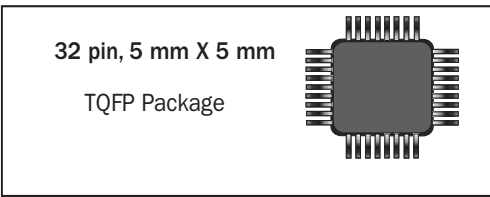
The SK1527 uses 50Ω outputs with source /sink capability, and is optimized for:

- High speed clock / data lines that require translation
- Point to point, double termination applications

#### Functional Block Diagram



#### Package Information

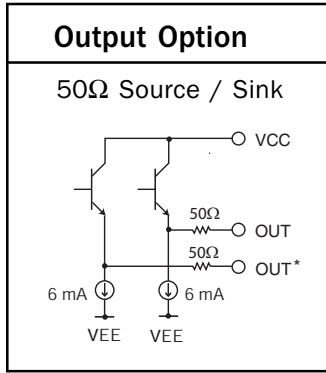


#### Features

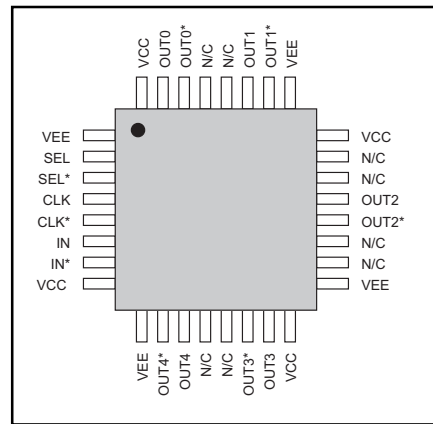
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Available in 32 pin, 5mm X5mm, TQFP Package

#### Application Notes

- AN1001** - EPIC Family Product Line
- AN1003** - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL



#### Pin Description



## TEST AND MEASUREMENT PRODUCTS

### DC Characteristics

(VCC = 3.0V to 3.6V; VEE = -3.6 to -3.0V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High Input Low	V <sub>IH</sub> V <sub>IL</sub>	VEE + 2.0 VEE		VCC VCC - 0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	V <sub>IH</sub> V <sub>IL</sub>	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	I <sub>IH</sub> I <sub>IL</sub>	-5 -6		+30 +6	μA μA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	I <sub>IH</sub> , I <sub>IL</sub>	-500		+500	μA
<b>Outputs</b>					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	OUT - OUT*   (OUT + OUT*) / 2 I <sub>SINK</sub> R <sub>OUT</sub>	600 VCC - 1.4 4 40	700 VCC - 1.2 6 50	VCC - 1.0 7.5 60	mV V mA Ω
<b>Power Supply</b>					
Power Supply Current	IEE			240	mA

Test Conditions: Outputs unterminated.

### AC Characteristics

(VCC = 3.0V to 3.6V; VEE = -3.6 to -3.0V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	T <sub>pd</sub> T <sub>pd</sub> T <sub>pd</sub>	490 300 300	690 500 500	890 700 700	ps ps ps
Channel to Channel Skew	t <sub>SKEW</sub>			35	ps
Maximum Operating Frequency (Note 1)	F <sub>max</sub>	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	T <sub>s</sub> T <sub>h</sub>	100 100			ps ps
Output Rise and Fall Times (20% / 80%)(Note 1)	T <sub>r</sub> / T <sub>f</sub>		125	175	ps
Temperature Coefficient(Note 1)	ΔT <sub>pd</sub> / ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to VCC-2.0V

Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

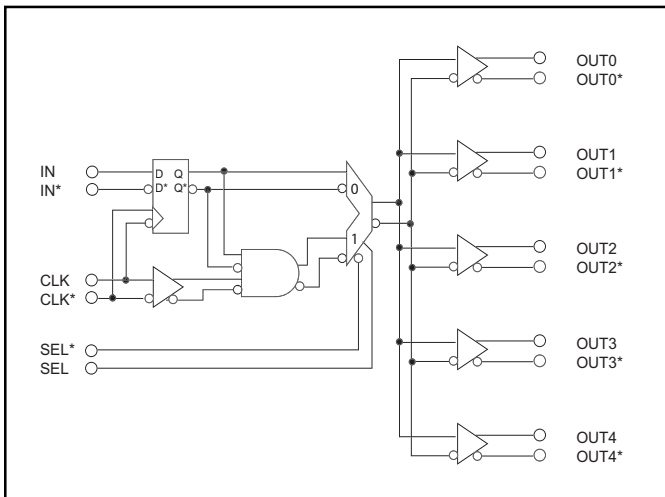
#### Description

The SK1528 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. It is also capable of receiving inputs of any technology and voltage level. The D - flip-flop is triggered on the falling edge of the clock.

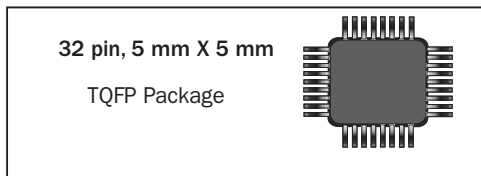
The SK1528 has 50Ω outputs with source /sink capability, and is optimized for:

- High speed clock / data lines that require translation
- Point to point, double termination applications

#### Functional Block Diagram



#### Package Information

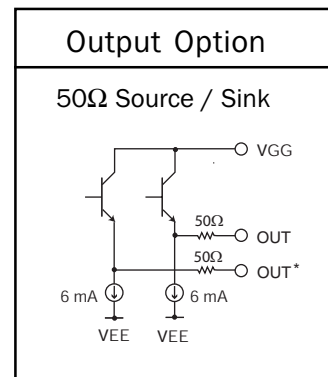


#### Features

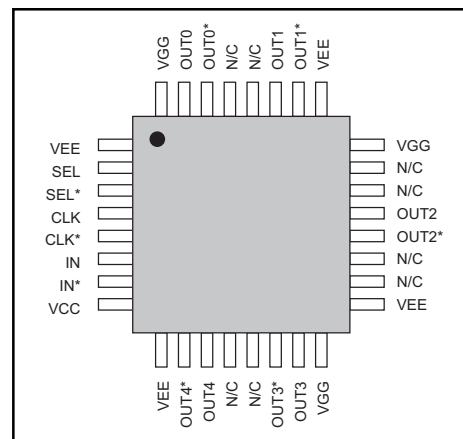
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to ECL Translation
- Available in 32 pin, 5mm X5mm, TQFP Package

#### Application Notes

- AN1001** - EPIC Family Product Line
- AN1003** - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL



#### Pin Description



## TEST AND MEASUREMENT PRODUCTS

### DC Characteristics

(V<sub>GG</sub> = - 0.1V to 2.0V; V<sub>CC</sub> = 2.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High	V <sub>IH</sub>	V <sub>EE</sub> + 2.0		V <sub>CC</sub>	V
Input Low	V <sub>IL</sub>	V <sub>EE</sub>		V <sub>CC</sub> - 0.2	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	V <sub>IH</sub> - V <sub>IL</sub>	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I <sub>IH</sub>	-5		+30	μA
Input Low Current	I <sub>IL</sub>	-6		+6	μA
Functional Inputs (IN / IN*, SEL / SEL*)					
Input Current	I <sub>IH</sub> , I <sub>IL</sub>	-500		+500	μA
<b>Outputs</b>					
Digital Output Voltage	OUT - OUT*	600	700		mV
Output Common Mode Range	(OUT + OUT*) / 2	V <sub>GG</sub> - 1.4	V <sub>GG</sub> - 1.2	V <sub>GG</sub> - 1.0	V
Internal Current Source	I <sub>SINK</sub>	4	6	7.5	mA
Output Impedance	R <sub>OUT</sub>	40	50	60	Ω
<b>Power Supply</b>					
Power Supply Current	I <sub>EE</sub> I <sub>CC</sub>			220 60	mA mA

Test Conditions: Outputs unterminated.

### AC Characteristics

(V<sub>GG</sub> = - 0.1V to 2.0V; V<sub>CC</sub> = 2.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay					
CLK to OUT (SEL = 0)	T <sub>pd</sub>	460	786	1100	ps
CLK to OUT (SEL = 1)	T <sub>pd</sub>	300	600	900	ps
SEL to OUT	T <sub>pd</sub>	300	600	900	ps
Channel to Channel Skew	t <sub>SKEW</sub>			35	ps
Maximum Operating Frequency (Note 1)	F <sub>max</sub>	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK					
Set Up Time	T <sub>s</sub>	100			ps
Hold Time	T <sub>h</sub>	100			ps
Output Rise and Fall Times (20% / 80%) (Note 1)	T <sub>r</sub> / T <sub>f</sub>		125	300	ps
Temperature Coefficient (Note 1)	ΔT <sub>pd</sub> / ΔT		<2		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to V<sub>GG</sub> -2.0V

Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

#### Description

The SK1529 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. It is also capable of receiving inputs of any technology and voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1529 uses 50Ω outputs with source /sink capability, and is optimized for:

- High speed clock / data lines that require translation
- Point to point, series termination applications

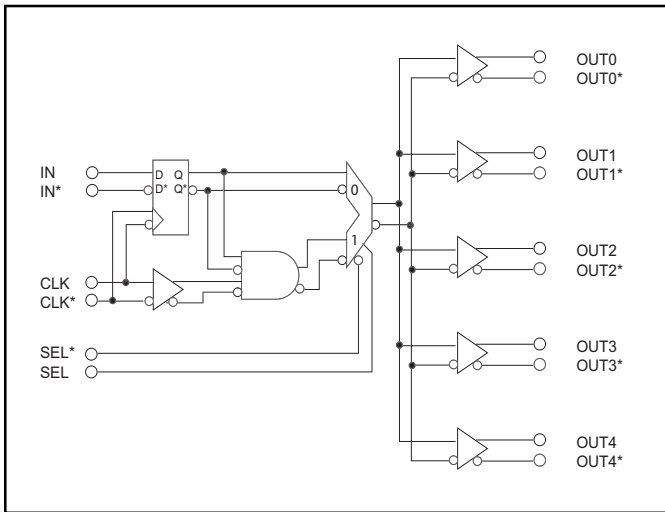
#### Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to PECL Translation
- Available in 32 pin, 5mm X5mm, TQFP Package

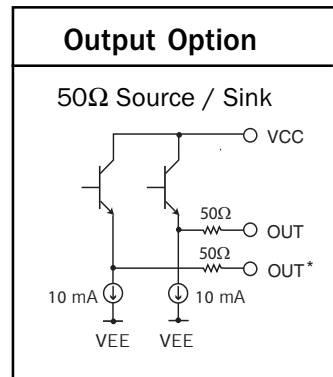
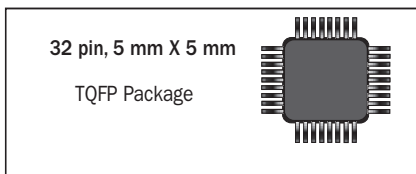
#### Application Notes

- AN1001** - EPIC Family Product Line
- AN1003** - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

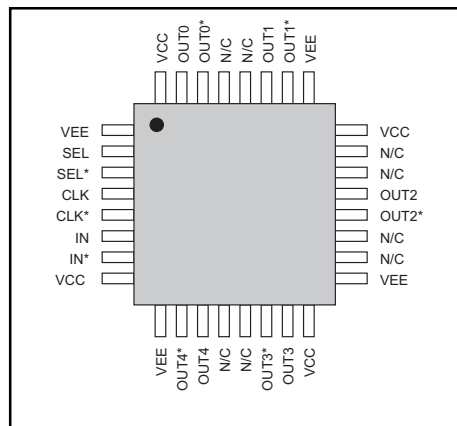
#### Functional Block Diagram



#### Package Information



#### Pin Description



## TEST AND MEASUREMENT PRODUCTS

### DC Characteristics

(V<sub>CC</sub> = 3.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High	V <sub>IH</sub>	V <sub>EE</sub> + 2.0		V <sub>CC</sub>	V
Input Low	V <sub>IL</sub>	V <sub>EE</sub>		V <sub>CC</sub> - 0.2	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	V <sub>IH</sub> - V <sub>IL</sub>	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current	I <sub>IH</sub>	-5		+30	μA
Input Low Current	I <sub>IL</sub>	-6		+6	μA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	I <sub>IH</sub> , I <sub>IL</sub>	-500		+500	μA
<b>Outputs</b>					
Digital Output Voltage	OUT - OUT*	600	700	V <sub>CC</sub> - 1.0	mV
Output Common Mode Range	(OUT + OUT*) / 2	V <sub>CC</sub> - 1.4	V <sub>CC</sub> - 1.2	V <sub>CC</sub> - 1.0	V
Internal Current Source	I <sub>SINK</sub>	7.5	10	13	mA
Output Impedance	R <sub>OUT</sub>	40	50	60	Ω
<b>Power Supply</b>					
Power Supply Current	I <sub>EE</sub>			250	mA

Test Conditions: Outputs unterminated.

### AC Characteristics

(V<sub>CC</sub> = 3.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay CLK to OUT (SEL = 0)	T <sub>pd</sub>	490	690	890	ps
CLK to OUT (SEL = 1)	T <sub>pd</sub>	300	500	700	ps
SEL to OUT	T <sub>pd</sub>	300	500	700	ps
Channel to Channel Skew	t <sub>SKEW</sub>			35	ps
Maximum Operating Frequency (Note 1)	F <sub>max</sub>	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time	T <sub>s</sub>	100			ps
Hold Time	T <sub>h</sub>	100			ps
Output Rise and Fall Times (20% / 80%) (Note 1)	T <sub>r</sub> / T <sub>f</sub>		125	200	ps
Temperature Coefficient (Note 1)	ΔT <sub>pd</sub> / ΔT		<2		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to V<sub>CC</sub>-2.0V  
 Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

#### Description

The SK1530 is an extremely fast, stable and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1530 uses 50Ω outputs with source /sink capability, and is optimized for:

- High speed clock / data lines that require translation
- Point to point, series termination applications

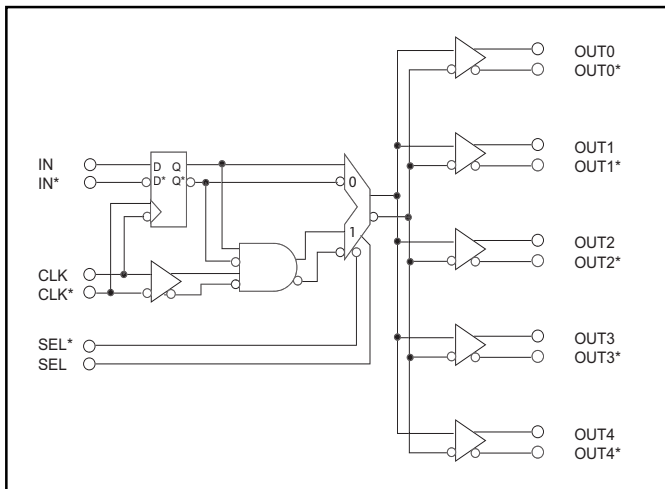
#### Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to ECL Translation
- Available in 32 pin, 5mm X5mm, TQFP Package

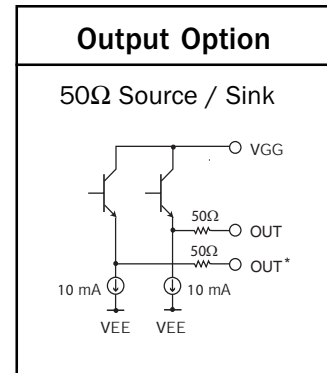
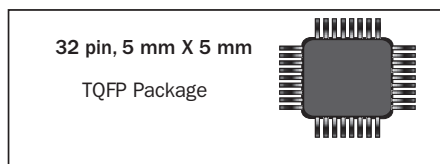
#### Application Notes

- AN1001** - EPIC Family Product Line
- AN1003** - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

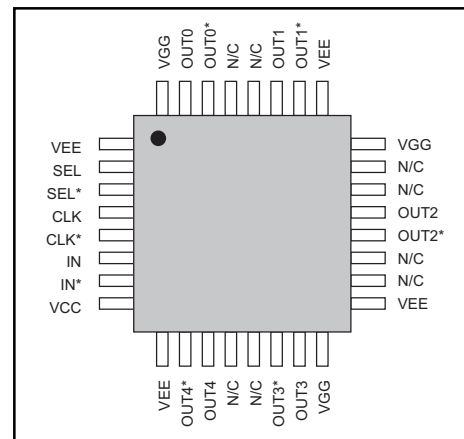
#### Functional Block Diagram



#### Package Information



#### Pin Description



### TEST AND MEASUREMENT PRODUCTS

#### DC Characteristics

(V<sub>GG</sub> = -0.1V to 2.0V; V<sub>CC</sub> = 2.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	V <sub>IH</sub>	V <sub>EE</sub> + 2.0		V <sub>CC</sub>	V
Input Low	V <sub>IL</sub>	V <sub>EE</sub>		V <sub>CC</sub> - 0.2	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	V <sub>IH</sub> - V <sub>IL</sub>	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I <sub>IH</sub>	-5		+30	μA
Input Low Current	I <sub>IL</sub>	-6		+6	μA
Functional Inputs (IN / IN*, SEL / SEL*)					
Input Current	I <sub>IH</sub> , I <sub>IL</sub>	-500		+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	700		mV
Output Common Mode Range	(OUT + OUT*) / 2	V <sub>GG</sub> - 1.4	V <sub>GG</sub> - 1.2	V <sub>GG</sub> - 1.0	V
Internal Current Source	I <sub>SINK</sub>	7.5	10	13	mA
Output Impedance	R <sub>OUT</sub>	40	50	60	Ω
Power Supply					
Power Supply Current	I <sub>EE</sub> I <sub>CC</sub>	2.0		375 60	mA mA

Test Conditions: Outputs unterminated.

#### AC Characteristics

(V<sub>GG</sub> = -0.1V to 2.0V; V<sub>CC</sub> = 2.0V to 3.6V; V<sub>EE</sub> = -3.6V to -3.0V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
CLK to OUT (SEL = 0)	T <sub>pd</sub>	460	480	1100	ps
CLK to OUT (SEL = 1)	T <sub>pd</sub>	300	600	900	ps
SEL to OUT	T <sub>pd</sub>	300	600	900	ps
Channel to Channel Skew	t <sub>SKEW</sub>			35	ps
Maximum Operating Frequency (Note 1)	F <sub>max</sub>	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK					
Set Up Time	T <sub>s</sub>	100			ps
Hold Time	T <sub>h</sub>	100			ps
Output Rise and Fall Times (20% / 80%) (Note 1)	T <sub>r</sub> / T <sub>f</sub>		125	300	ps
Temperature Coefficient (Note 1)	ΔT <sub>pd</sub> / ΔT		<2		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to V<sub>GG</sub> -2.0V

Note 1: Guaranteed by characterization. Not production tested.

### TEST AND MEASUREMENT PRODUCTS

#### Description

The SK1599 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1599 has open collector (CML) outputs, targeted for:

- Ultra high speed applications
- Adjustable common mode levels at the destination.

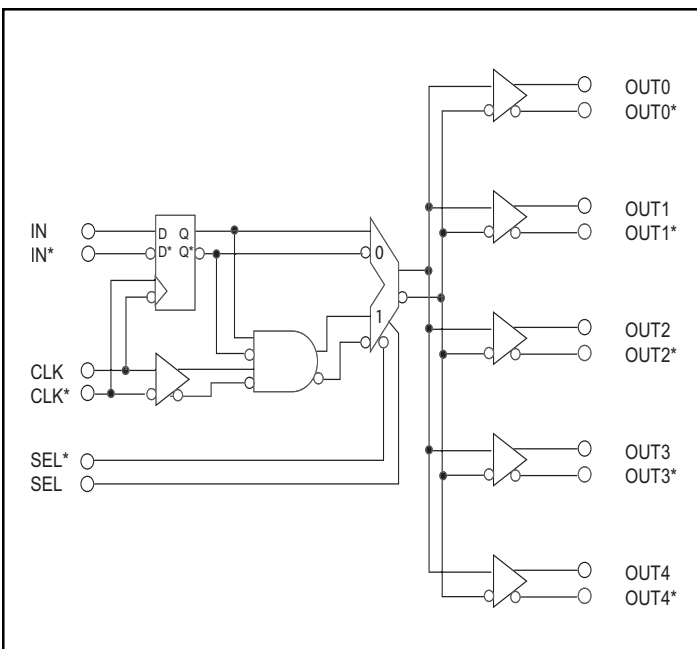
#### Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible
- Available in 32 lead, 5mm X5mm, TQFP Package

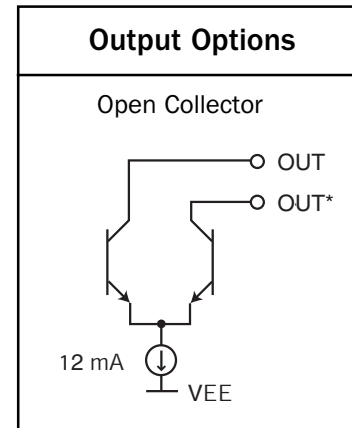
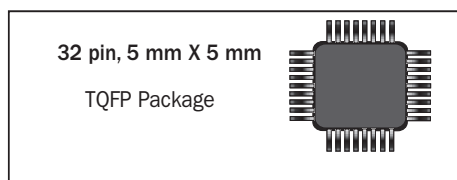
#### Application Notes

- AN1001** - EPIC Family Product Line
- AN1003** - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
- AN1004** - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL
- AN1008** - Interfacing with CML

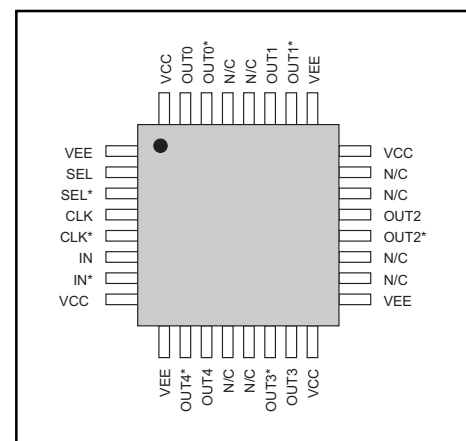
#### Functional Block Diagram



#### Package Information



#### Pin Description



## TEST AND MEASUREMENT PRODUCTS

### DC Characteristics

(V<sub>CC</sub> - V<sub>EE</sub> = 3.0V to 5.5V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>Inputs</b>					
Input High	V <sub>IH</sub>	V <sub>EE</sub> + 2.0		V <sub>CC</sub>	V
Input Low	V <sub>IL</sub>	V <sub>EE</sub>		V <sub>CC</sub> - 0.2	V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	V <sub>IH</sub> - V <sub>IL</sub>	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current	I <sub>IH</sub>	-5		+30	μA
Input Low Current	I <sub>IL</sub>	-6		+6	μA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	I <sub>IH</sub> , I <sub>IL</sub>	-500		+500	μA
<b>Outputs</b>					
Output Current High	I <sub>OZ</sub>	-500	0	+500	μA
Output Current Low	I <sub>OL</sub>	9	12	15	mA
<b>Power Supply</b>					
Power Supply Current	I <sub>EE</sub>		145	225	mA

Test Conditions: Outputs terminated with 50Ω to V<sub>CC</sub>.

### AC Characteristics

(V<sub>CC</sub> - V<sub>EE</sub> = 3.0V to 5.5V; T<sub>A</sub> = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
<b>High Performance Option</b>					
Propagation Delay CLK to OUT (SEL = 0)	T <sub>pd</sub>	485	630	785	ps
CLK to OUT (SEL = 1)	T <sub>pd</sub>	300	450	600	ps
SEL to OUT	T <sub>pd</sub>	300	450	600	ps
Channel to Channel Skew	t <sub>SKEW</sub>			35	ps
Maximum Operating Frequency (Note 1)	F <sub>max</sub>	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time	T <sub>s</sub>	100			ps
Hold Time	T <sub>h</sub>	100			ps
Output Rise and Fall Times (20% / 80%) (Note 1)	T <sub>r</sub> / T <sub>f</sub>		125	250	ps
Temperature Coefficient (Note 1)	ΔT <sub>pd</sub> / ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to V<sub>CC</sub>

Note 1: Guaranteed by characterization. Not production tested.

**TEST AND MEASUREMENT PRODUCTS****Ordering Information**

Ordering Code	Package ID
SK1500ATF	32 - TQFP 5 X 5 mm
SK1501ATF	32 - TQFP 5 X 5 mm
SK1502ATF	32 - TQFP 5 X 5 mm
SK1503ATF	32 - TQFP 5 X 5 mm
SK1504ATF	32 - TQFP 5 X 5 mm
SK1525ATF	32 - TQFP 5 X 5 mm
SK1526ATF	32 - TQFP 5 X 5 mm
SK1527ATF	32 - TQFP 5 X 5 mm
SK1528ATF	32 - TQFP 5 X 5 mm
SK1529ATF	32 - TQFP 5 X 5 mm
SK1530ATF	32 - TQFP 5 X 5 mm
SK1599ATF	32 - TQFP 5 X 5 mm

**Notes:**

1. For Tape and Reel, add the letter "T" at the end of Ordering Code.
2. For Tape and Reel information, see TMD Part Ordering Information Data Sheet.

**Contact Information**

Semtech Corporation  
Test and Measurement Division  
10021 Willow Creek Rd., San Diego, CA 92131  
Phone: (858) 695-1808 FAX: (858) 695-2633