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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2738

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

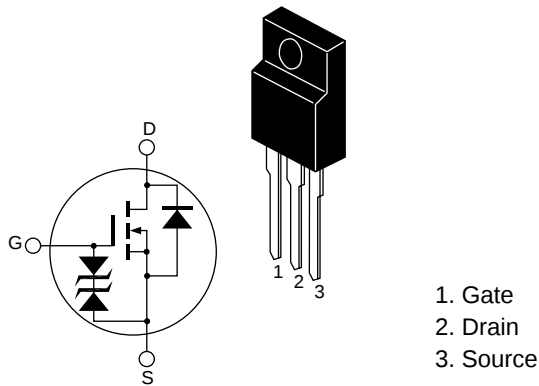
ADE-208-483 (Z)
1st. Edition
Jun 1997

Features

- Low on-resistance
 $R_{DS} = 15 \text{ m}\Omega$ typ
- High speed switching
- 4V gate drive device can be driven from 5V source

Outline

TO-220CFM



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	40	A
Drain peak current	I _{D(pulse)} ^{*1}	160	A
Body to drain diode reverse drain current	I _{DR}	40	A
Avalanche current	I _{AP} ^{*3}	40	A
Avalanche Energy	E _{AR} ^{*3}	137	mJ
Channel dissipation	Pch ^{*2}	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

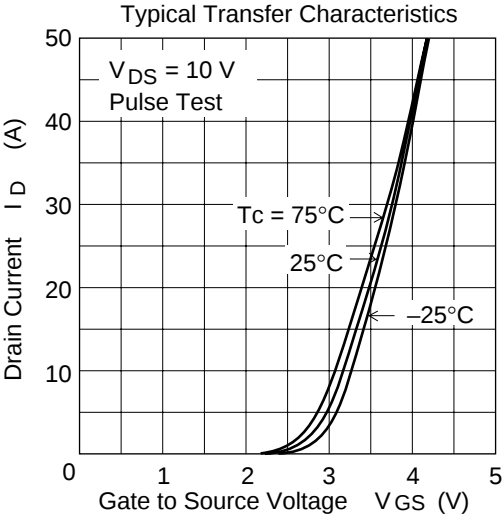
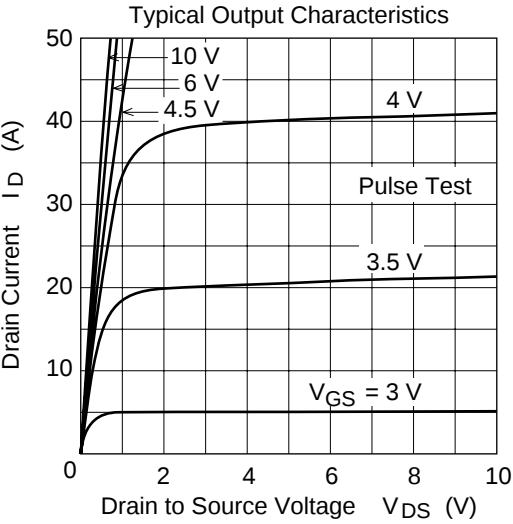
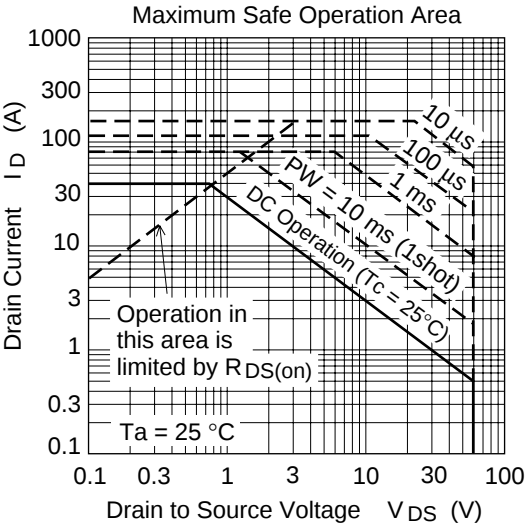
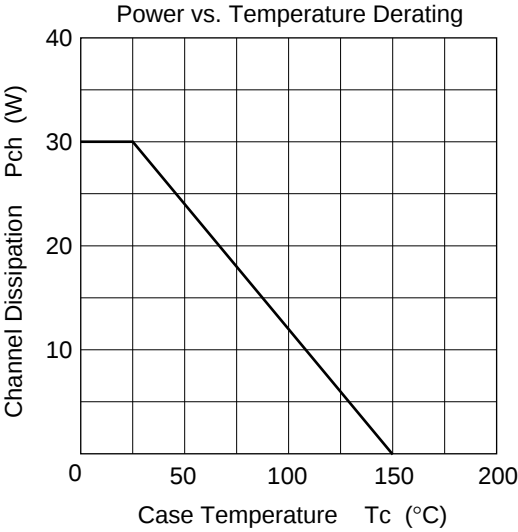
Notes: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg 50 Ω

Electrical Characteristics (Ta = 25°C)

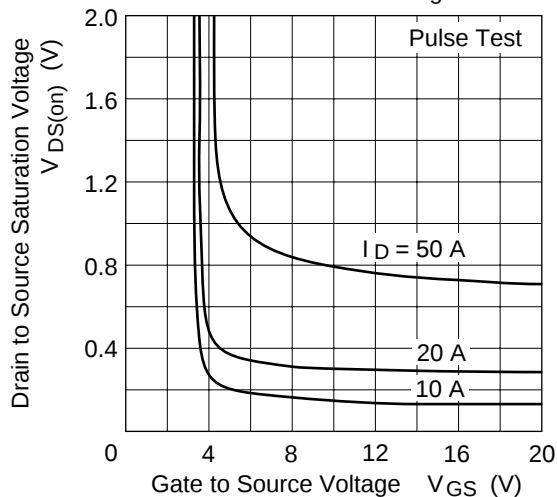
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60\text{V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1\text{mA}$, $V_{DS} = 10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	15	20	$\text{m}\Omega$	$I_D = 20\text{A}$, $V_{GS} = 10\text{V}^{*1}$
	$R_{DS(on)}$	—	25	40	$\text{m}\Omega$	$I_D = 20\text{A}$, $V_{GS} = 4\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	20	35	—	S	$I_D = 20\text{A}$, $V_{DS} = 10\text{V}^{*1}$
Input capacitance	C_{iss}	—	1500	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	C_{oss}	—	720	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	200	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$I_D = 20\text{A}$, $V_{GS} = 10\text{V}$
Rise time	t_r	—	180	—	ns	$R_L = 1.5\Omega$
Turn-off delay time	$t_{d(off)}$	—	200	—	ns	
Fall time	t_f	—	200	—	ns	
Body to drain diode forward voltage	VDF	—	0.95	—	V	$I_F = 40\text{A}$, $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$
Body to drain diode reverse recovery time	t_{rr}	—	70	—	V	$I_F = 40\text{A}$, $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

Note: 1. Pulse test

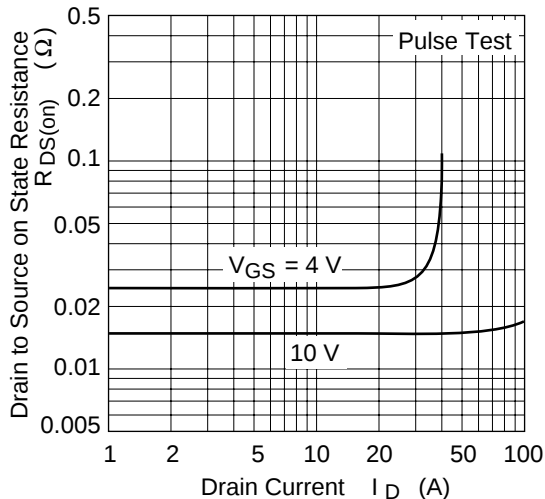
Main Characteristics



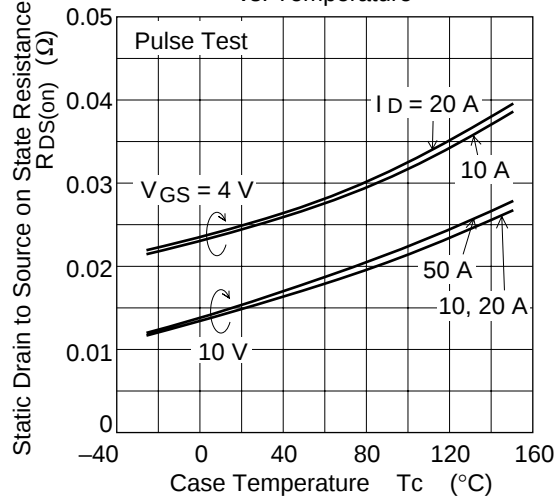
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



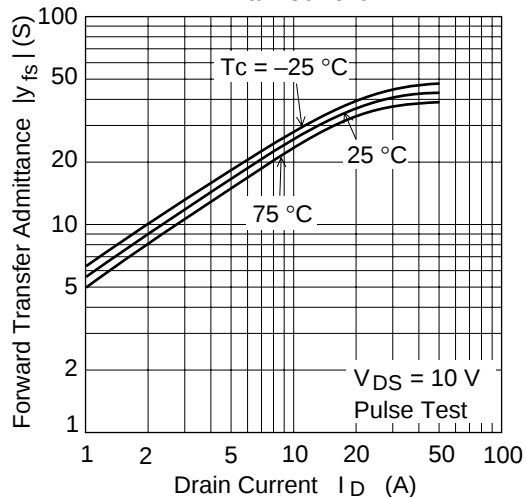
Static Drain to Source on State Resistance
vs. Drain Current



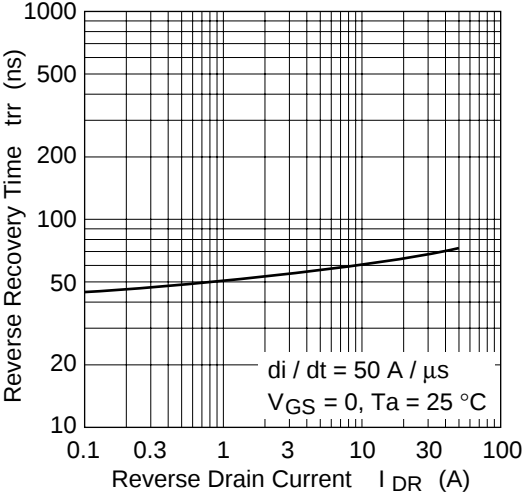
Static Drain to Source on State Resistance
vs. Temperature



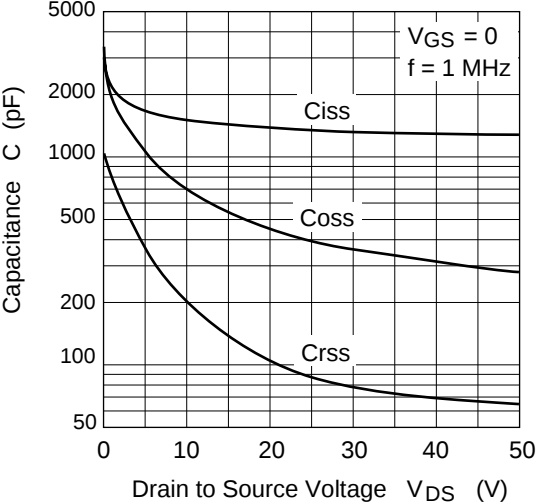
Forward Transfer Admittance vs.
Drain Current



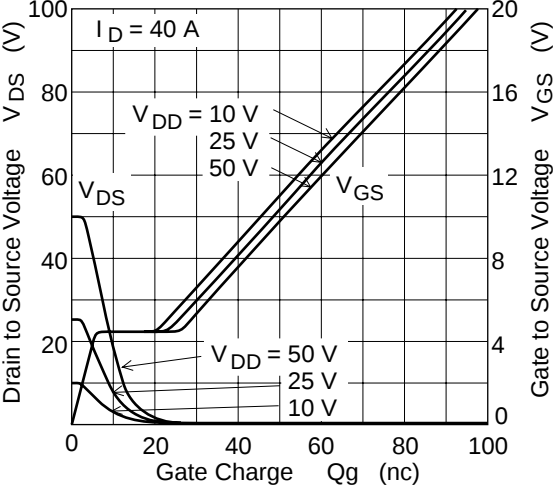
Body to Drain Diode Reverse Recovery Time



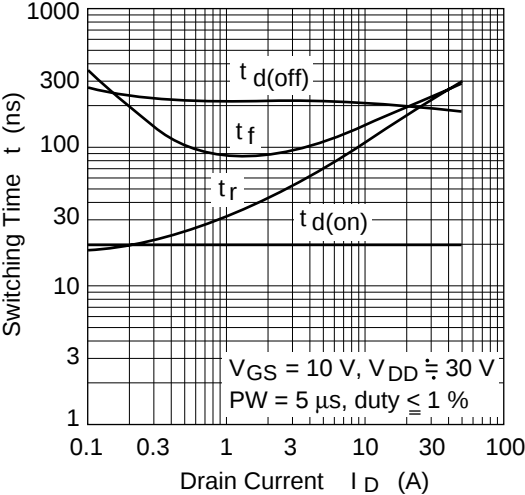
Typical Capacitance vs. Drain to Source Voltage

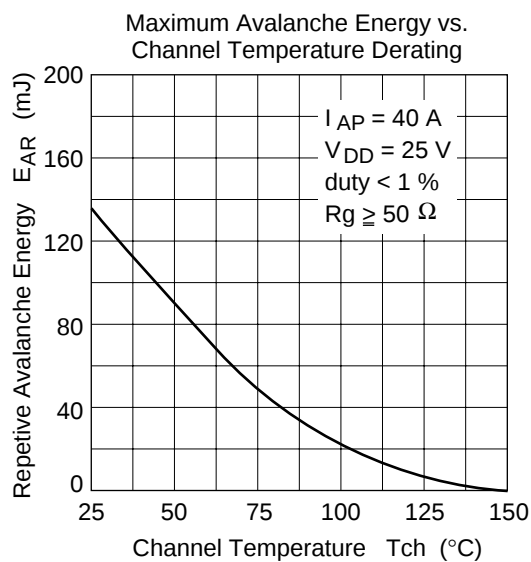
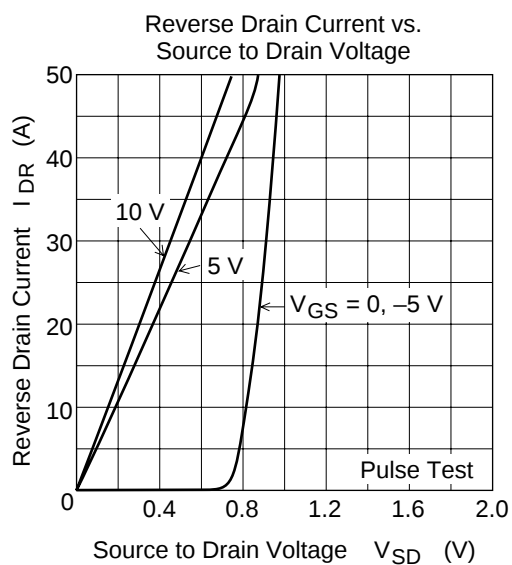


Dynamic Input Characteristics

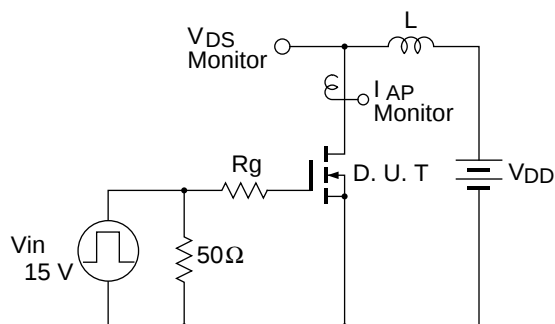


Switching Characteristics



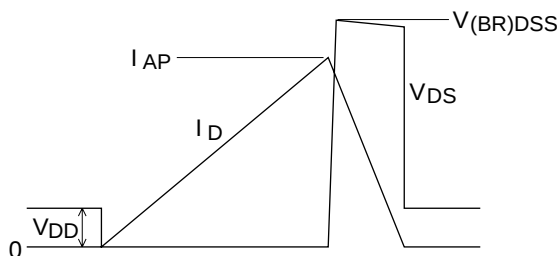


Avalanche Test Circuit

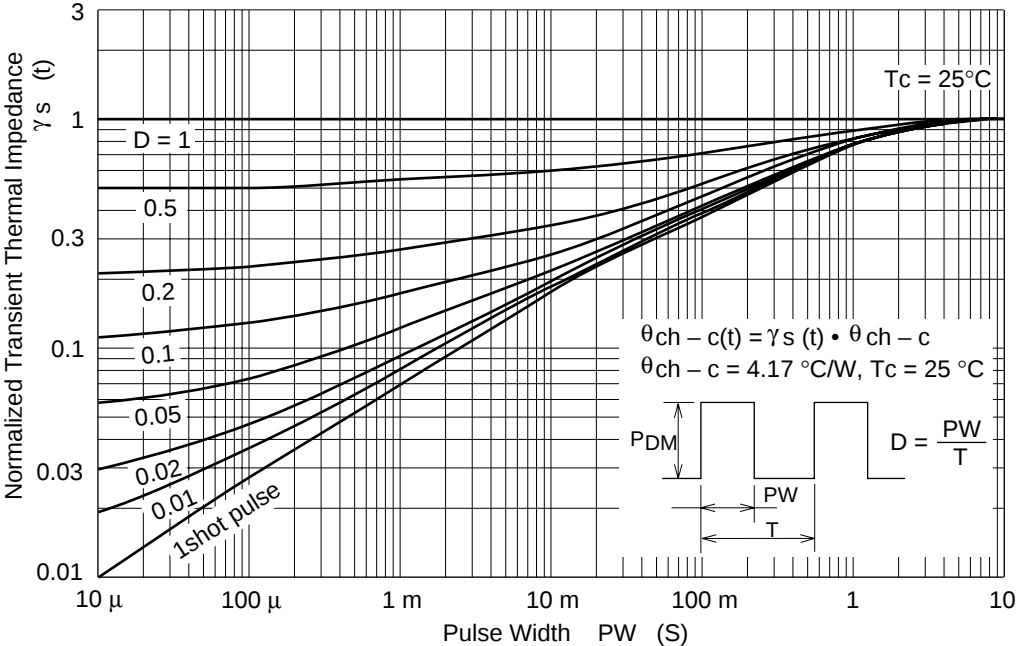


Avalanche Waveform

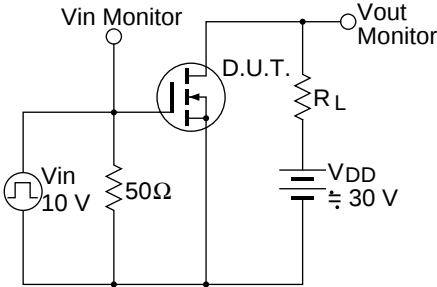
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



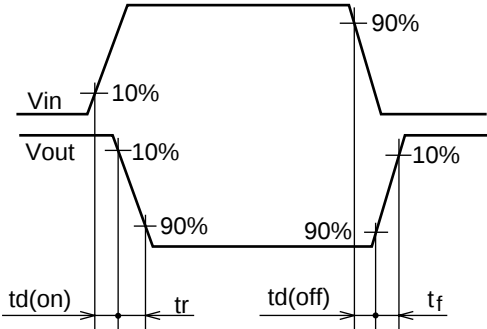
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



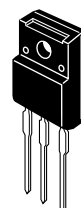
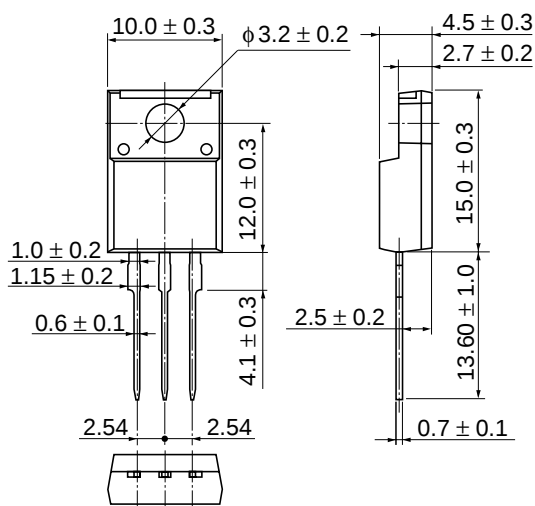
Switching Time Waveforms



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	TO-220CFM
JEDEC	—
EIAJ	—
Mass (reference value)	1.9 g

Cautions

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