

To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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H5N2005DL, H5N2005DS

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

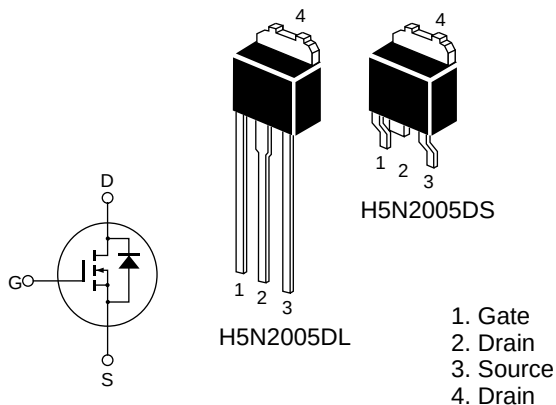
ADE-208-1373 (Z)
Target Specification 1st. Edition
Mar. 2001

Features

- Low on-resistance
- Low drive current
- High speed switching

Outline

DPAK-2



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	(6)	A
Drain peak current	$I_{D (pulse)}^{Note 1}$	(24)	A
Body-drain diode reverse drain current	I_{DR}	(6)	A
Body-drain diode reverse drain peak current	$I_{DR (pulse)}^{Note 1}$	(24)	A
Channel dissipation	$P_{ch}^{Note 2}$	25	W
Channel to case thermal impedance	θ_{ch-c}	5	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ C$

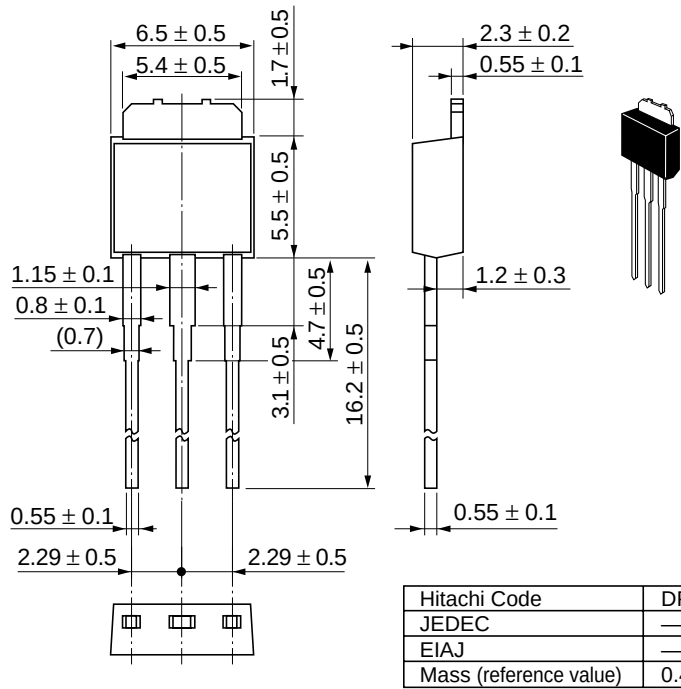
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	(3.0)	—	(4.5)	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.52)	(0.65)	Ω	$I_D = 3 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	(2.0)	(3.4)	—	S	$I_D = 3 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	(300)	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	(50)	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	(14)	—	pF	$f = 1 \text{ MHz}$
Total Gate charge	Q_g	—	(9.5)	—	nC	$V_{DD} = 160 \text{ V}$
Gate to source charge	Q_{gs}	—	(1.8)	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	(5.2)	—	nC	$I_D = 6 \text{ A}$
Turn-on delay time	$t_d(on)$	—	(19)	—	ns	$I_D = 3 \text{ A}$
Rise time	t_r	—	(16)	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_d(off)$	—	(44)	—	ns	$R_L = 33.3 \Omega$
Fall time	t_f	—	(12)	—	ns	$R_g = 10 \Omega$
Body-drain diode forward voltage	V_{DF}	—	(1.0)	(1.5)	V	$I_F = 6 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	(90)	—	ns	$I_F = 6 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery charge	Q_{rr}	—	(300)	—	nC	$diF/dt = 100 \text{ A/us}$

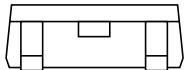
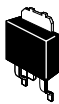
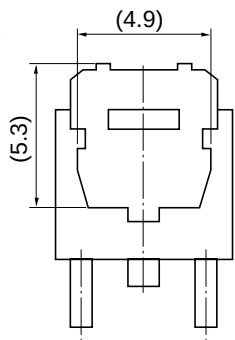
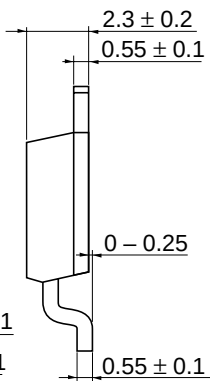
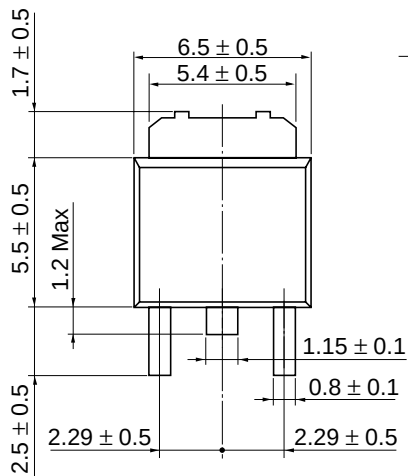
Note: 4. Pulse test

Package Dimensions

As of January, 2001
Unit: mm

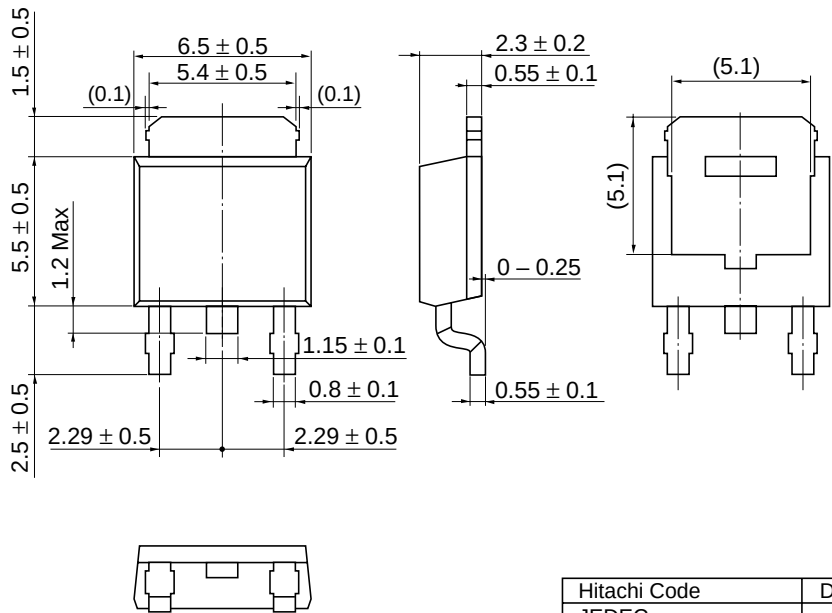


As of January, 2001
Unit: mm



Hitachi Code	DPAK (S)-(1),(2)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

As of January, 2001
Unit: mm



Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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