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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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HAT1036R

Silicon P Channel Power MOS FET Power Switching

RENESAS

ADE-208-662E (Z)

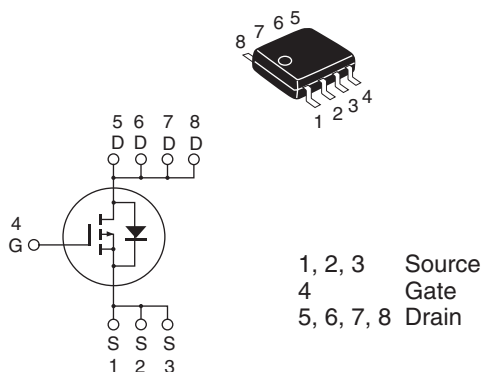
6th. Edition
Dec. 2002

Features

- Low on-resistance
 $R_{DS(on)} = 11\text{ m}\Omega$ typ
- Capable of -4 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	-12	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-96	A
Body-drain diode reverse drain current	I_{DR}	-12	A
Channel dissipation	Pch ^{Note2}	2.5	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \bullet 10 s$

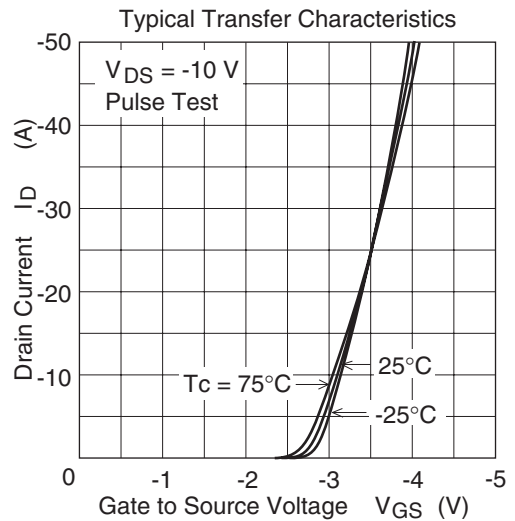
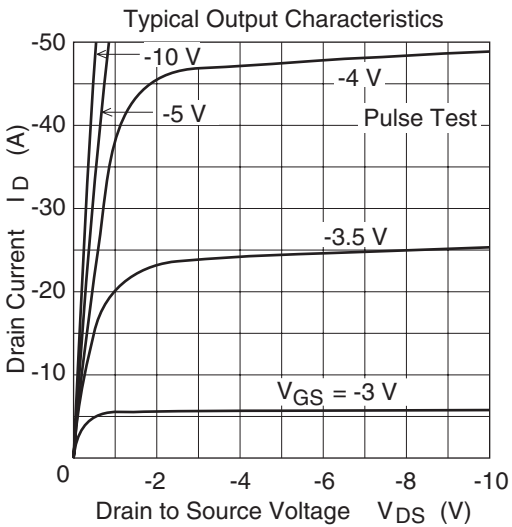
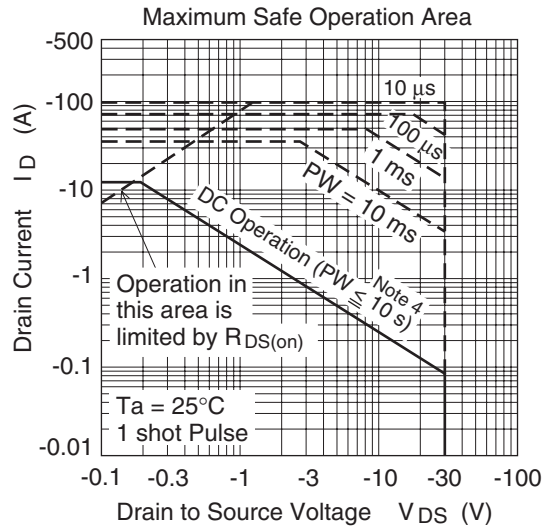
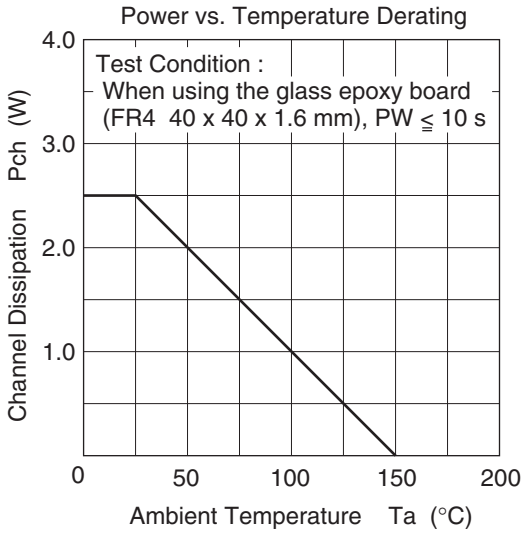
Electrical Characteristics

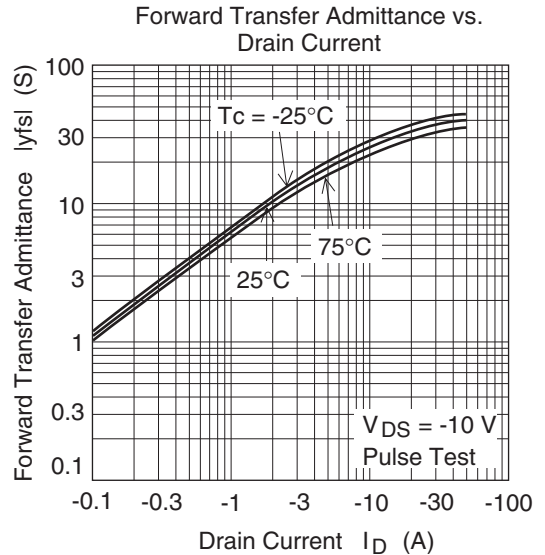
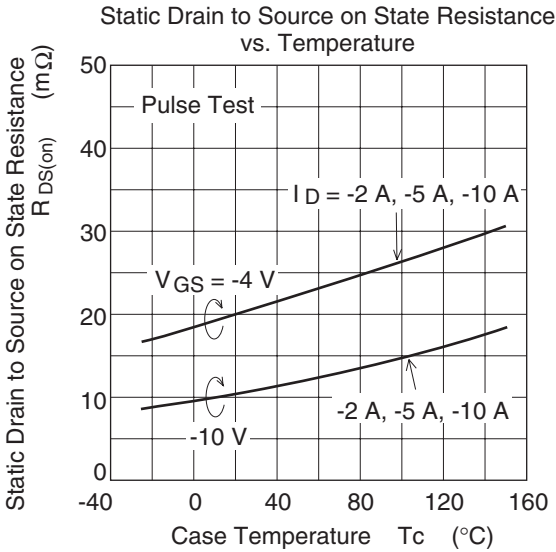
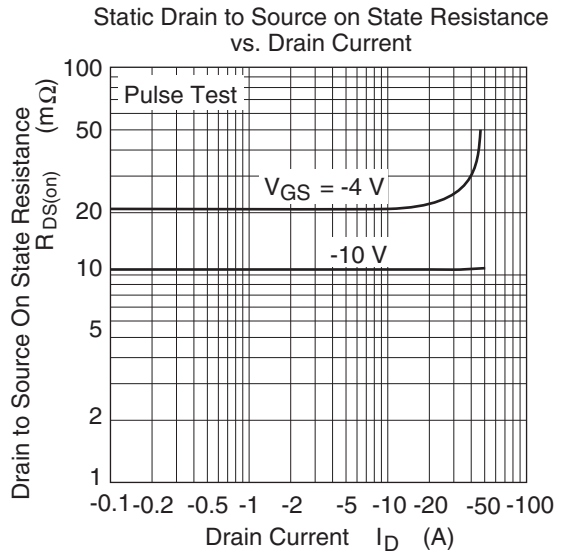
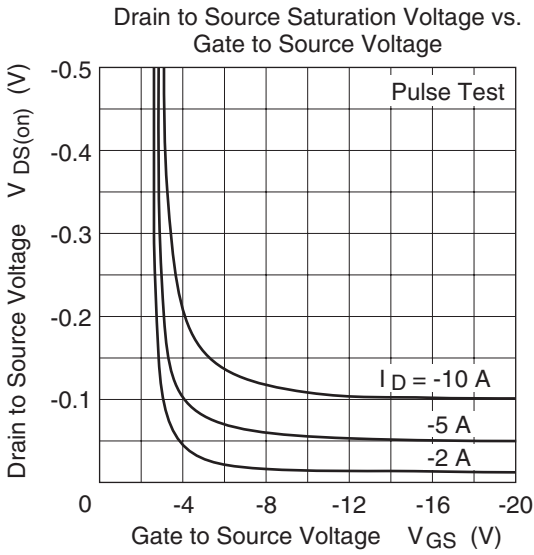
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	11	14	mΩ	$I_D = -6 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note1}
	$R_{DS(on)}$	—	21	34	mΩ	$I_D = -6 \text{ A}$, $V_{GS} = -4 \text{ V}$ ^{Note1}
Forward transfer admittance	$ y_{fs} $	12	20	—	S	$I_D = -6 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note1}
Input capacitance	Ciss	—	4200	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	Coss	—	870	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	360	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	70	—	nc	$V_{DD} = -10 \text{ V}$
Gate to source charge	Qgs	—	12	—	nc	$V_{GS} = -10 \text{ V}$
Gate to drain charge	Qgd	—	14	—	nc	$I_D = -12 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	120	—	ns	$V_{GS} = -4 \text{ V}$, $I_D = -6 \text{ A}$
Rise time	t_r	—	350	—	ns	$V_{DD} \cong -10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	100	—	ns	
Fall time	t_f	—	120	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.85	-1.11	V	$I_F = -12 \text{ A}$, $V_{GS} = 0$ ^{Note1}
Body-drain diode reverse recovery time	t_{rr}	—	55	—	ns	$I_F = -12 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 20 \text{ A}/\mu\text{s}$

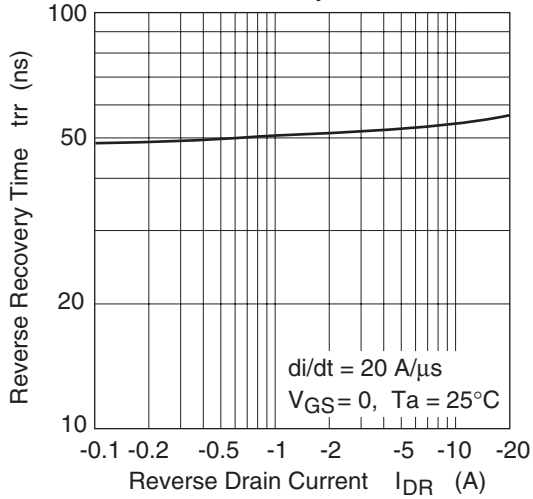
Note: 1. Pulse test

Main Characteristics

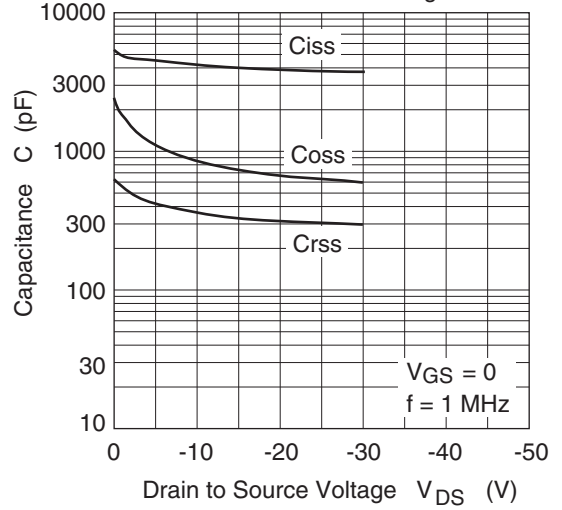




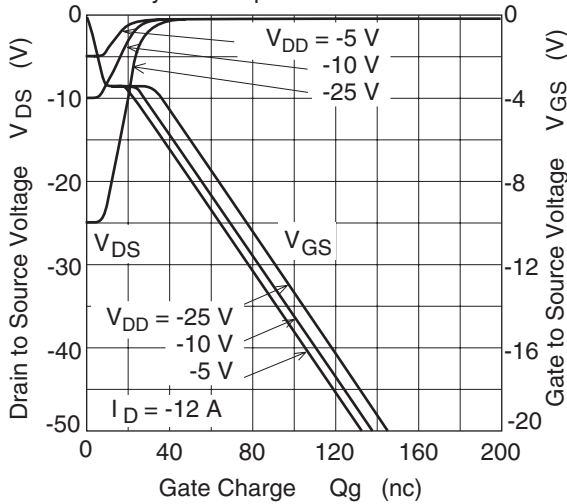
Body-Drain Diode Reverse Recovery Time



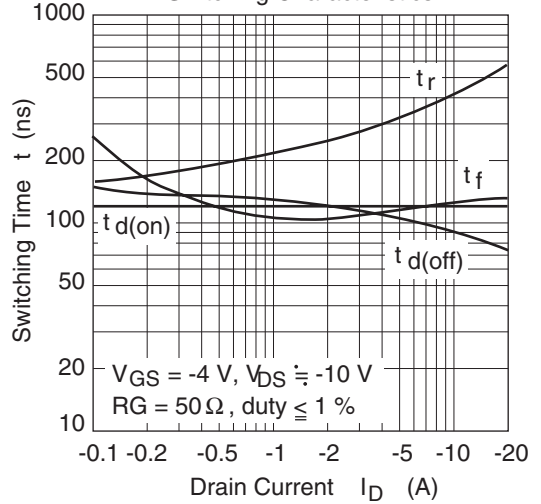
Typical Capacitance vs. Drain to Source Voltage

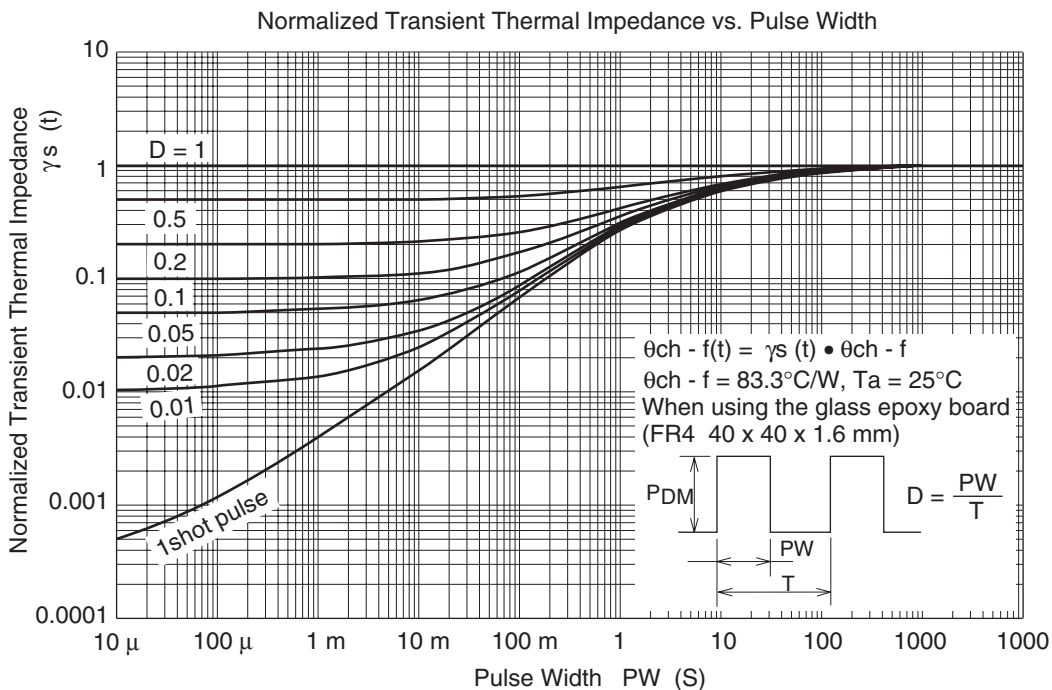
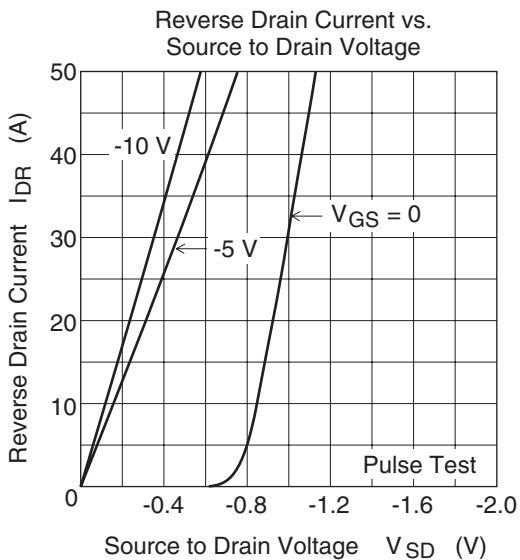


Dynamic Input Characteristics

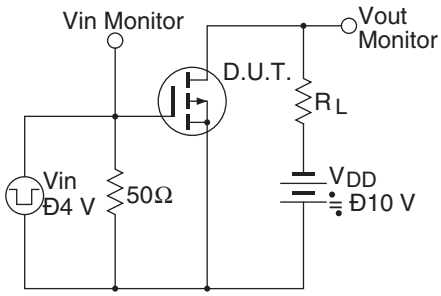


Switching Characteristics

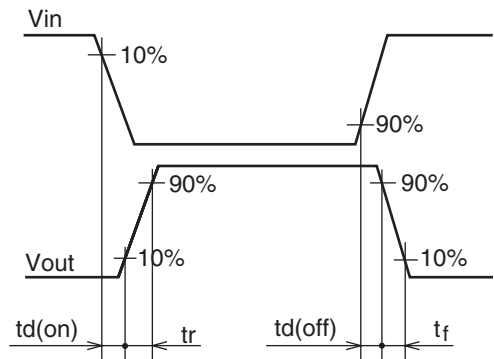




Switching Time Test Circuit

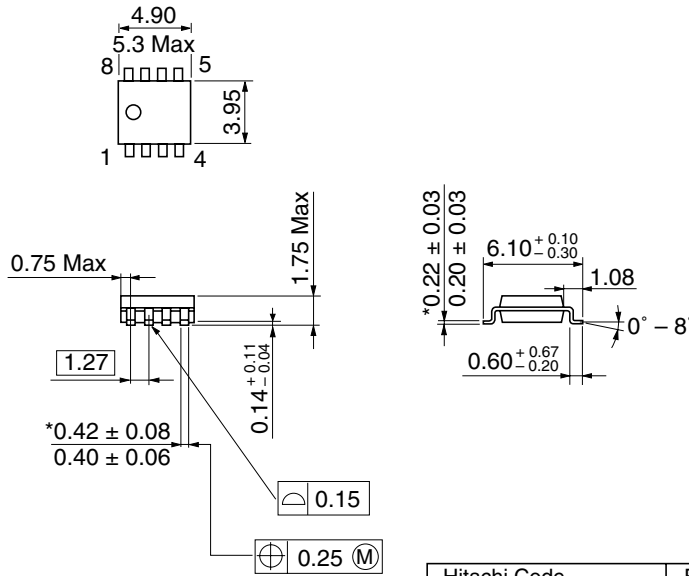


Switching Time Waveforms



Package Dimensions

As of July, 2002
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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