

OptiMOS[®]-P Small-Signal-Transistor

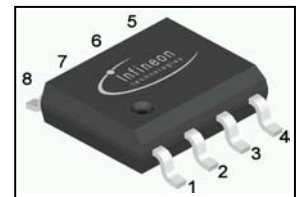
Features

- P-Channel
- Enhancement mode
- Logic level
- 150°C operating temperature
- Avalanche rated
- dv/dt rated
- Ideal for fast switching buck converter

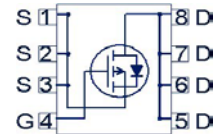
Product Summary

V_{DS}	-30	V
$R_{DS(on),max}$	13	mΩ
I_D	-11.3	A

P-DSO-8



Type	Package	Ordering Code	Marking
BSO130P03S	P-DSO-8	Q67042-S4233	130P3S



Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			≤10 secs	steady state	
Continuous drain current	I_D	$T_A=25\text{ °C}^{(1)}$	-11.3	-9.2	A
		$T_A=70\text{ °C}^{(1)}$	-9.1	-7.4	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}^{(2)}$	-45		
Avalanche energy, single pulse	E_{AS}	$I_D=11.3\text{ A}$, $R_{GS}=25\text{ Ω}$	148		mJ
Reverse diode dv/dt	dv/dt	$I_D=11.3\text{ A}$, $V_{DS}=20\text{ V}$, $di/dt=-200\text{ A/μs}$, $T_{j,max}=150\text{ °C}$	-6		kV/μs
Gate source voltage	V_{GS}		±25		V
Power dissipation	P_{tot}	$T_A=25\text{ °C}^{(1)}$	2.36	1.56	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - soldering point	R_{thJS}		-	-	35	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, $t_p \leq 10$ s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm ² cooling area ¹⁾ , $t_p \leq 10$ s	-	-	53	
		6 cm ² cooling area ¹⁾ , steady state	-	-	80	

Electrical characteristics, at $T_j = 25$ °C, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ μ A	-30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -140$ μ A	-1	-1.5	-2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_j = 25$ °C	-	-0.1	-1	μ A
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_j = 125$ °C	-	-10	-100	
Gate-source leakage current	I_{GSS}	$V_{GS} = -25$ V, $V_{DS} = 0$ V	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -11.3$ A	-	9.9	13.0	m Ω
Transconductance	g_{fs}	$ V_{DS} > 2 I_D R_{DS(on)max}$, $I_D = -9.5$ A	14	27	-	S

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μ m thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V},$ $V_{DS}=-25\text{ V}, f=1\text{ MHz}$	-	2650	3520	pF
Output capacitance	C_{oss}		-	708	942	
Reverse transfer capacitance	C_{rss}		-	580	870	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-15\text{ V},$ $V_{GS}=-10\text{ V},$ $I_D=-1\text{ A}, R_G=6\ \Omega$	-	13	20	ns
Rise time	t_r		-	16	24	
Turn-off delay time	$t_{d(off)}$		-	70	105	
Fall time	t_f		-	62	93	

Gate Charge Characteristics³⁾

Gate to source charge	Q_{gs}	$V_{DD}=-24\text{ V}, I_D=11.3\text{ A},$ $V_{GS}=0\text{ to }-10\text{ V}$	-	-7	-9	nC
Gate charge at threshold	$Q_{g(th)}$		-	-3.7	-5.0	
Gate to drain charge	Q_{gd}		-	-21	-32	
Switching charge	Q_{sw}		-	-25	-36	
Gate charge total	Q_g		-	-61	-81	
Gate plateau voltage	$V_{plateau}$		-	-2.6	-	V
Output charge	Q_{oss}	$V_{DD}=-15\text{ V}, V_{GS}=0\text{ V}$	-	-22	-29	

Reverse Diode

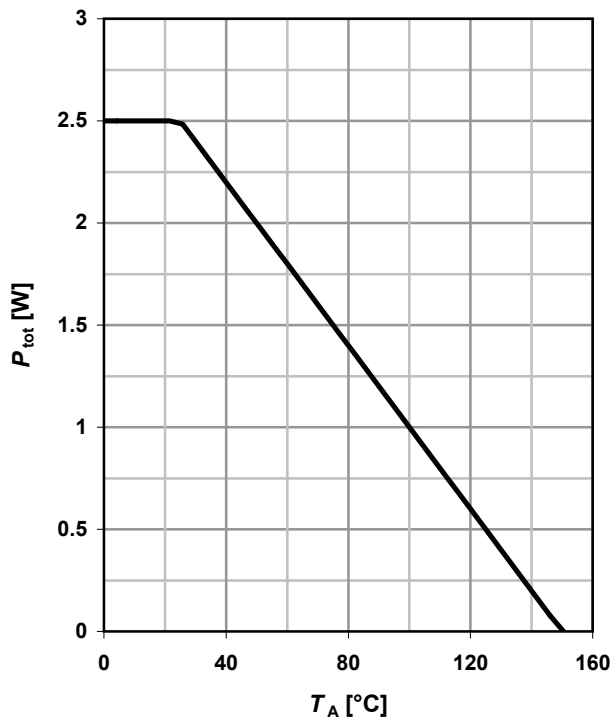
Diode continuous forward current	I_S	$T_A=25\text{ °C}$	-	-	-2.1	A
Diode pulse current	$I_{S,pulse}$		-	-	-45	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=-11.3\text{ A},$ $T_J=25\text{ °C}$	-	-0.84	-1.2	V
Reverse recovery time	t_{rr}	$V_R=15\text{ V}, I_F=-11.3\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	26	33	ns
Reverse recovery charge	Q_{rr}		-	16	20	nC

²⁾ See figure 3

³⁾ See figure 16 for gate charge parameter definition

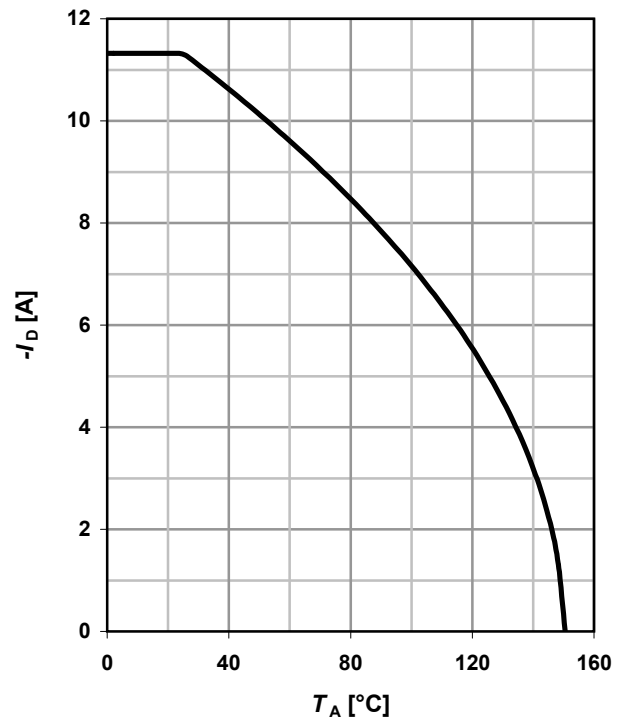
1 Power dissipation

$$P_{\text{tot}} = f(T_A); t_p \leq 10 \text{ s}$$



2 Drain current

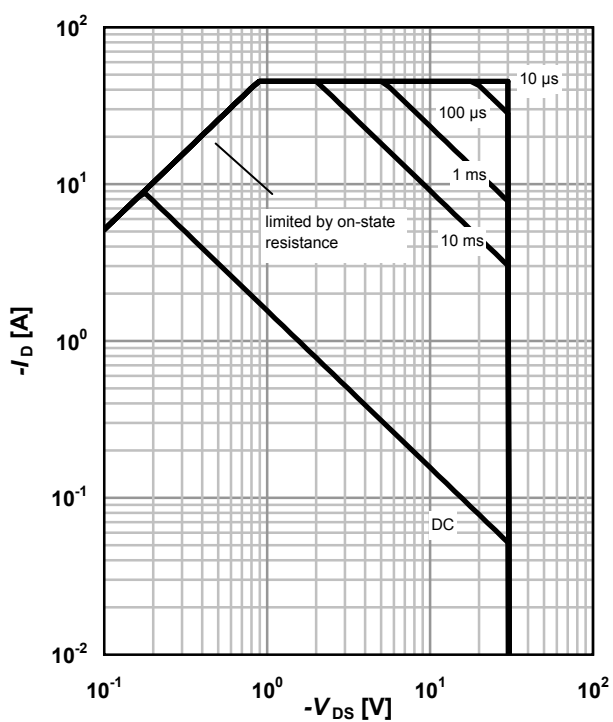
$$I_D = f(T_A); |V_{GS}| \geq 10 \text{ V}; t_p \leq 10 \text{ s}$$



3 Safe operation area

$$I_D = f(V_{DS}); T_A = 25 \text{ °C}^{(1)}; D = 0$$

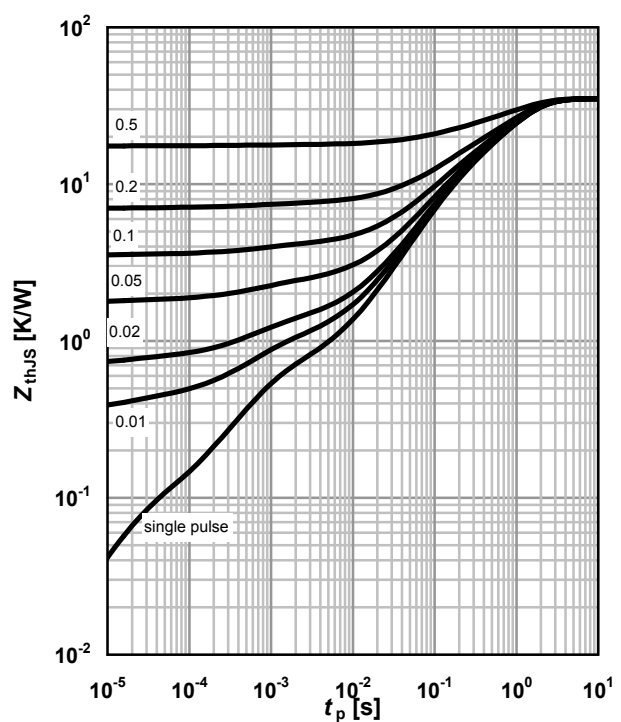
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJS}} = f(t_p)$$

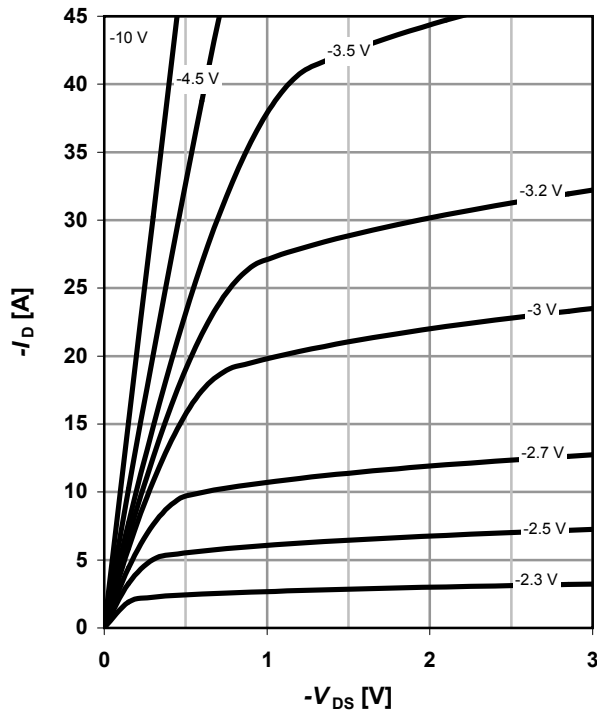
parameter: $D = t_p / T$



5 Typ. output characteristics

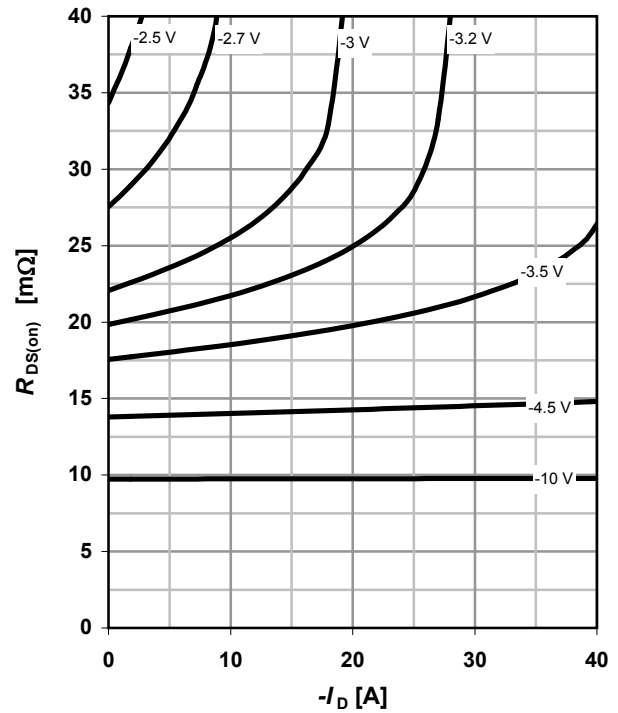
$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

parameter: V_{GS}


6 Typ. drain-source on resistance

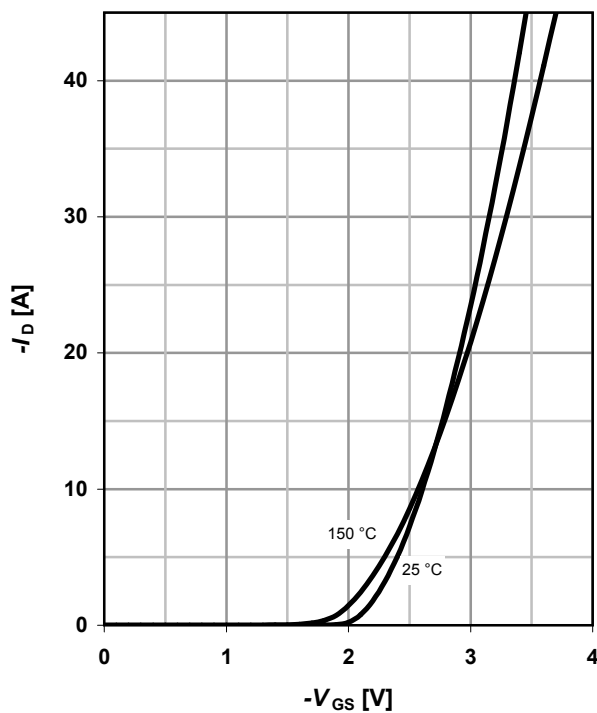
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

parameter: V_{GS}

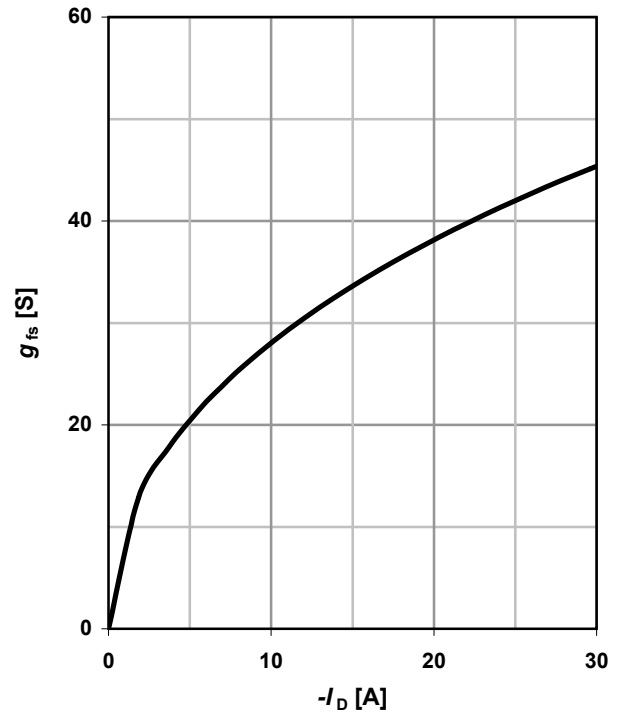

7 Typ. transfer characteristics

$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

parameter: T_j

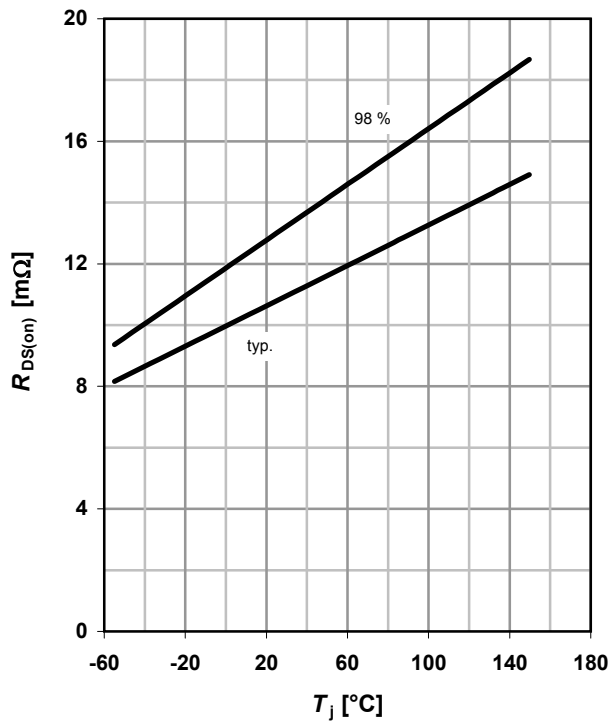

8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$

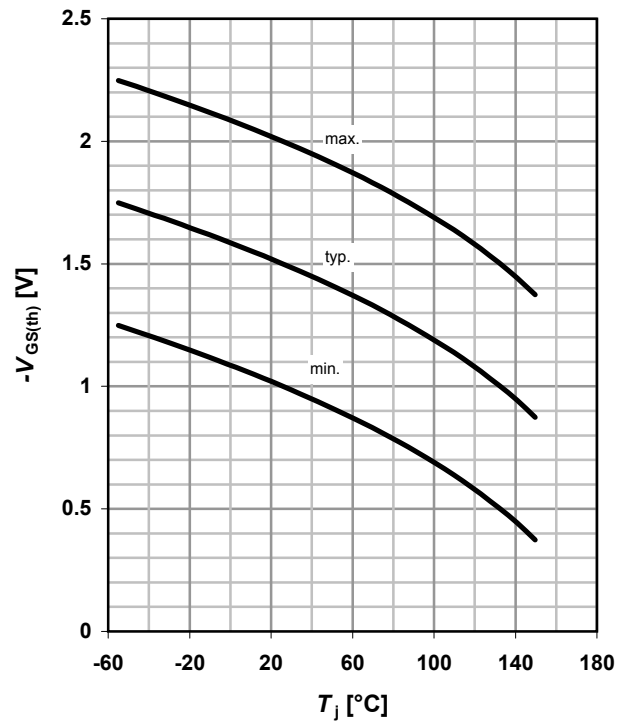


9 Drain-source on-state resistance

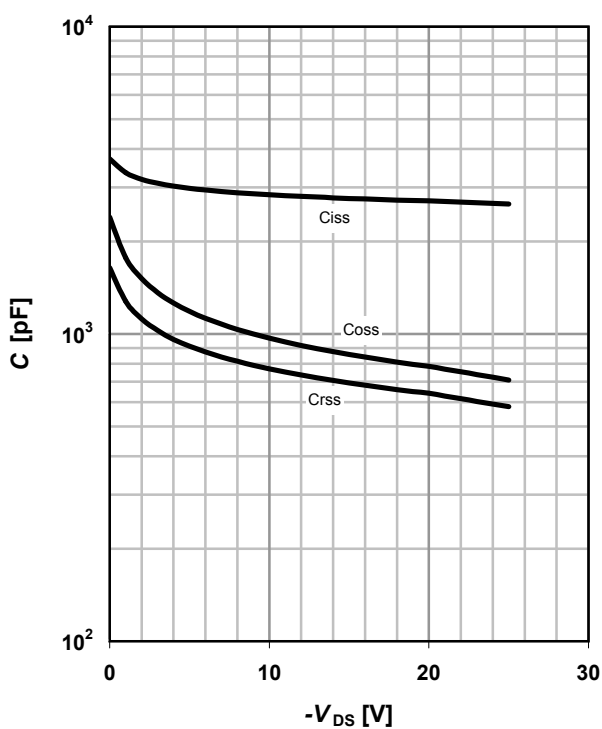
$$R_{DS(on)} = f(T_j); I_D = -11.3 \text{ A}; V_{GS} = -10 \text{ V}$$


10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = -140 \mu\text{A}$$

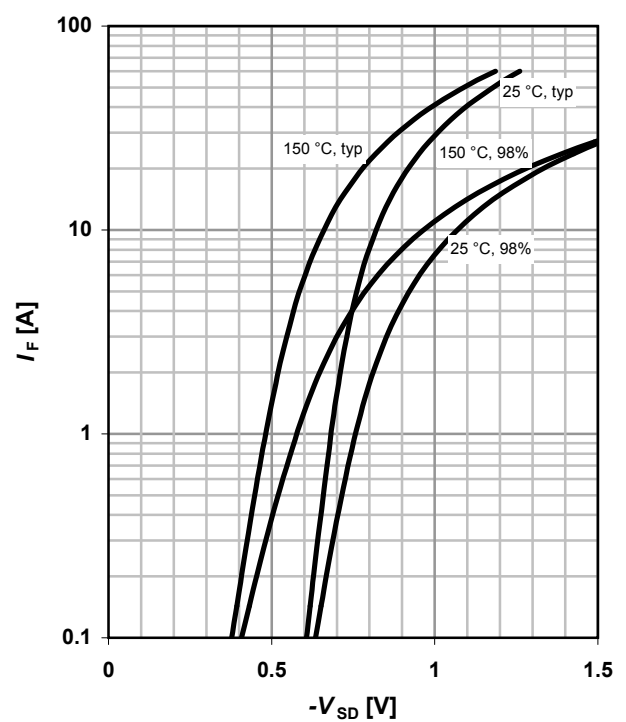

11 Typ. capacitances

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$


12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

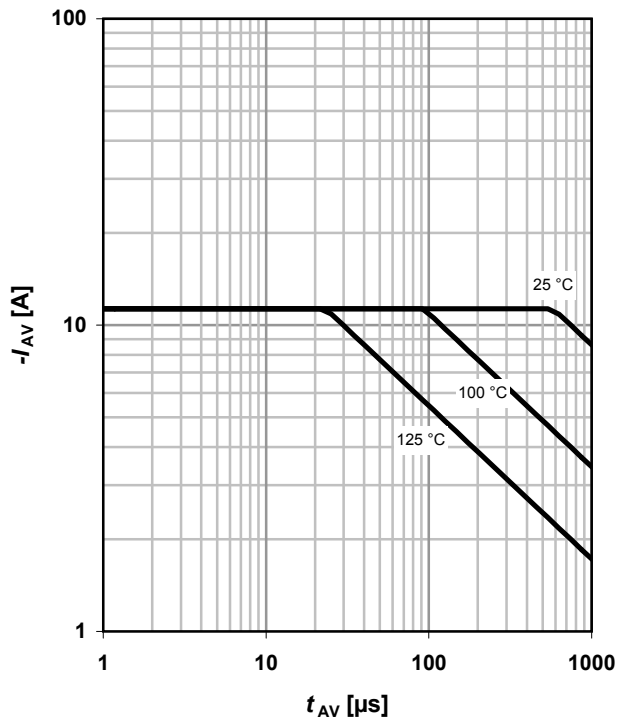
parameter: T_j



13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

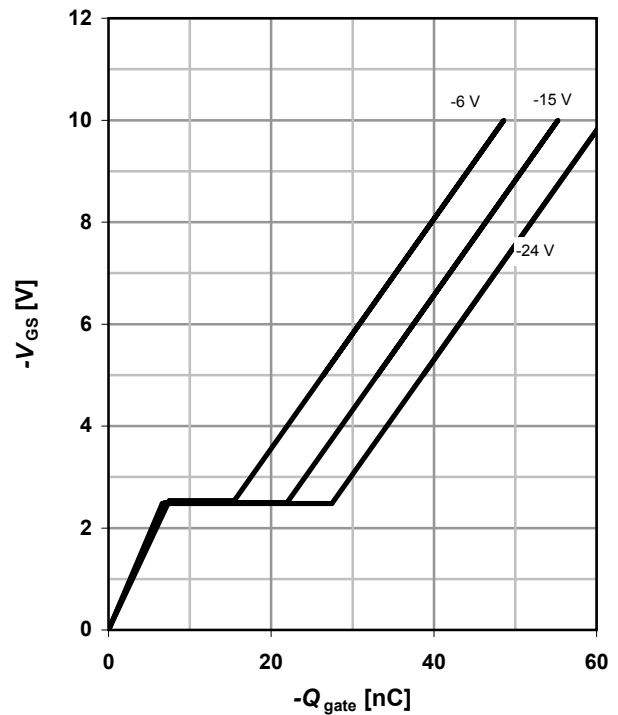
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

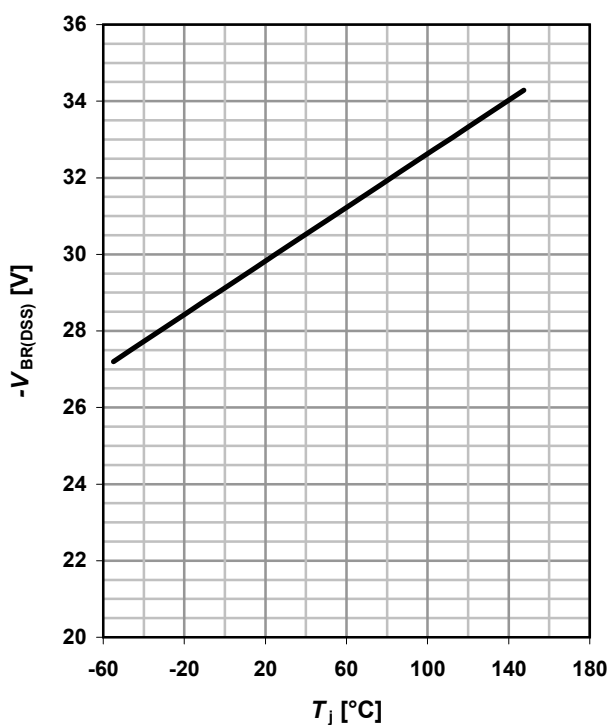
$$V_{GS}=f(Q_{\text{gate}}); I_D=-5.5\ \text{A pulsed}$$

parameter: V_{DD}

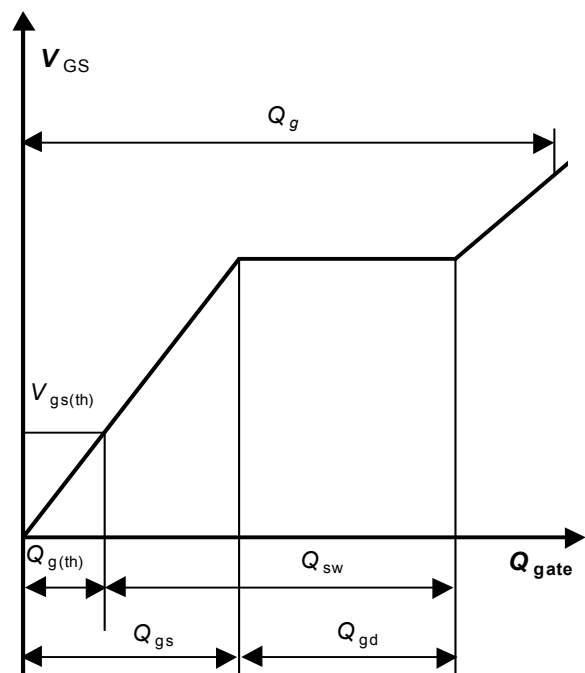


15 Drain-source breakdown voltage

$$V_{BR(DSS)}=f(T_j); I_D=-250\ \mu\text{A}$$

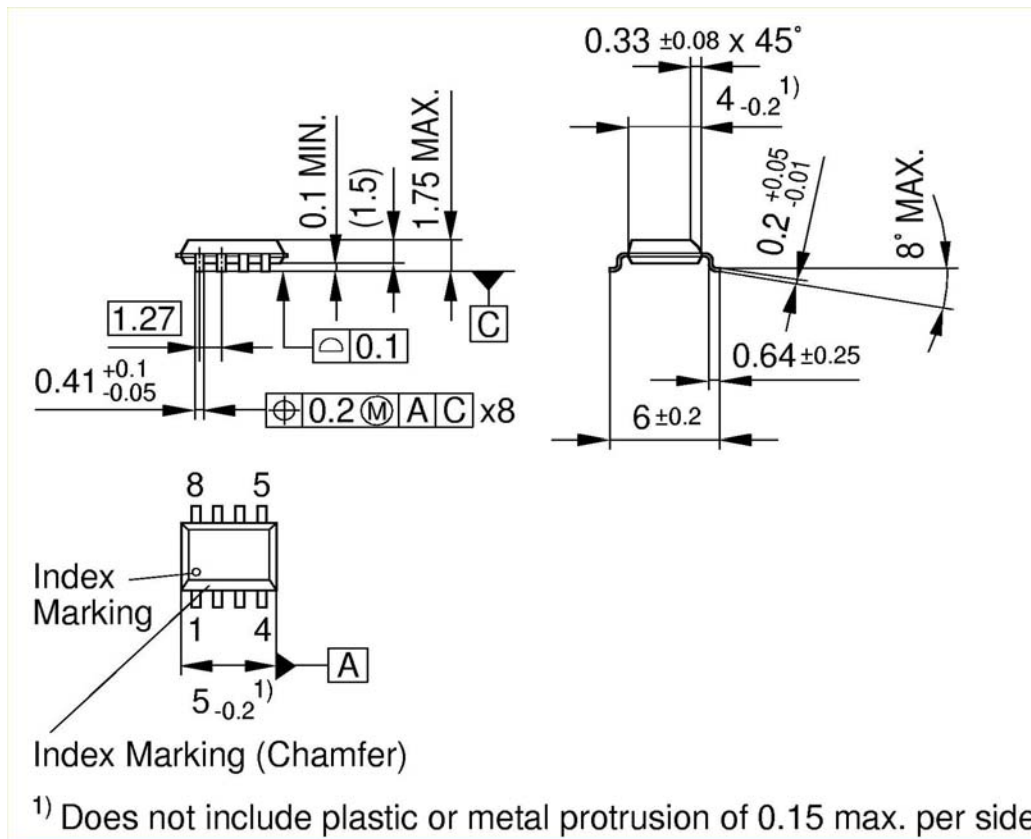


16 Gate charge waveforms

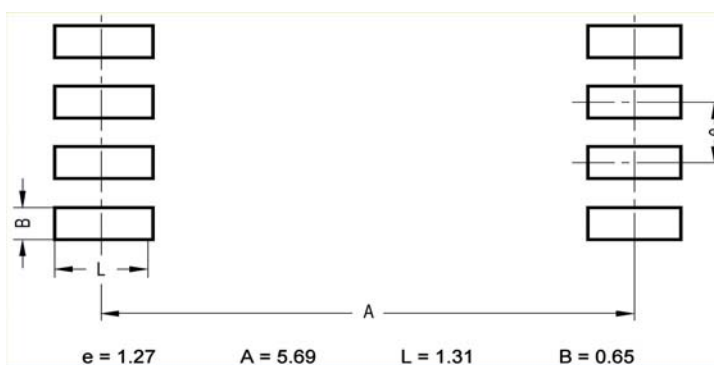


Package Outline

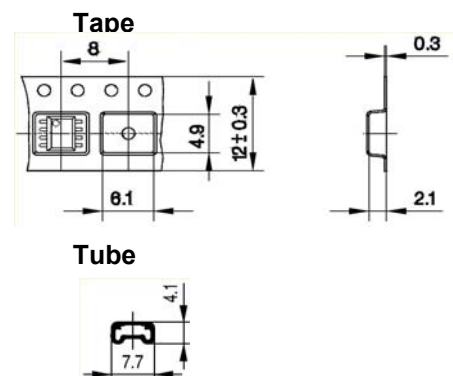
P-DSO-8: Outline



Footprint



Packaging



Dimensions in mm

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