



74VHCT16240A

16-BIT BUS BUFFER WITH 3-STATE OUTPUTS (INVERTED)

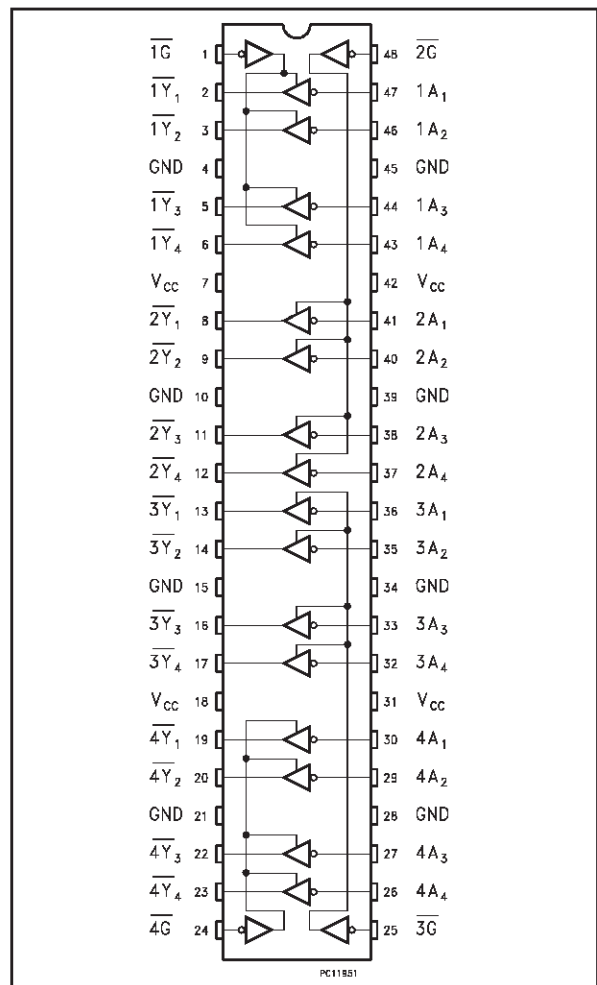
- HIGH SPEED: $t_{PD} = 5.6 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS:
 $V_{IH} = 2V$ (MIN.), $V_{IL} = 0.8V$ (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR}) = 4.5V \text{ to } 5.5V$
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.9V$ (MAX.)



ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74VHCT16240ATTR

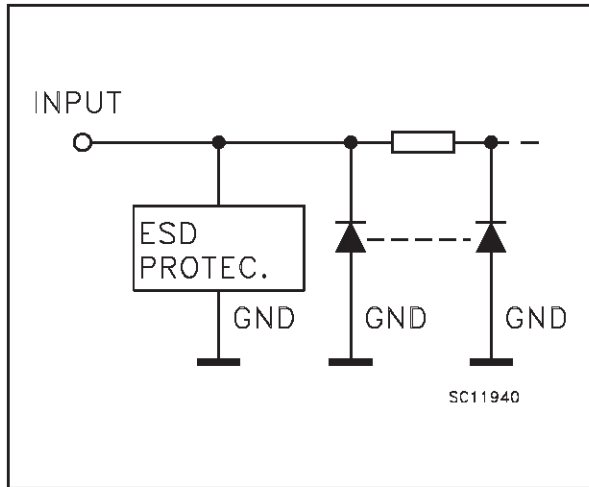
PIN CONNECTION



DESCRIPTION

The 74VHCT16240A is an advanced high-speed CMOS 16-BIT BUS BUFFER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. Any \overline{nG} output control governs four BUS BUFFERS. Output Enable inputs (\overline{nG}) tied together give full 16 bit operation. When \overline{nG} is LOW, the outputs are on. When \overline{nG} is HIGH, the output are in high impedance state. This device is designed to be used with 3 state memory address drivers, etc. Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V since all inputs are equipped with TTL threshold. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

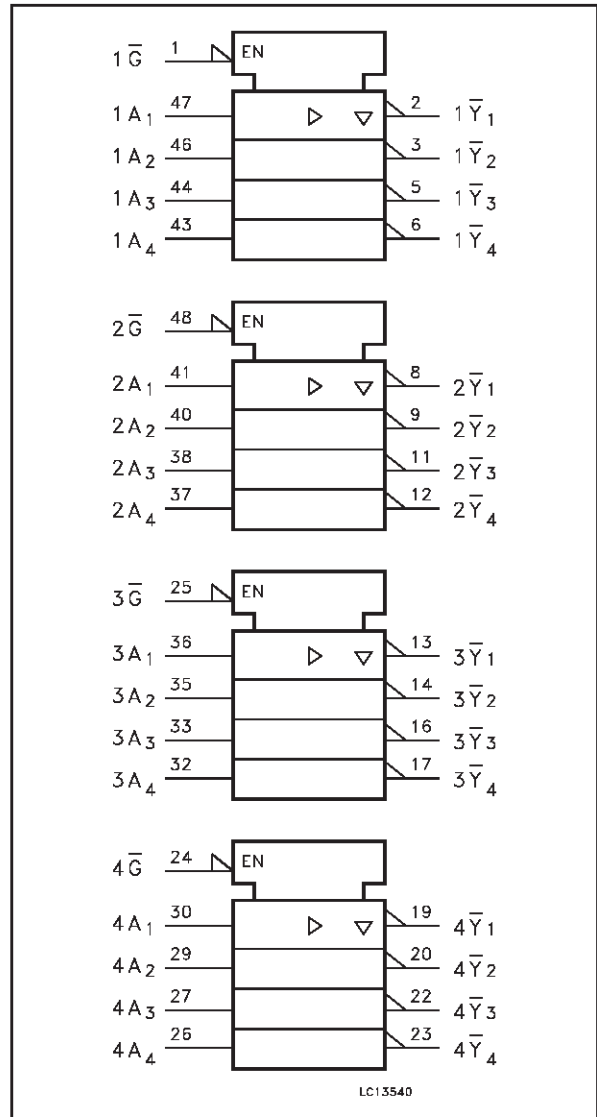
PIN No	SYMBOL	NAME AND FUNCTION
1	1G	Output Enable Input
2, 3, 5, 6	1Y1 to 1Y4	Data Outputs
8, 9, 11, 12	2Y1 to 2Y4	Data Outputs
13, 14, 16, 17	3Y1 to 3Y4	Data Outputs
19, 20, 22, 23	4Y1 to 4Y4	Data Outputs
24	4G	Output Enable Input
25	3G	Output Enable Input
30, 29, 27, 26	4A1 to 4A4	Data Input
36, 35, 33, 32	3A1 to 3A4	Data Input
41, 40, 38, 37	2A1 to 2A4	Data Input
47, 46, 44, 43	1A1 to 1A4	Data Input
48	2G	Output Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS		OUTPUT
G	A _n	Y _n
L	L	H
L	H	L
H	X	Z

X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 1)	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 2)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

- 1) Output in OFF State
2) High or Low State

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (see note 1)	0 to 5.5	V
V_O	Output Voltage (see note 2)	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (see note 3) ($V_{CC} = 5.0 \pm 0.5V$)	0 to 20	ns/V

- 1) Output in OFF State
2) High or Low State
3) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V _{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V _{OH}	High Level Output Voltage	4.5	I _O =-50 μA	4.4	4.5		4.4		4.4		V
		4.5	I _O =-8 mA	3.94			3.8		3.7		
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =8 mA			0.36		0.44		0.55	
I _{oz}	High Impedance Output Leakage Current	4.5 to 5.5	V _I = V _{IH} or V _{IL} V _O = 0V to 5.5V			±0.25		± 2.5		± 2.5	μA
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1.0		± 1.0	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			2		20		20	μA
I _{CC}	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V _{CC} or GND			1.35		1.5		1.5	mA
I _{OPD}	Output Leakage Current	0	V _{OUT} = 5.5V			0.5		5.0		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value						Unit		
		V _{CC} ^(*) (V)	C _L (pF)		T _A = 25°C			-40 to 85°C			-55 to 125°C	
					Min.	Typ.	Max.	Min.	Max.		Min.	Max.
t _{PLH} t _{PHL}	Propagation Delay Time	5.0	15		5.4	8.5	1.0	9.5	1.0	10.0	ns	
		5.0	50		7.0	9.5	1.0	10.5	1.0	11.0		
t _{PZL} t _{PZH}	Output Disable Time	5.0	15	RL = 1KΩ	7.7	10.4	1.0	12.0	1.0	12.0	ns	
		5.0	50		8.2	11.4	1.0	13.0	1.0	13.0		
t _{PZL} t _{PZH}	Output Enable Time	5.0	50	RL = 1KΩ	8.8	11.4	1.0	13.0	1.0	13.0	ns	

(*) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
				T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance			5	10			10		10	pF
C _{OUT}	Output Capacitance			9							pF
C _{PD}	Power Dissipation Capacitance (note 1)			21							pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per Circuit)

DYNAMIC SWITCHING CHARACTERISTICS

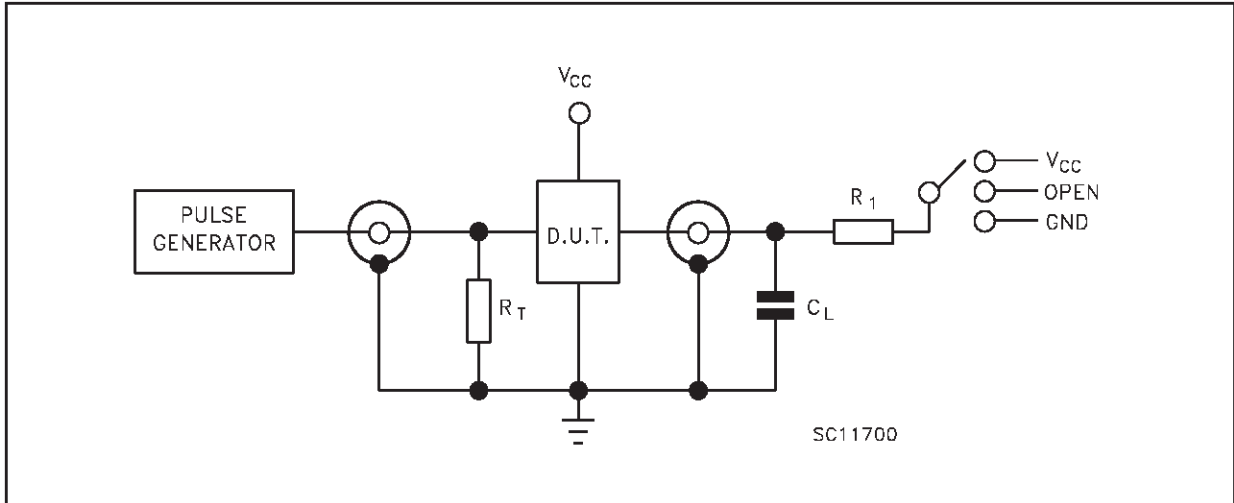
Symbol	Parameter	Test Condition		Value						Unit		
				V _{CC} (V)	T _A = 25°C			-40 to 85°C			-55 to 125°C	
					Min.	Typ.	Max.	Min.	Max.		Min.	Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C _L = 50 pF		0.9	1.1					V	
V _{OLV}				1.1	-0.9							
V _{IHD}	5.0	2.0										
V _{ILD}	5.0				0.8							

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.0V. Inputs under test switching: 3.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

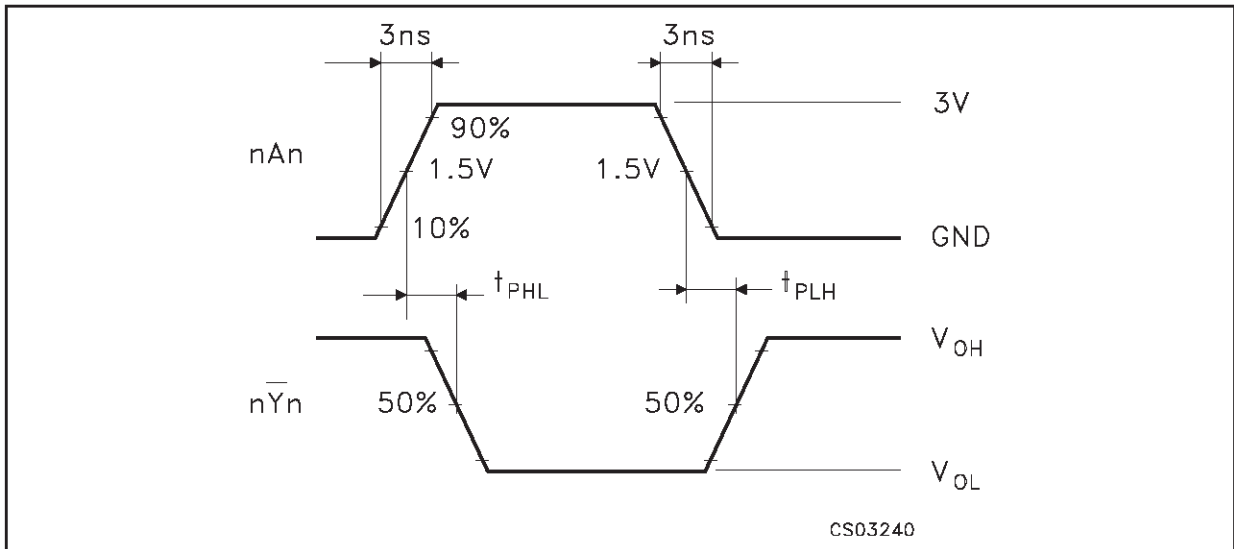
TEST CIRCUIT



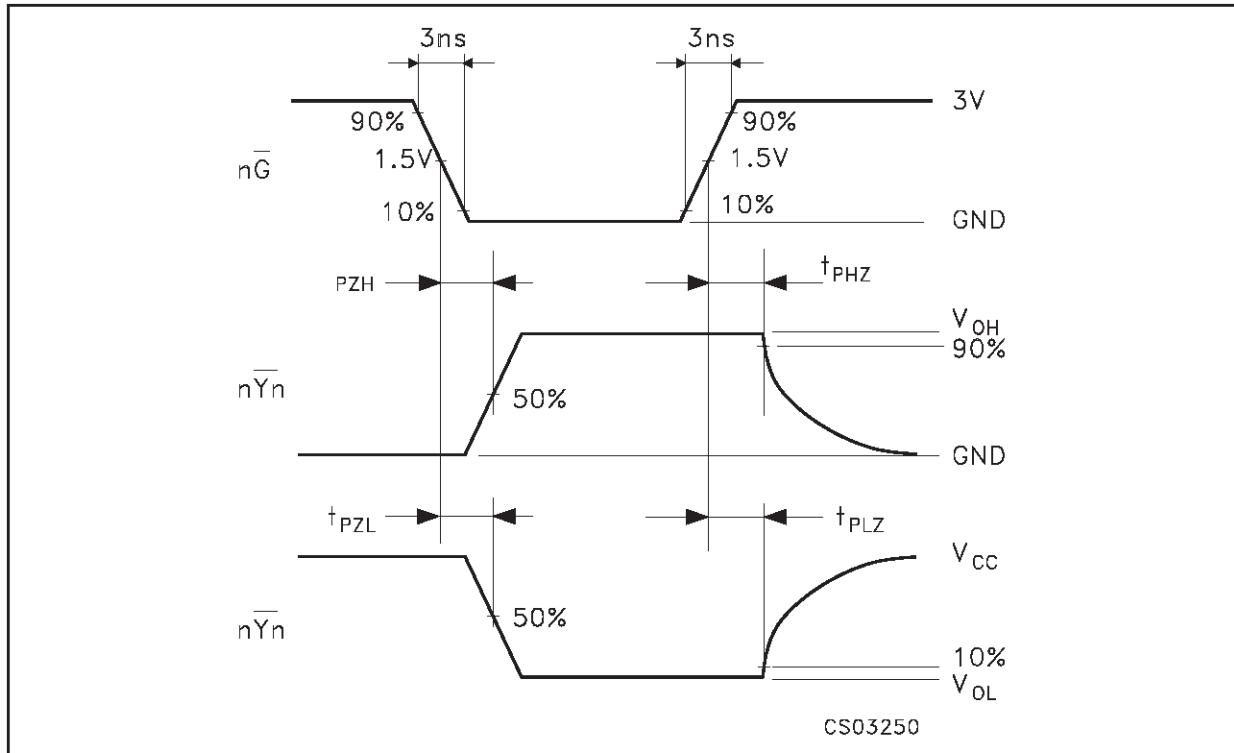
TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_{CC}
t_{PZH} , t_{PHZ}	GND

$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = R_1 = 1\text{K}\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)

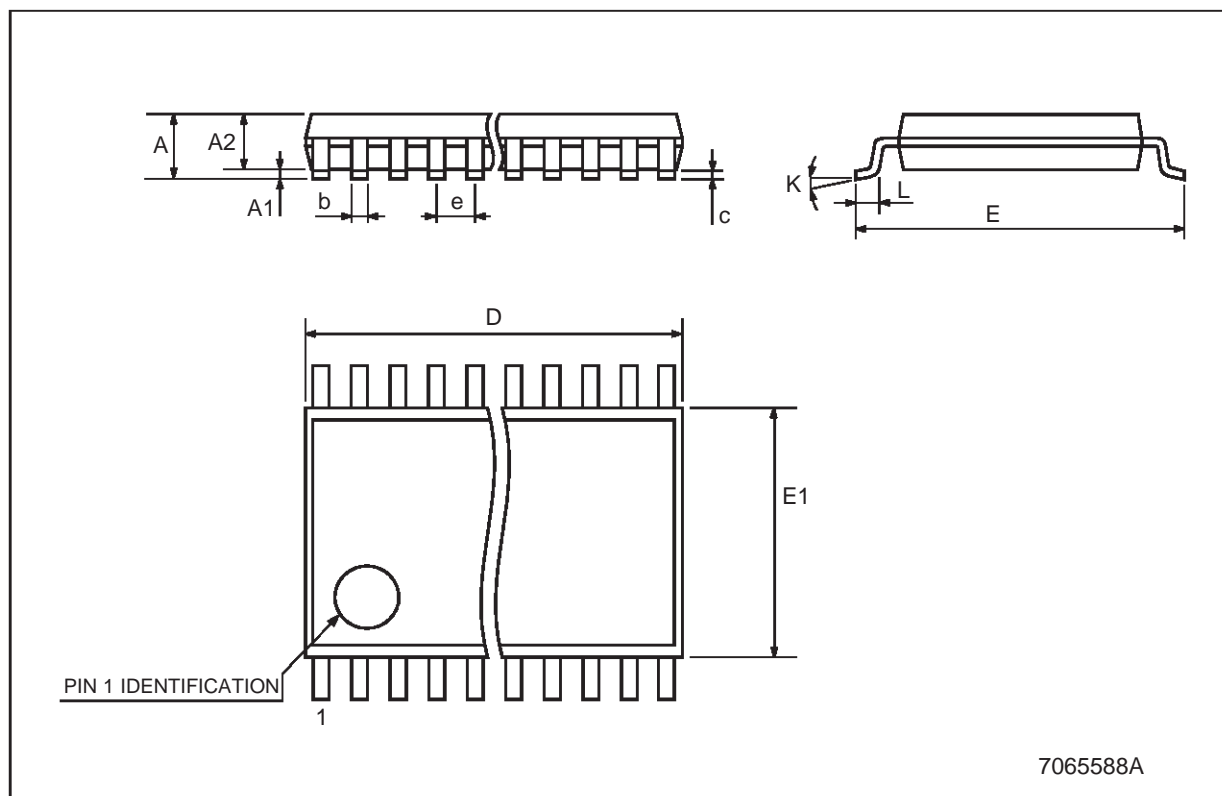


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.408		0.496
E	7.95		8.25	0.313		0.325
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



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