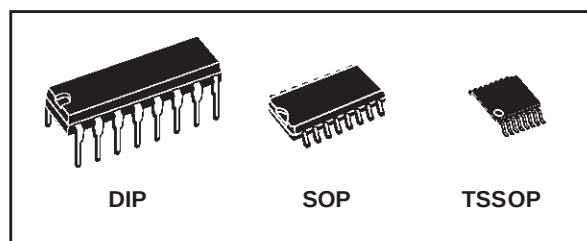


QUAD D-TYPE REGISTER (3 STATE)

- HIGH SPEED:
 $f_{MAX} = 84\text{MHz}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 6\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH
74 SERIES 173



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC173B1R	
SOP	M74HC173M1R	M74HC173RM13TR
TSSOP		M74HC173TTR

DESCRIPTION

The M74HC173 is an high speed CMOS QUAD D-TYPE REGISTER (3-STATE) fabricated with silicon gate C²MOS technology.

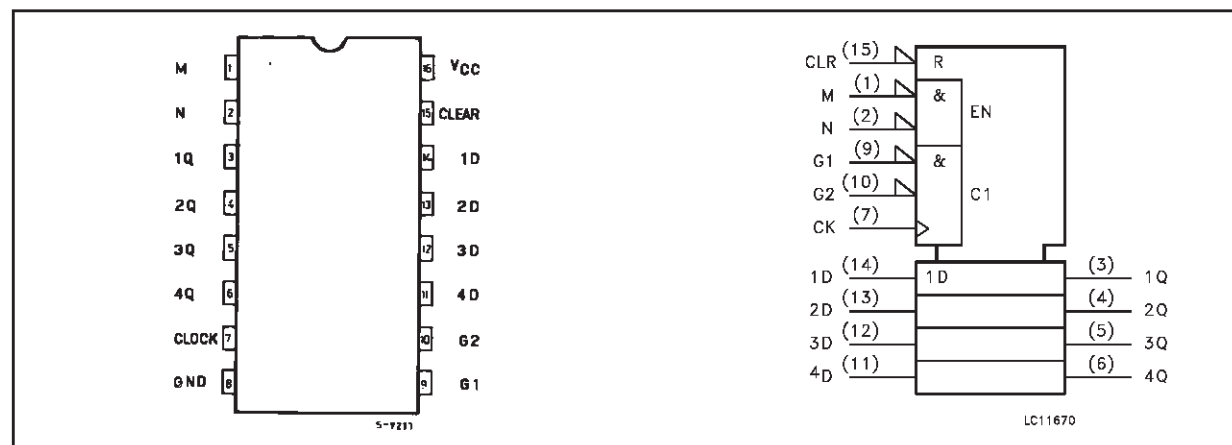
This device is composed of a four-bit register including D-TYPE flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common reset input (CLEAR). Signals applied to the data inputs (D₁ - D₄) are stored at the respective flip-flops on the positive going transition of the clock input, only

when both clock control inputs (G1 and G2) are held low.

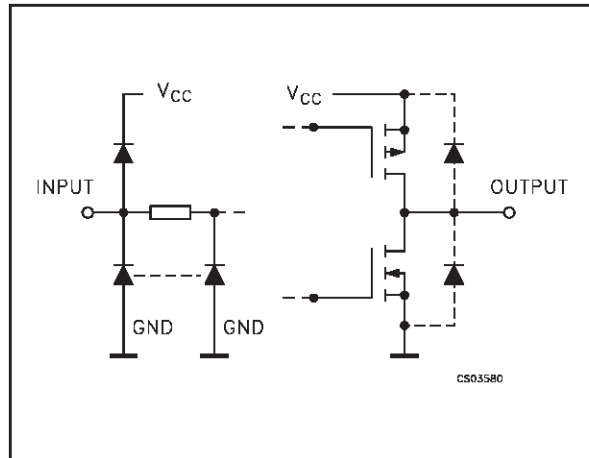
The reset feature is asynchronous and active high. The stored data are provided on each output only when both output control inputs (M and N) are held low, otherwise the outputs go to the high-impedance state.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

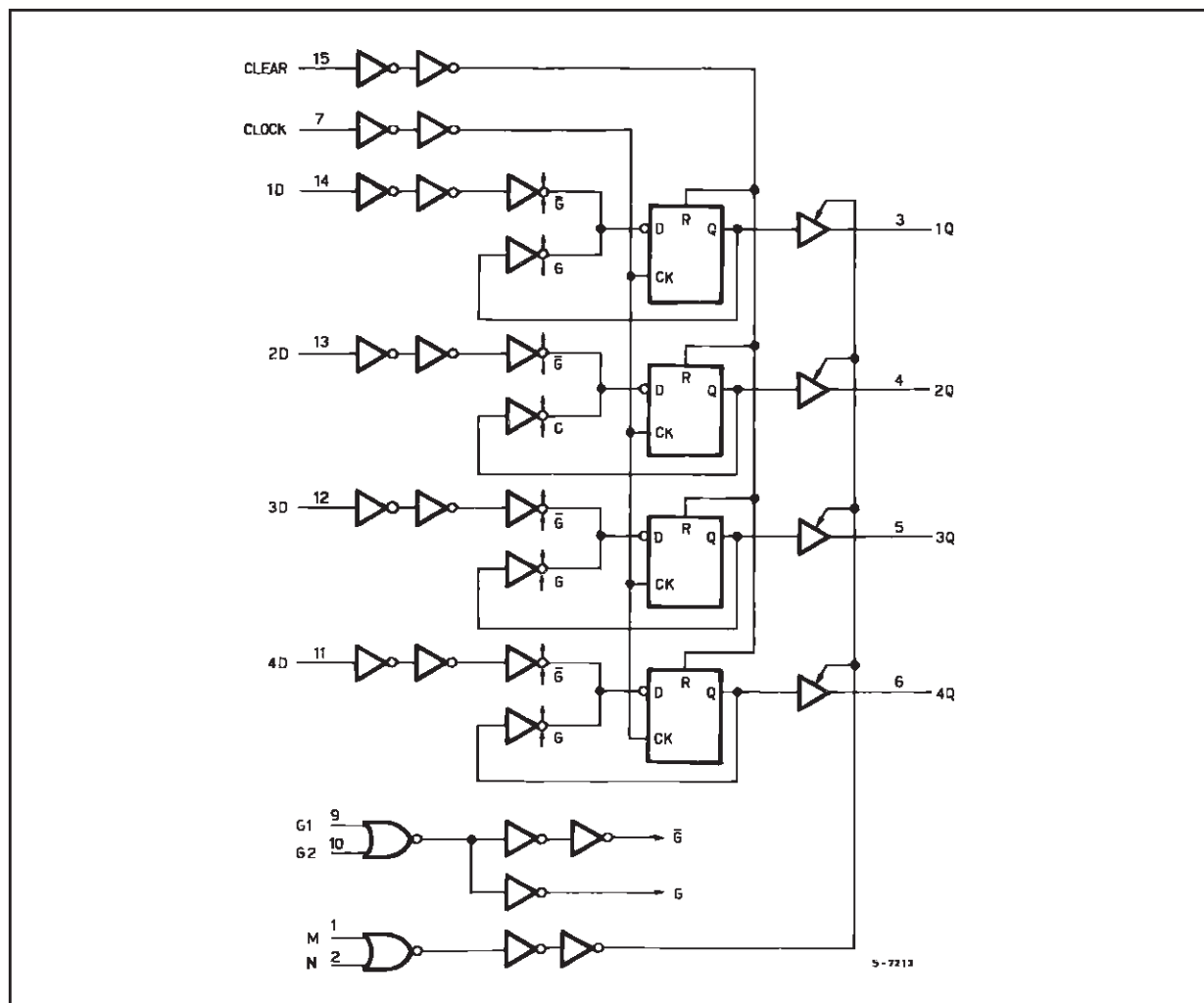
PIN No	SYMBOL	NAME AND FUNCTION
1, 2	M, N	Output Enable Input (Active Low)
3, 4, 5, 6	1Q to 4Q	3-State Flip-Flop Outputs
7	CLOCK	Clock Input (Low to HIGH, Edge-triggered)
9, 10	G1, G2	Data Enable Inputs (Active Low)
14, 13, 12, 11	1D to 4D	Data Inputs
15	CLEAR	Asynchronous Master Reset (Active High)
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

CLEAR	CLOCK	DATA ENABLE		D _n	OUTPUT CONTROL		Q _n
		G1	G2		M	N	
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L		X	X	X	L	L	Q0
L		H	X	X	L	L	Q0
L		X	H	X	L	L	Q0
L		L	L	H	L	L	H
L		L	L	L	L	L	L

X : Don't Care
Z : High Impedance

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V	
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4			
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9			
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10			
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60			
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V	
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1		
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1		
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40		
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40		
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA	
I _{OZ}	High Impedance Output Leakage Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			± 0.5		± 5.0		± 10	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

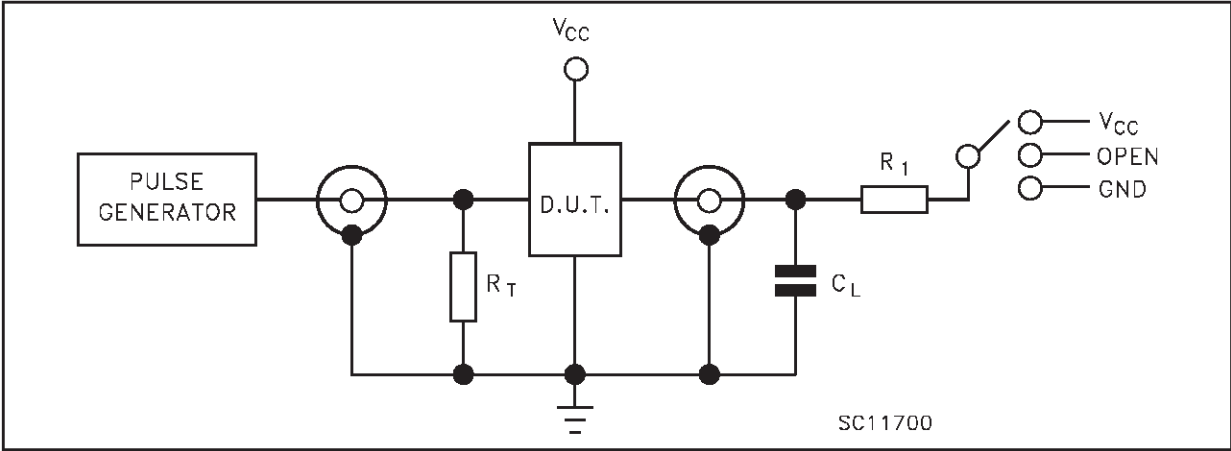
Symbol	Parameter	Test Condition			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK - Q)	2.0	50			50	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
		2.0	150			65	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
t _{PLH} t _{PHL}	Propagation Delay Time (CLEAR - Q)	2.0	50			50	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
		2.0	150			65	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
f _{MAX}	Maximum Clock Frequency	2.0	50		8.6	20		6.8		5.8		MHz
		4.5			43	67		34		29		
		6.0			51	84		40		34		
t _{PZL} t _{PZH}	Output Enable Time	2.0	50	R _L = 1 KΩ		50	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
		2.0	150	R _L = 1 KΩ		65	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
t _{PLZ} t _{PHZ}	Output Disable Time	2.0	50	R _L = 1 KΩ		36	105		130		160	ns
		4.5				15	21		26		32	
		6.0				13	18		22		27	
t _{W(H)} t _{W(L)}	Minimum Pulse Width (CLOCK)	2.0	50			16	75		95		110	ns
		4.5				4	15		19		22	
		6.0				3	13		16		19	
t _{W(L)}	Minimum Pulse Width (CLEAR)	2.0	50			16	75		95		110	ns
		4.5				4	15		19		22	
		6.0				3	13		16		19	
t _S	Minimum Set-up Time (G1, G2)	2.0	50			40	100		125		150	ns
		4.5				10	20		25		30	
		6.0				9	17		21		26	
t _S	Minimum Set-up Time (D)	2.0	50			24	75		95		110	ns
		4.5				6	15		19		22	
		6.0				5	13		16		19	
t _H	Minimum Hold Time (G1 ,G2, D)	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t _{REM}	Minimum Removal Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	5.0			5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0			50						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (Per Circuit)

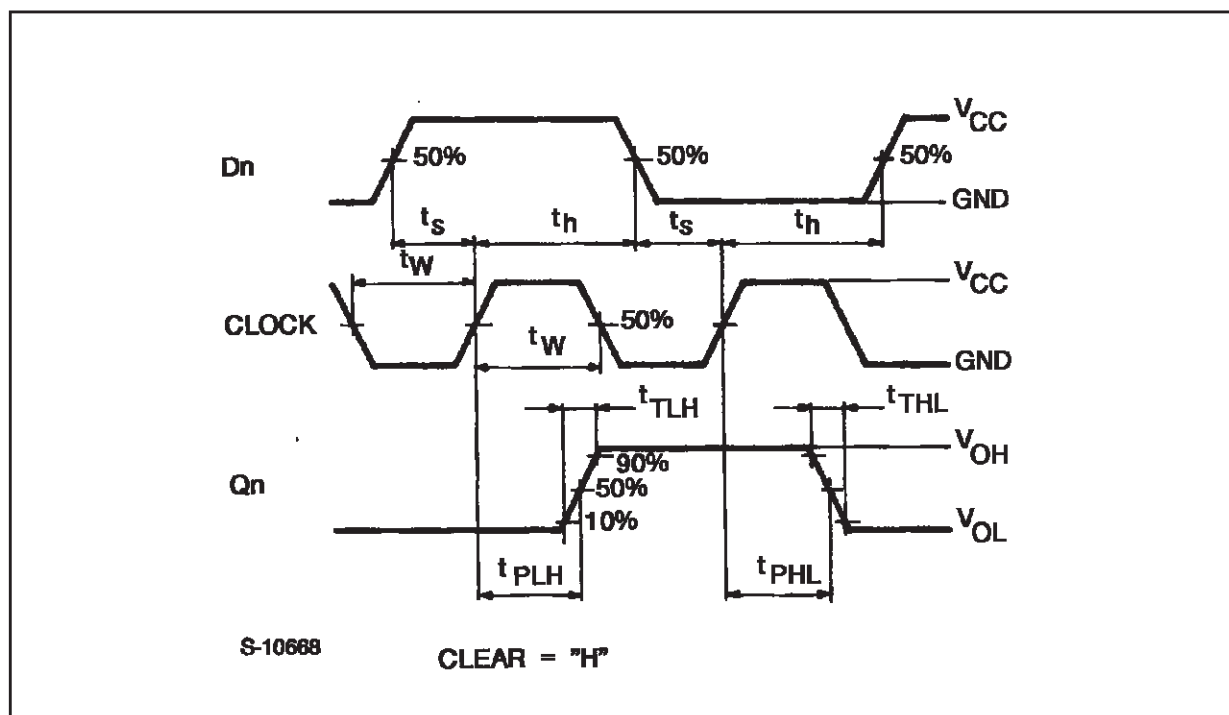
TEST CIRCUIT



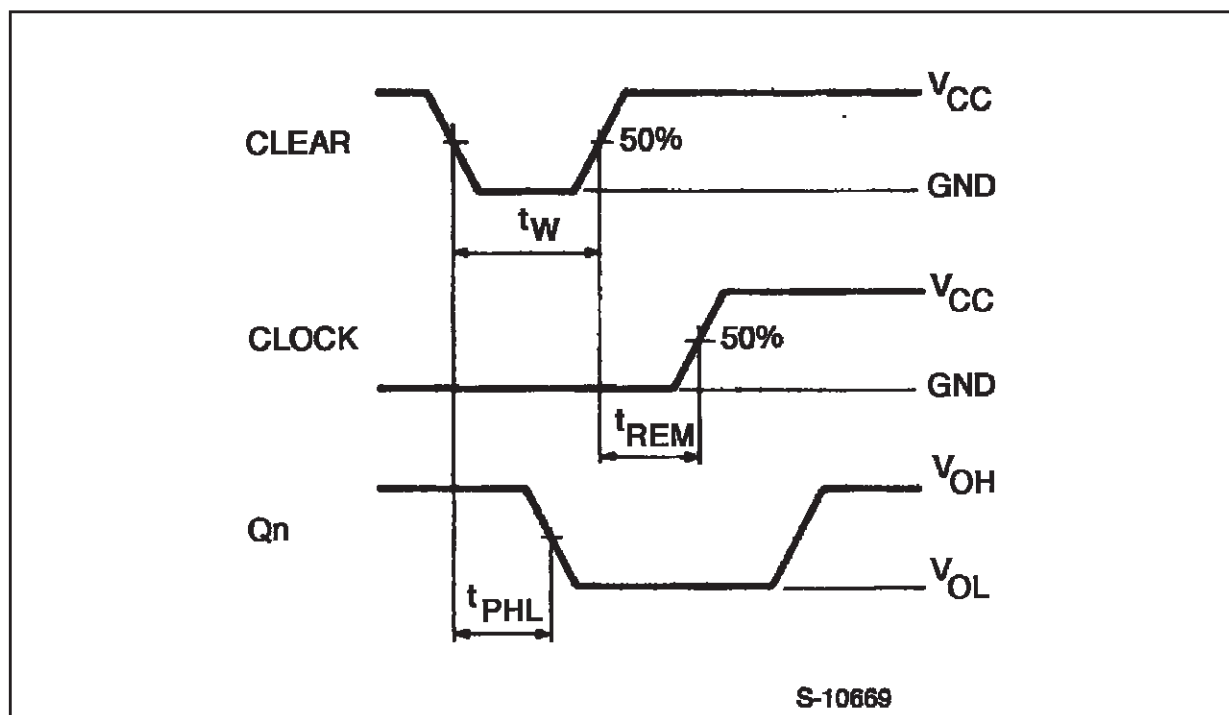
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	V _{CC}
t _{PZH} , t _{PHZ}	GND

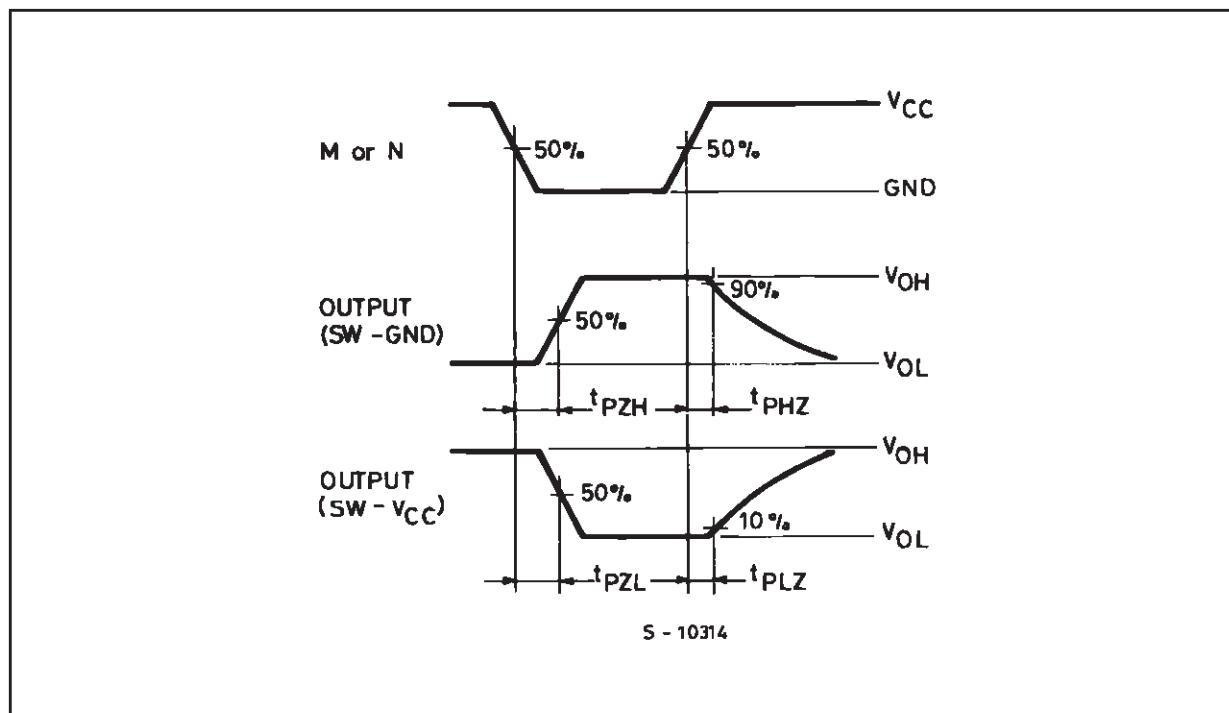
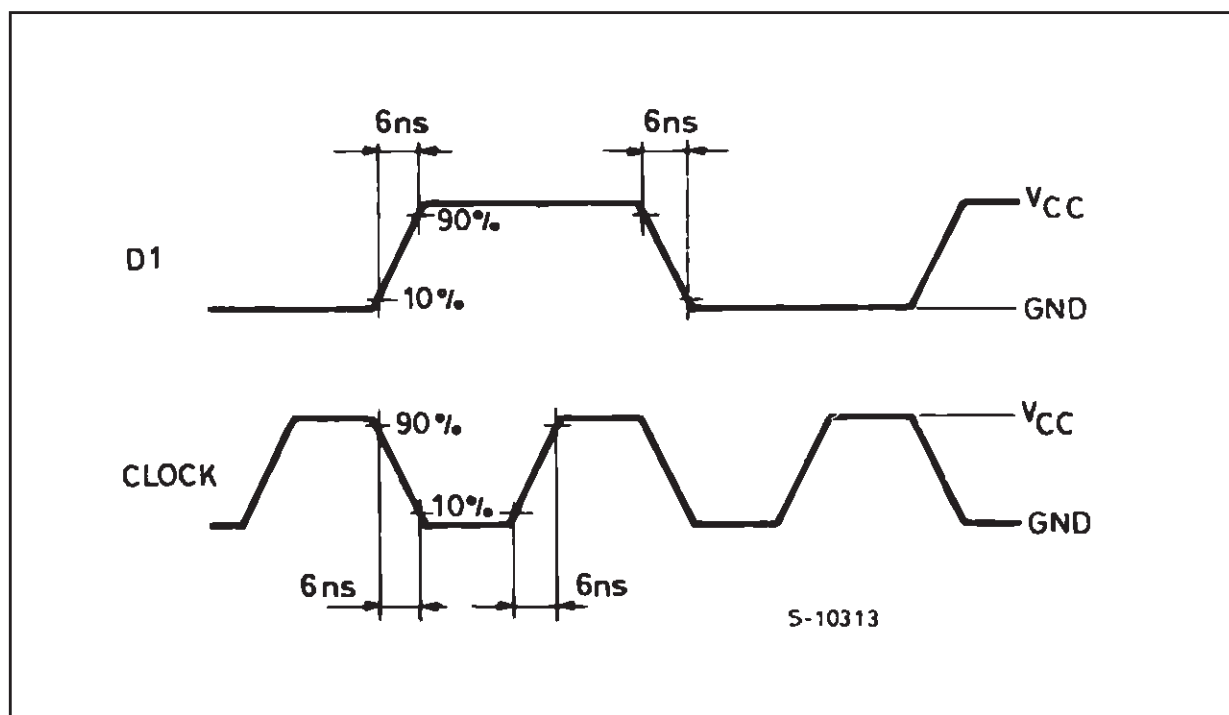
C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
R₁ = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAY TIMES, MINIMUM PULSE WIDTH (CLOCK), SETUP AND HOLD TIME (Dn TO CLOCK) ($f=1\text{MHz}$; 50% duty cycle)



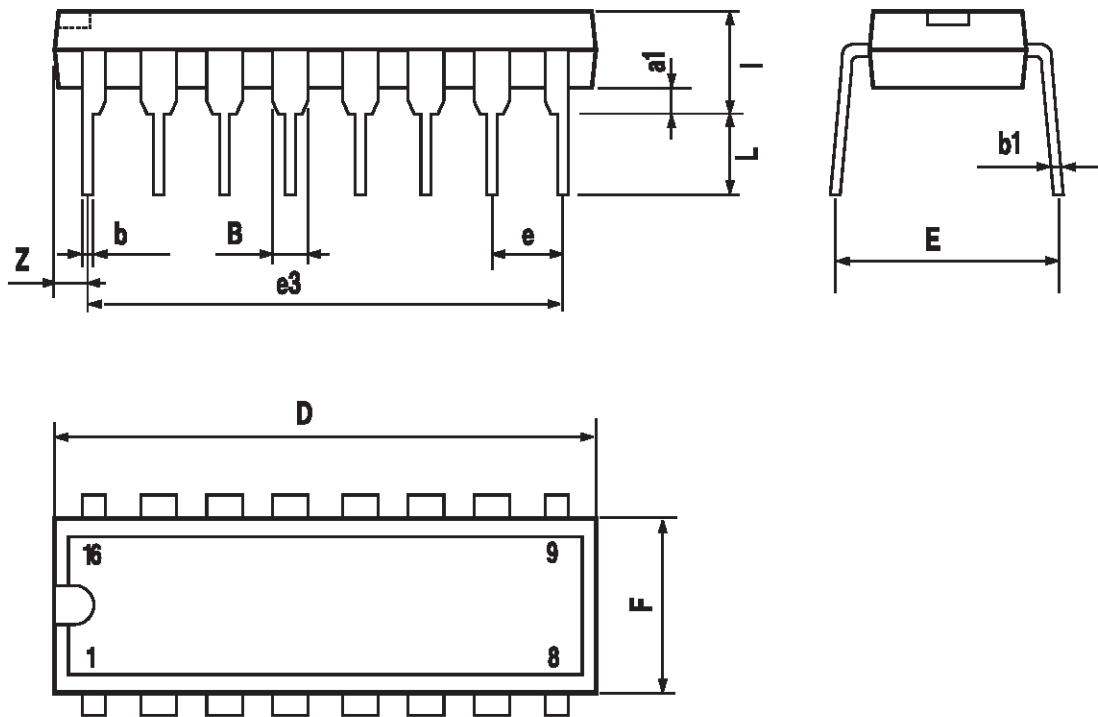
WAVEFORM 2: MINIMUM PULSE WIDTH (CLEAR) AND REMOVAL TIME (CLEAR TO CLOCK) ($f=1\text{MHz}$; 50% duty cycle)



WAVEFORM 3: OUTPUT ENABLE AND DISABLE TIME($f=1\text{MHz}$; 50% duty cycle)WAVEFORM 4: INPUT WAVEFORMS($f=1\text{MHz}$; 50% duty cycle)

Plastic DIP-16 (0.25) MECHANICAL DATA

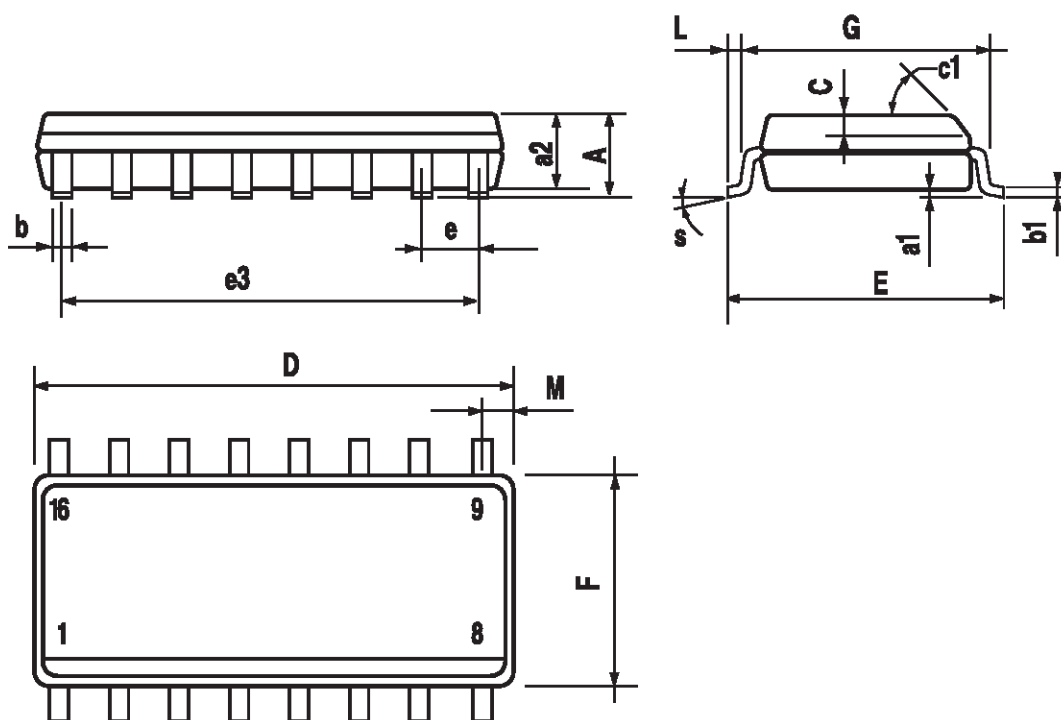
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

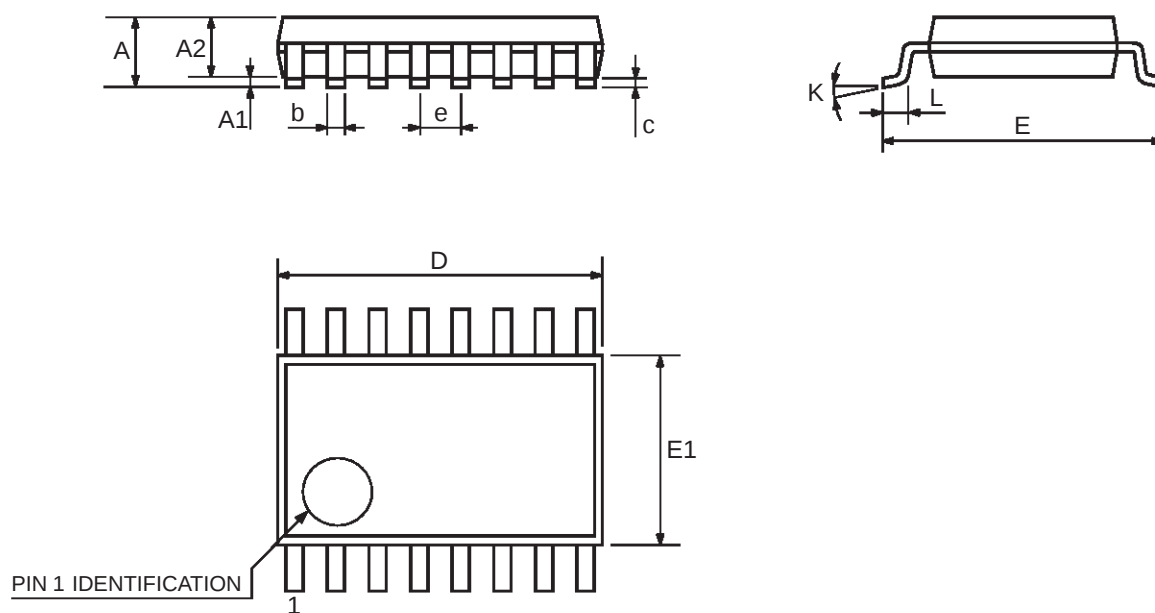
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0080338D

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>