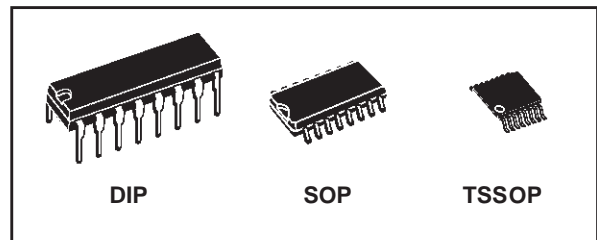




# M74HC597

## 8 BIT LATCH/SHIFT REGISTER

- HIGH SPEED :  
 $f_{MAX} = 50 \text{ MHz (TYP.) at } V_{CC} = 6V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4\text{mA (MIN)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:  
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE WITH  
 74 SERIES 597



### ORDER CODES

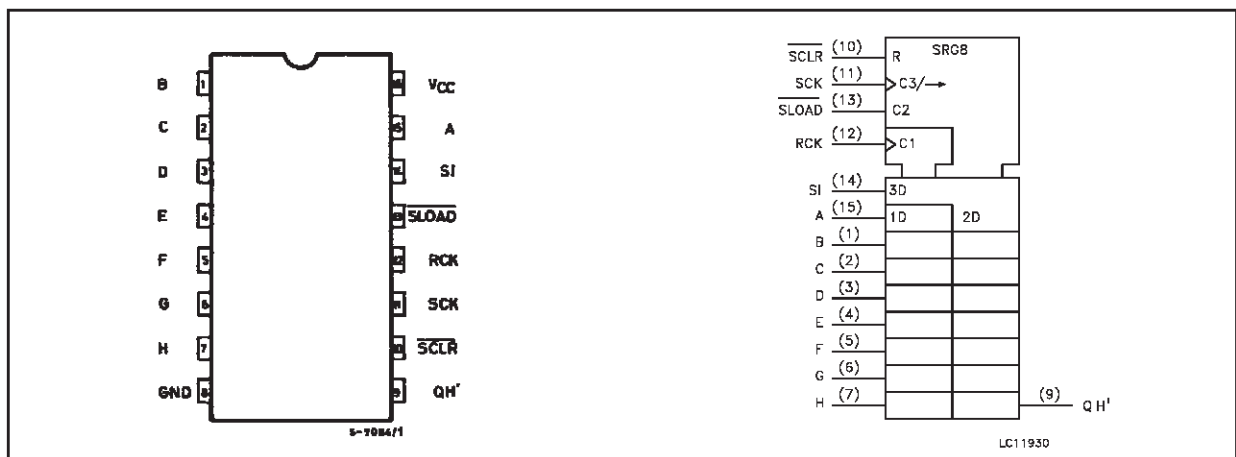
PACKAGE	TUBE	T & R
DIP	M74HC597B1R	
SOP	M74HC597M1R	M74HC597RM13TR
TSSOP		M74HC597TTR

### DESCRIPTION

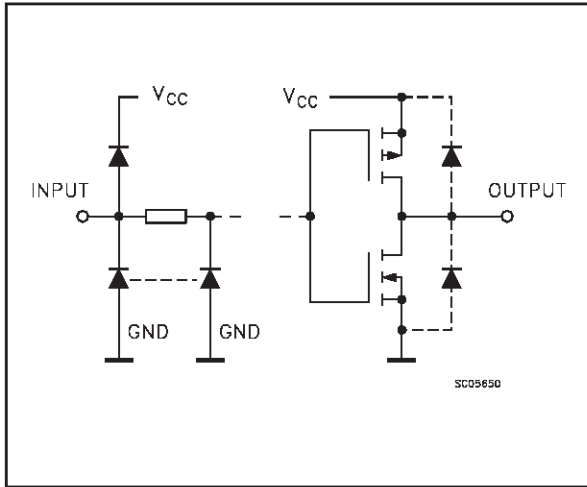
The M74HC597 is an high speed CMOS 8 BIT PIPO SHIFT REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology. This devices comes in a 16-pin package and consist of an 8-bit storage latch feeding a parallel in, serial out 8-bit shift register. Both the storage

register and shift register have positive edge triggered clocks. The shift register also has direct load (from storage) and clear inputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

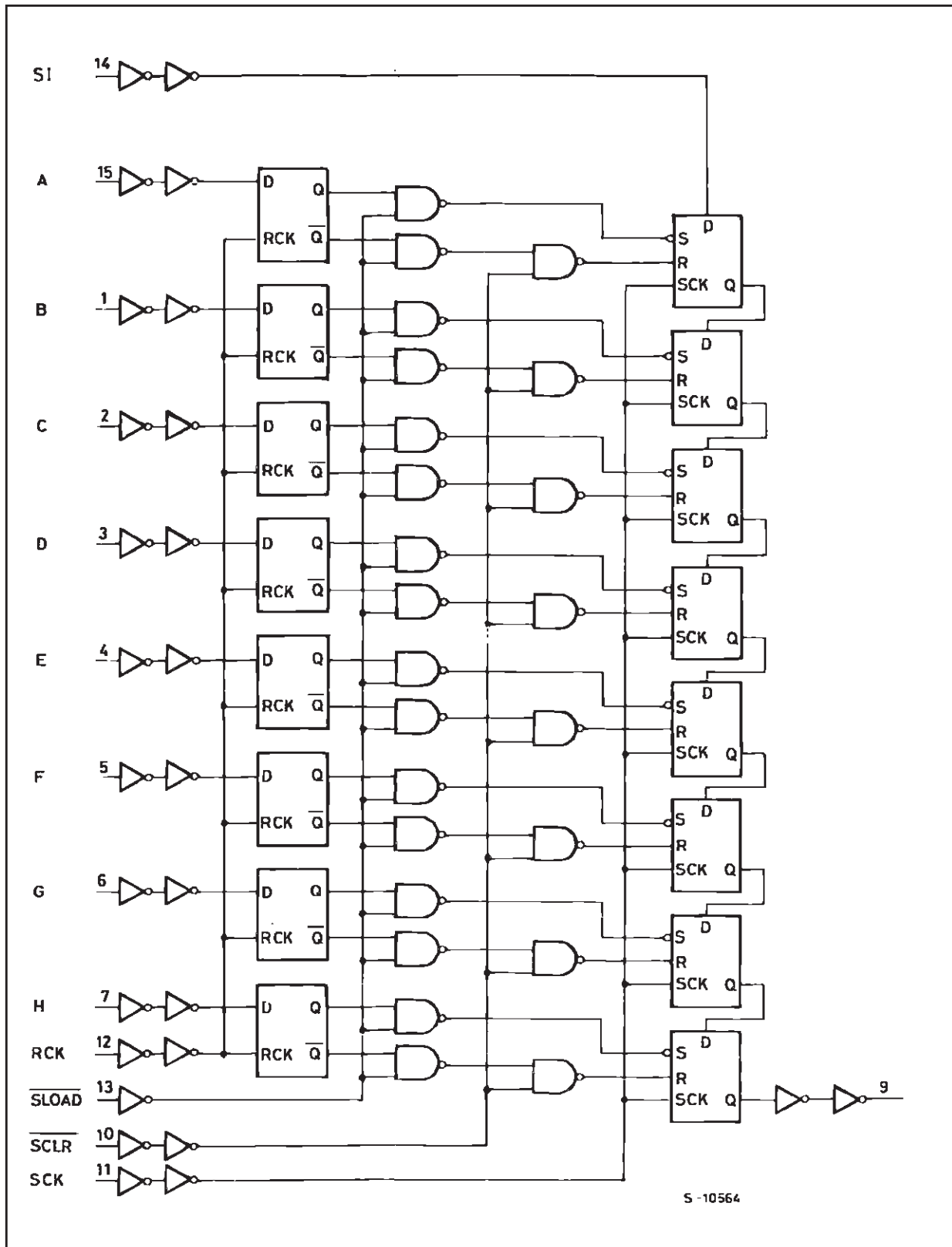
PIN No	SYMBOL	NAME AND FUNCTION
9	QH'	Serial Data Outputs
10	$\overline{\text{SCLR}}$	Asynchronous Reset Input (Active LOW)
11	SCK	Shift Clock Input (LOW to HIGH Edge-triggered)
12	RCK	Storage Clock Input (LOW to HIGH Edge-triggered)
13	$\overline{\text{SLOAD}}$	Parallel Data Input (Active Low)
10	SI	Serial Data Input
15, 1, 2, 3, 4, 5, 6, 7	A to H	Parallel Data Inputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS					OUTPUT
SI	SCK	$\overline{\text{SCLR}}$	$\overline{\text{SLOAD}}$	RCK	
X	X	L	H	X	S.R. IS CLEARED TO "L"
X	X	H	L	X	INPUT REGISTER DATA IS STORED INTO S.R.
L		H	H	X	FIRST STAGE OF S.R. BECOMES "L" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H		H	H	X	FIRST STAGE OF S.R. BECOMES "H" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X		H	H	X	STATE OF S.R. IS NOT CHANGED
X	X	X	X		INPUT DATA ON A ~ H LINE IS STORED INTO INPUT REGISTER
X	X	X	X		STORAGE REGISTER STATE IS NOT CHANGED

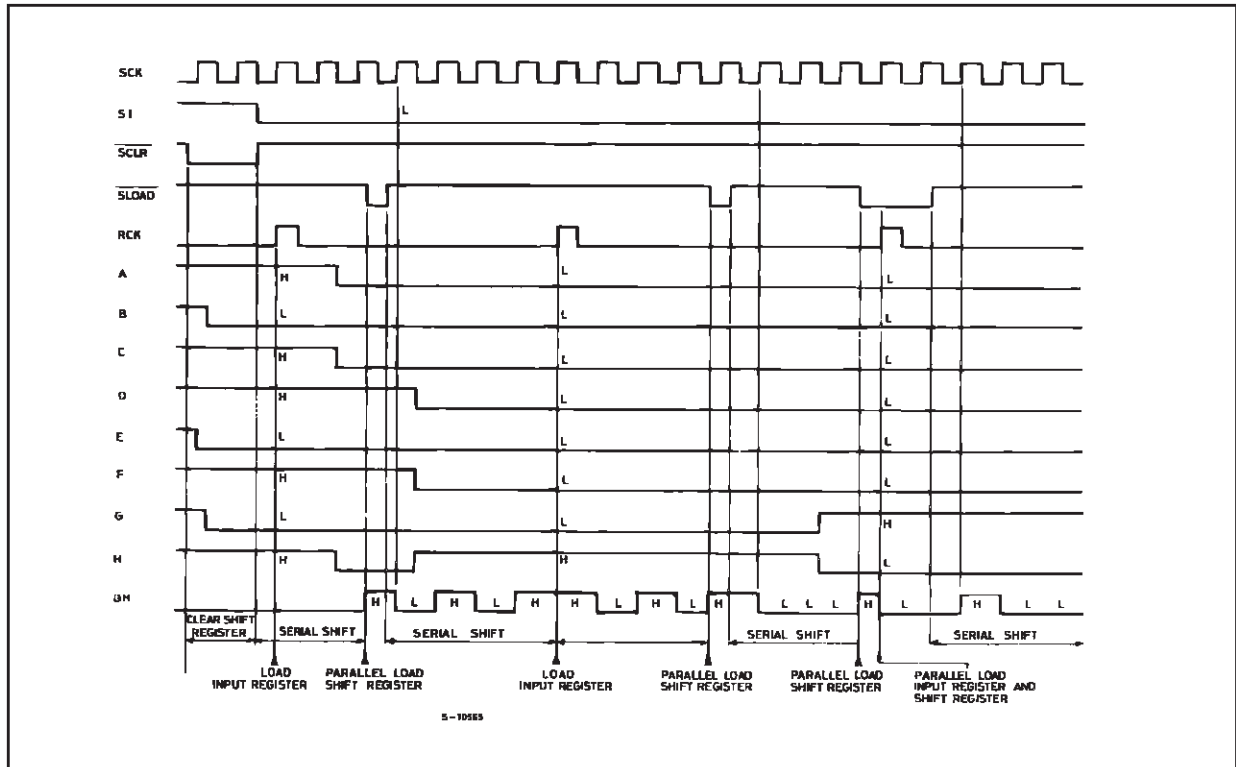
X : Don't Care

## LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$P_D$	Power Dissipation	500(*)	mW
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(\*) 500mW at 65  $^{\circ}C$ ; derate to 300mW by 10mW/ $^{\circ}C$  from 65 $^{\circ}C$  to 85 $^{\circ}C$

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating Temperature	-55 to 125	°C	
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ C$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$V_{IH}$	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
$V_{IL}$	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
$V_{OH}$	High Level Output Voltage	2.0	$I_O = -20 \mu A$	1.9	2.0		1.9		1.9		V
		4.5	$I_O = -20 \mu A$	4.4	4.5		4.4		4.4		
		6.0	$I_O = -20 \mu A$	5.9	6.0		5.9		5.9		
		4.5	$I_O = -4.0 mA$	4.18	4.31		4.13		4.10		
		6.0	$I_O = -5.2 mA$	5.68	5.8		5.63		5.60		
$V_{OL}$	Low Level Output Voltage	2.0	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	V
		4.5	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	
		6.0	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	
		4.5	$I_O = 4.0 mA$		0.17	0.26		0.33		0.40	
		6.0	$I_O = 5.2 mA$		0.18	0.26		0.33		0.40	
$I_I$	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu A$
$I_{CC}$	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			4		40		80	$\mu A$

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

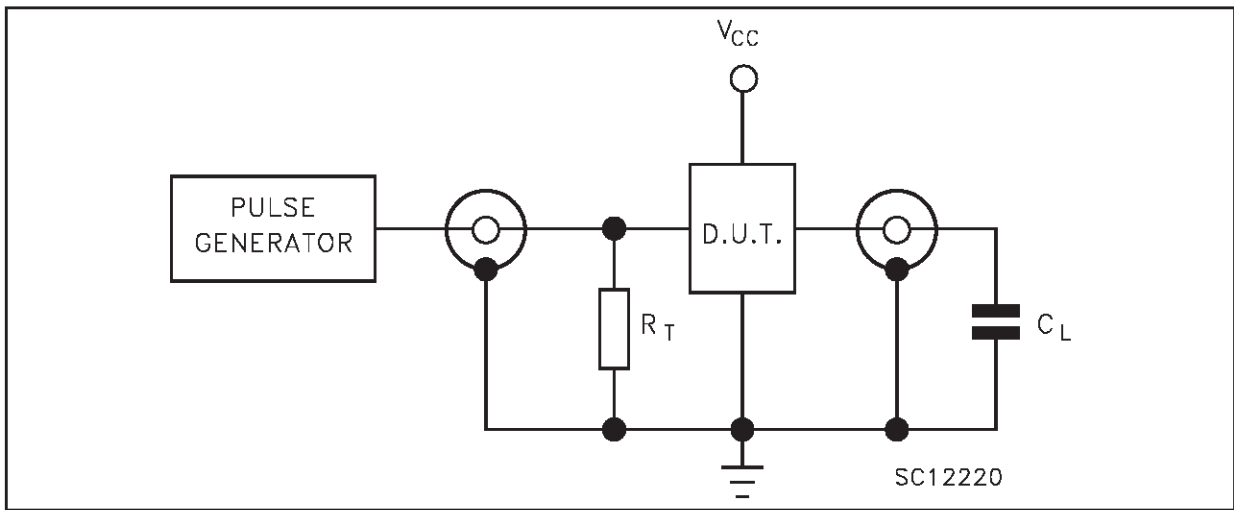
Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH}$ $t_{THL}$	Output Transition Time	2.0			30	75		95		115	ns
		4.5			8	15		19		23	
		6.0			7	13		16		20	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (SCK - QH')	2.0			78	145		180		220	ns
		4.5			20	29		36		44	
		6.0			16	25		31		37	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (SCLR - QH')	2.0			90	175		220		265	ns
		4.5			24	35		44		53	
		6.0			20	30		37		45	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (SLOAD - QH')	2.0			80	175		220		265	ns
		4.5			22	35		44		53	
		6.0			18	30		37		45	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (RCK - QH')	2.0	SLOAD = "L"		112	210		265		315	ns
		4.5			30	42		53		63	
		6.0			24	36		45		54	
$f_{MAX}$	Maximum Clock Frequency	2.0		6.0	12		4.8		4.0		MHz
		4.5		30	48		24		20		
		6.0		35	50		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (SCK, RCK)	2.0			20	75		95		110	ns
		4.5			7	15		19		22	
		6.0			4	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (SCLR, SLOAD)	2.0			25	75		95		110	ns
		4.5			7	15		19		22	
		6.0			5	13		16		19	
$t_s$	Minimum Set-up Time (RCK - SLOAD)	2.0			48	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
$t_s$	Minimum Set-up Time (SI, SCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
$t_s$	Minimum Set-up Time (PI, RCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
$t_h$	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
$t_{REM}$	Minimum Removal Time	2.0			12	75		95		115	ns
		4.5			4	15		19		23	
		6.0			3	13		16		20	

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	5.0			5	10		10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	5.0			60						pF

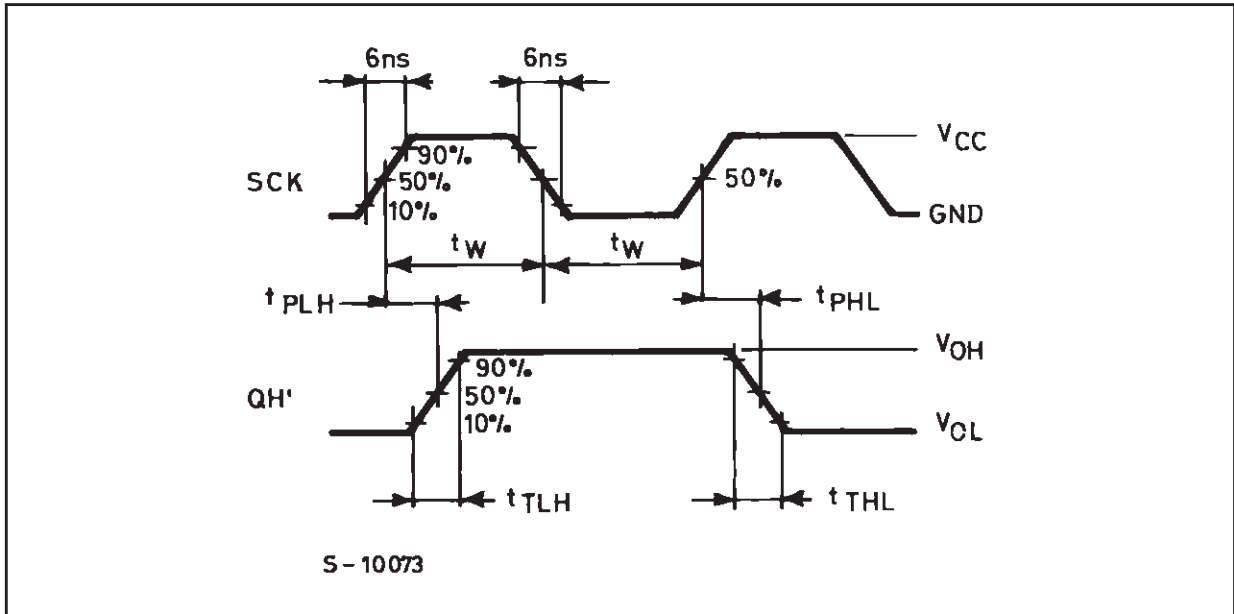
1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

**TEST CIRCUIT**

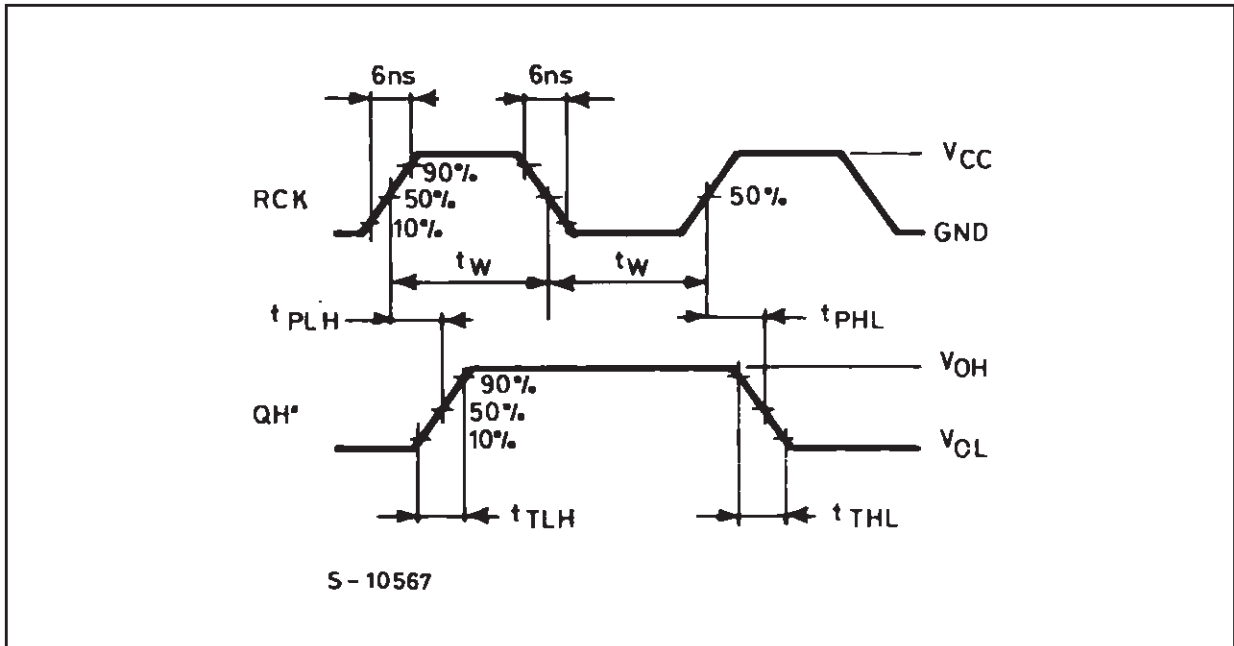


C<sub>L</sub> = 50pF or equivalent (includes jig and probe capacitance)  
 R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

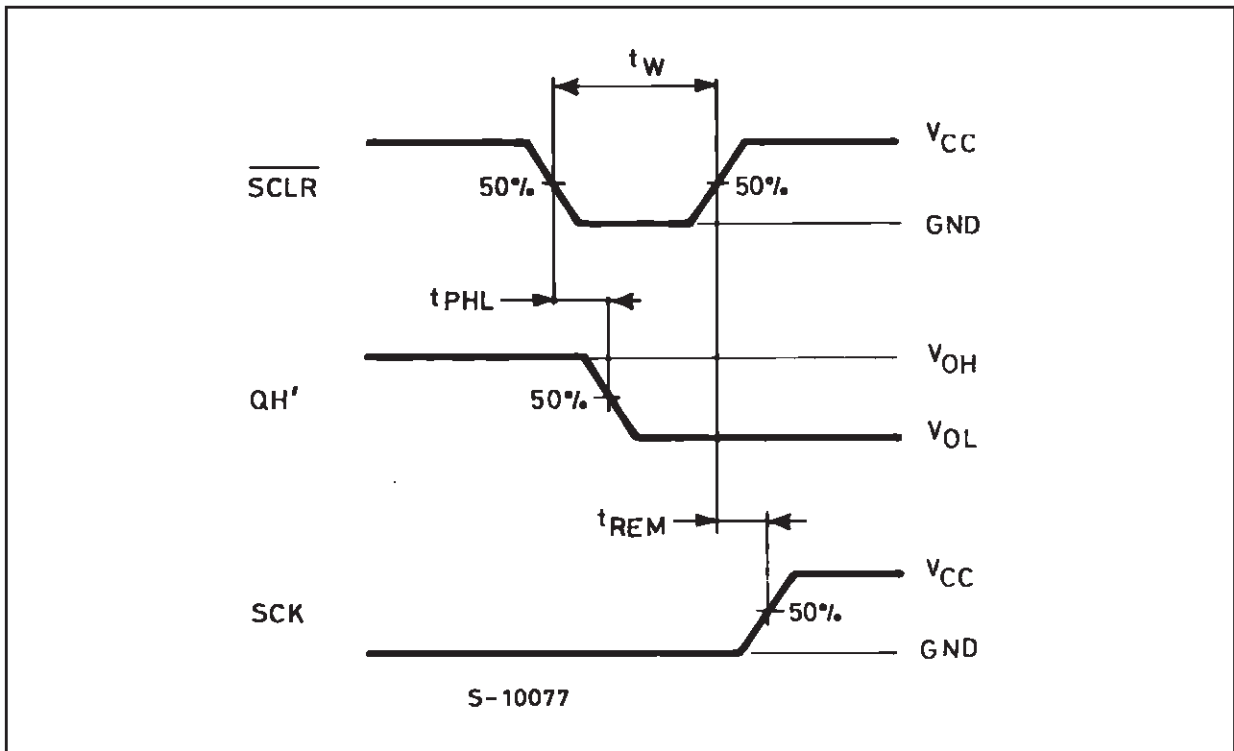
**WAVEFORM 1 : MINIMUM PULSE WIDTH, PROPAGATION DELAY TIME(f=1MHz; 50% duty cycle)**

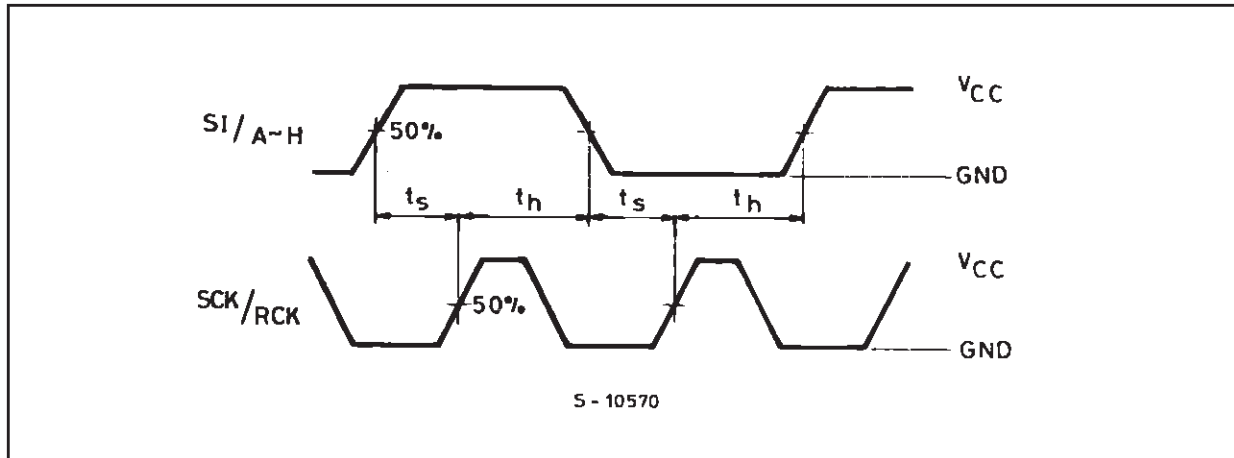
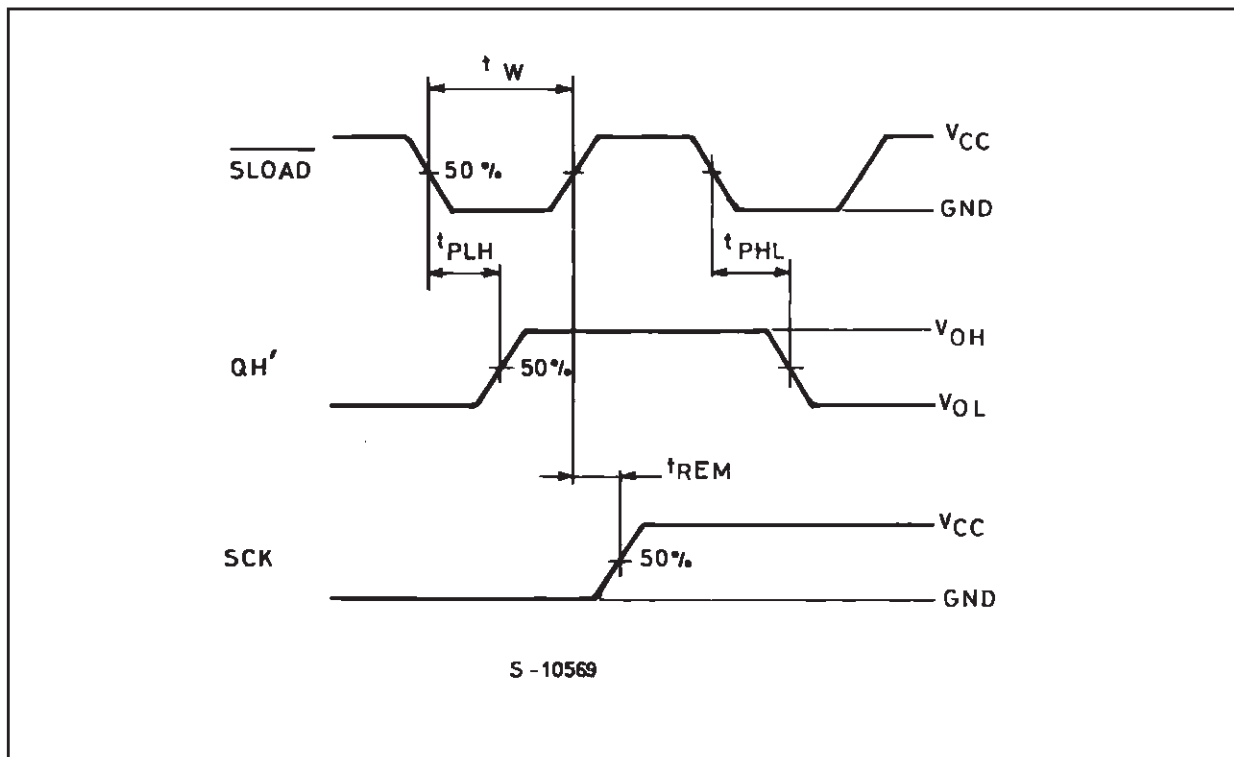


WAVEFORM 2 : MINIMUM PULSE WIDTH, PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)

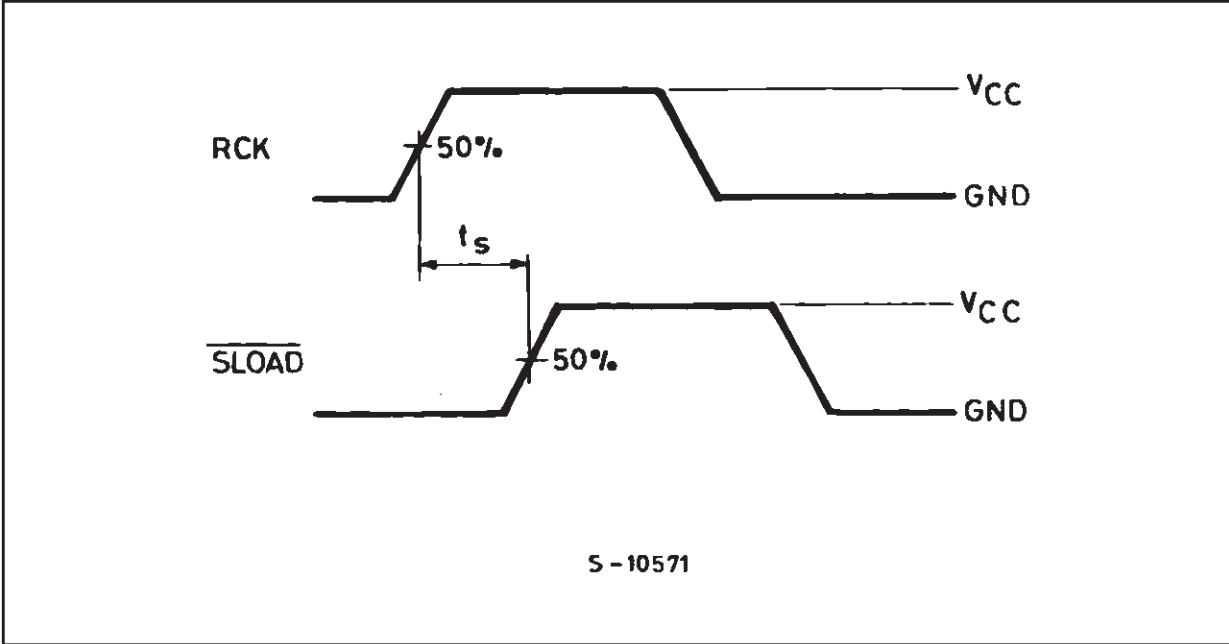


WAVEFORM 3 : MINIMUM PULSE WIDTH AND REMOVAL TIME (f=1MHz; 50% duty cycle)

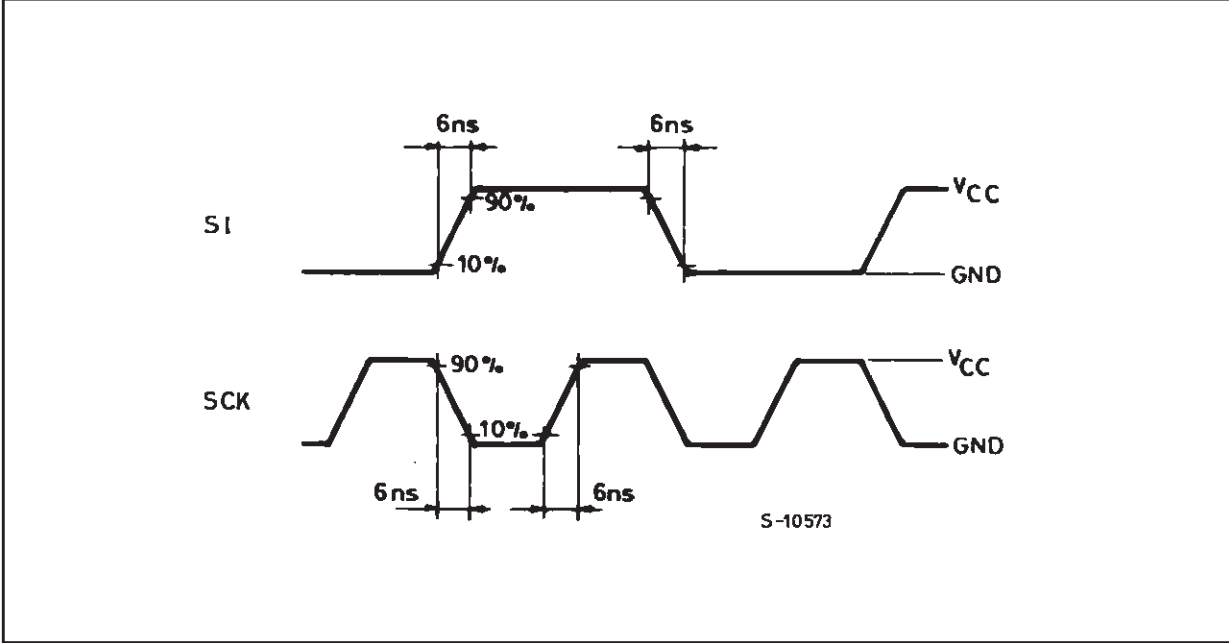


**WAVEFORM 4 : MINIMUM SETUP AND HOLD TIME** (f=1MHz; 50% duty cycle)**WAVEFORM 5 : PROPAGATION DELAY, MINIMUM PULSE WIDTH, REMOVAL TIME**  
(f=1MHz; 50% duty cycle)

WAVEFORM 6: MINIMUM SETUP TIME (f=1MHz; 50% duty cycle)

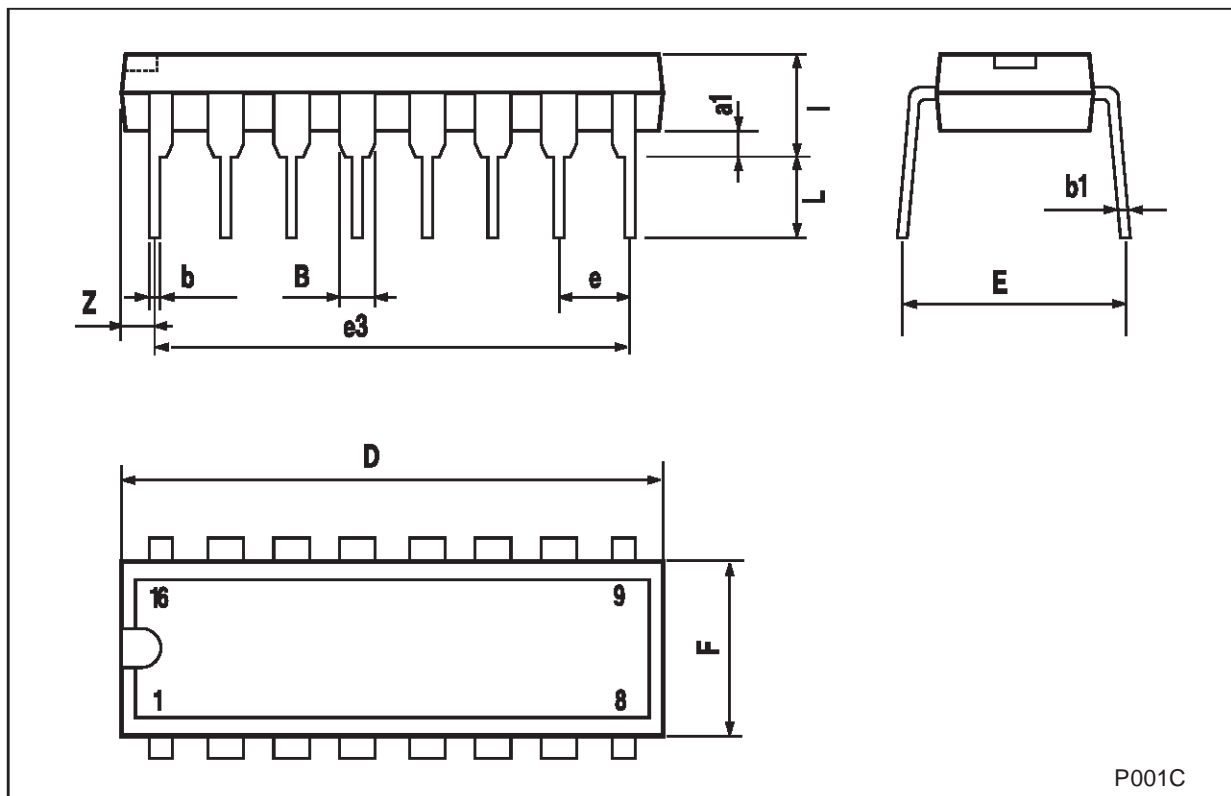


WAVEFORM 7: INPUT WAVEFORM (f=1MHz; 50% duty cycle)



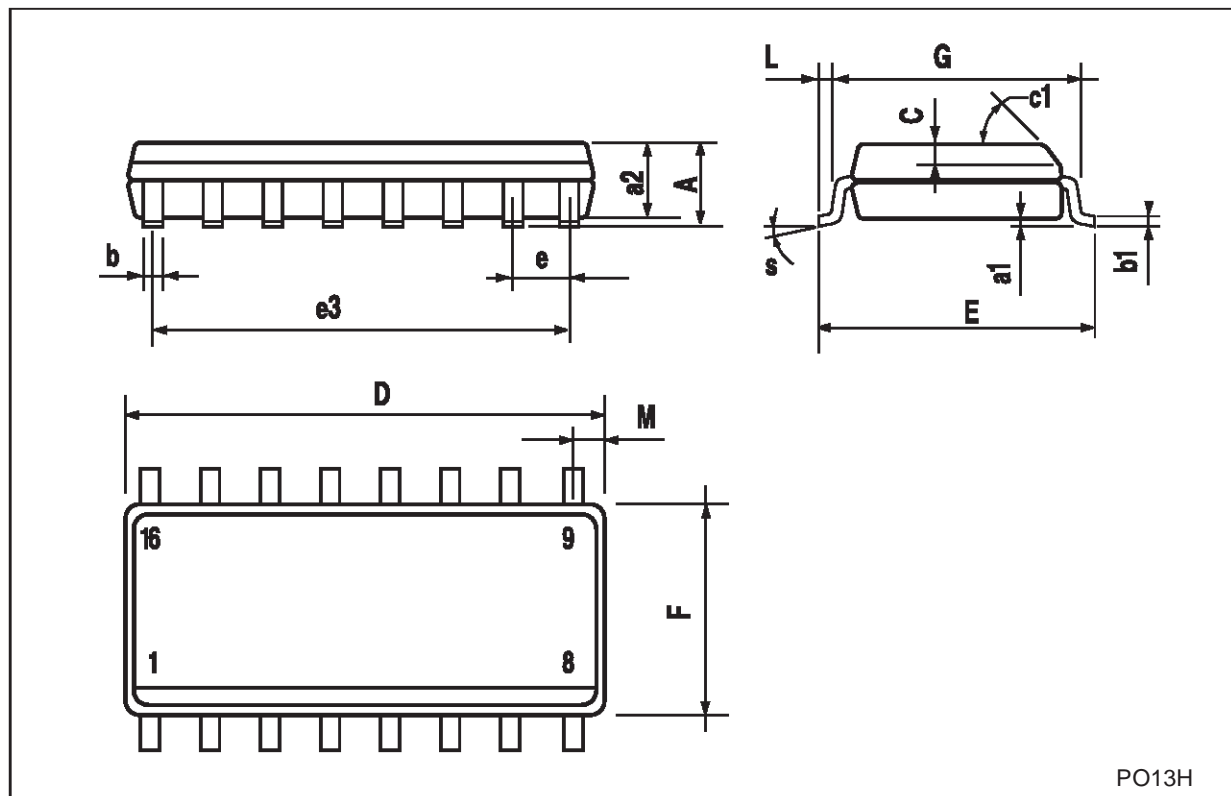
### Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



## SO-16 MECHANICAL DATA

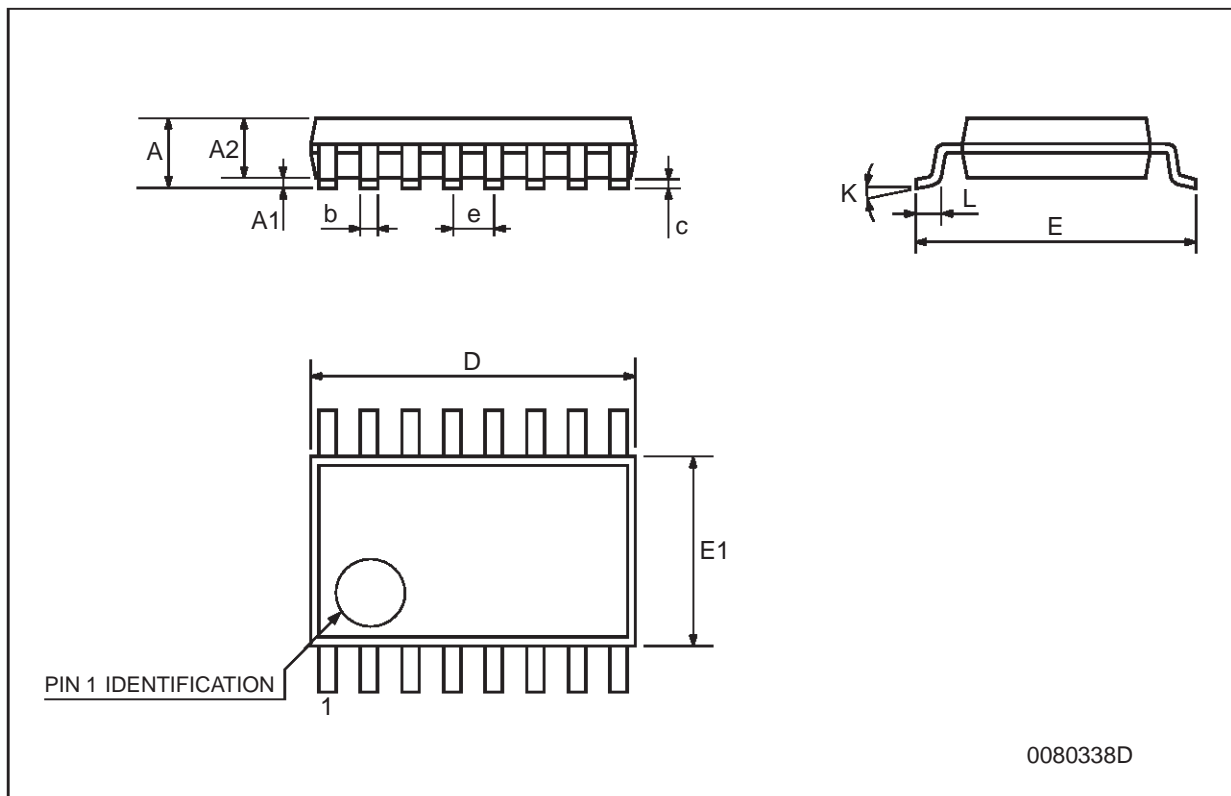
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

## TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>