



STB140NF75 STP140NF75 STB140NF75-1

N-CHANNEL 75V - 0.0065 Ω -120A D²PAK/I²PAK/TO-220
STripFET™ II POWER MOSFET

AUTOMOTIVE SPECIFIC

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB140NF75	75 V	<0.0075 Ω	120 A(**)
STP140NF75	75 V	<0.0075 Ω	120 A(**)
STB140NF75-1	75 V	<0.0075 Ω	120 A(**)

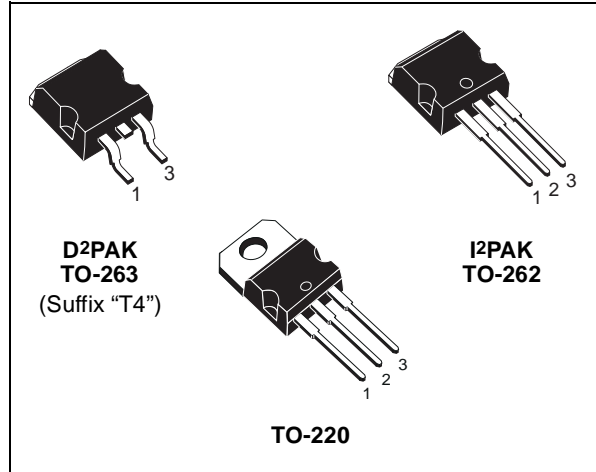
- TYPICAL R_{DS(on)} = 0.0065 Ω
- SURFACE-MOUNTING D²PAK (TO-263)
POWER PACKAGE

DESCRIPTION

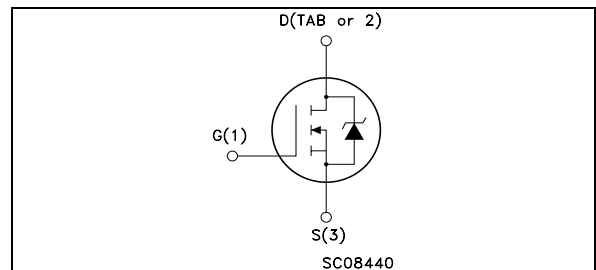
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED
- SOLENOID AND RELAY DRIVERS
- AUTOMOTIVE 42V BATTERY DRIVERS



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB140NF75T4	B140NF75	D ² PAK	TAPE & REEL
STP140NF75	P140NF75	TO-220	TUBE
STB140NF75-1	B140NF75	I ² PAK	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	75	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	75	V
V _{GS}	Gate- source Voltage	± 20	V
I _D (**)	Drain Current (continuous) at T _C = 25°C	120	A
I _D	Drain Current (continuous) at T _C = 100°C	100	A
I _{DM} (●)	Drain Current (pulsed)	480	A
P _{tot}	Total Dissipation at T _C = 25°C	310	W
	Derating Factor	2.08	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	10	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	750	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Operating Junction Temperature		

(●) Pulse width limited by safe operating area.
(**) Current Limited by Package

(1) I_{SD} ≤ 120A, di/dt ≤ 400A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}
(2) Starting T_j = 25 °C, I_D = 60 A, V_{DD} = 30V

STB140NF75 STP140NF75 STB150NF75-1

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.48	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
Rthj-pcb	Thermal Resistance Junction-pcb	Max	see curve on page 6	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose (for 10 sec. 1.6 mm from case)		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA V _{GS} = 0	75			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	2		4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 70 A		0.0065	0.0075	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 15 V I _D = 70 A		160		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		5000 960 310		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 38\text{ V}$ $I_D = 70\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		30 140		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=60\text{ V}$ $I_D=120\text{ A}$ $V_{GS}= 10\text{ V}$ (see test circuit, Figure 4)		160 28 70	218	nC nC nC

SWITCHING OFF

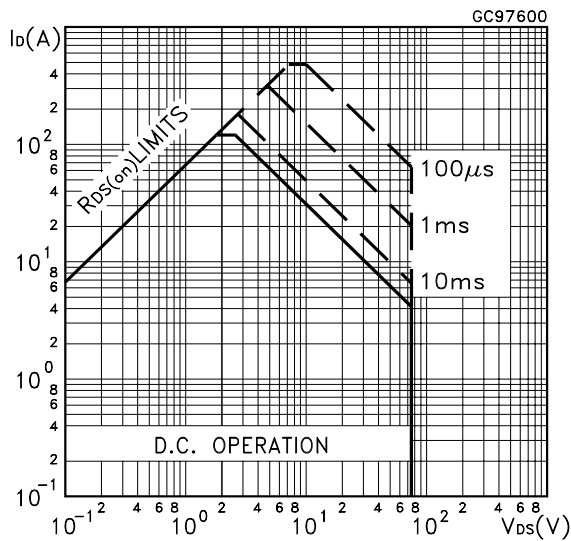
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 38\text{ V}$ $I_D = 70\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		130 90		ns ns

SOURCE DRAIN DIODE

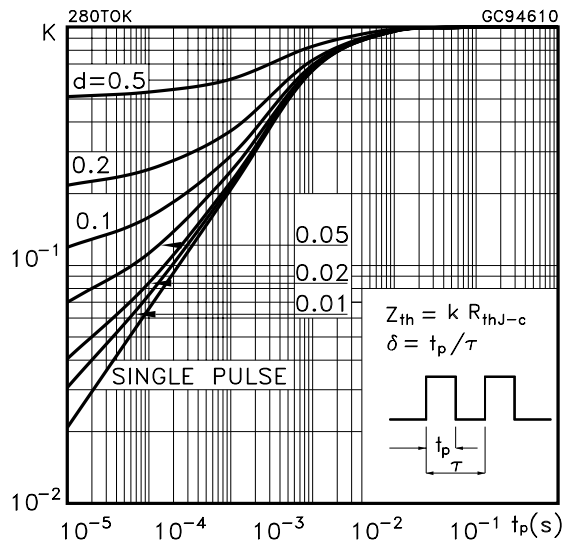
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				120 480	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 120\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 120\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 35\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		115 450 8		ns nC A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 (•) Pulse width limited by safe operating area.

Safe Operating Area

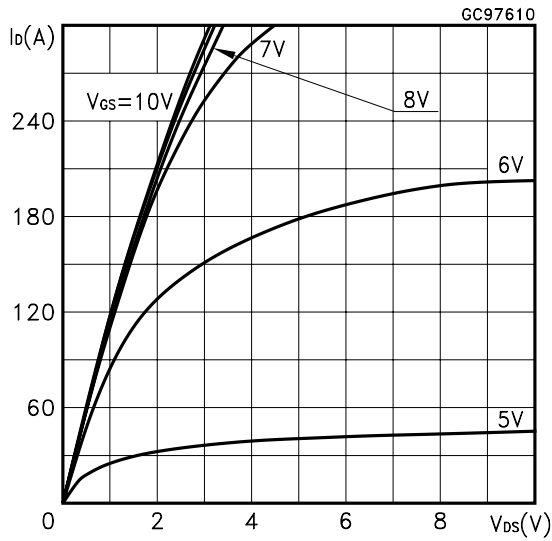


Thermal Impedance

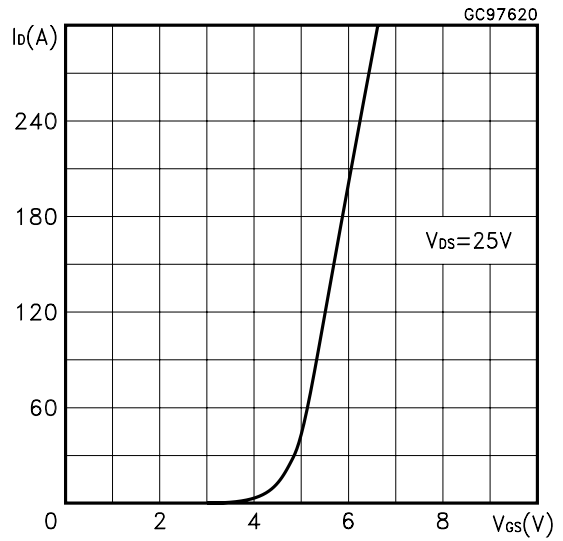


STB140NF75 STP140NF75 STB150NF75-1

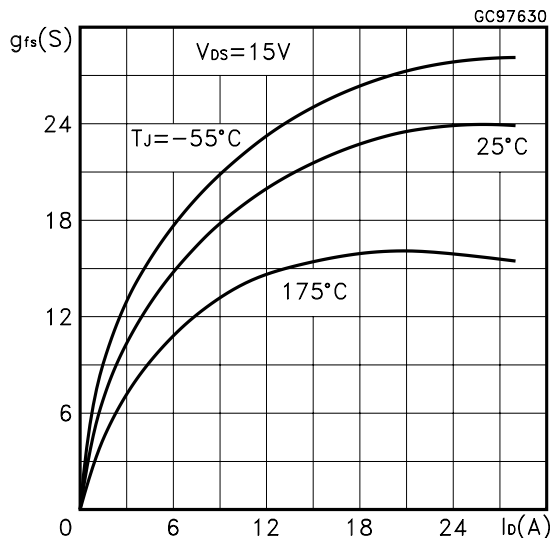
Output Characteristics



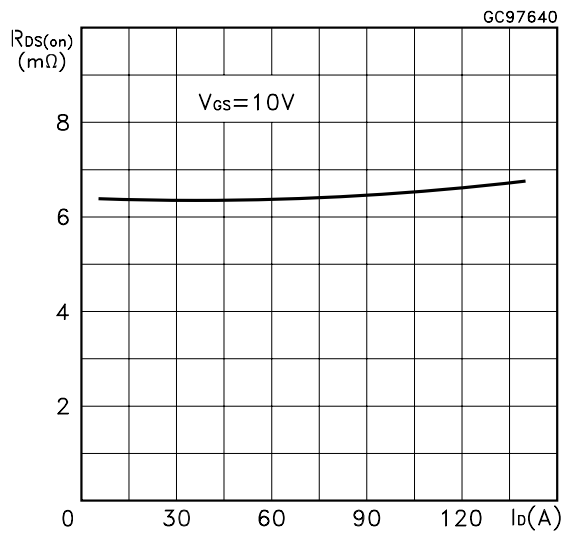
Transfer Characteristics



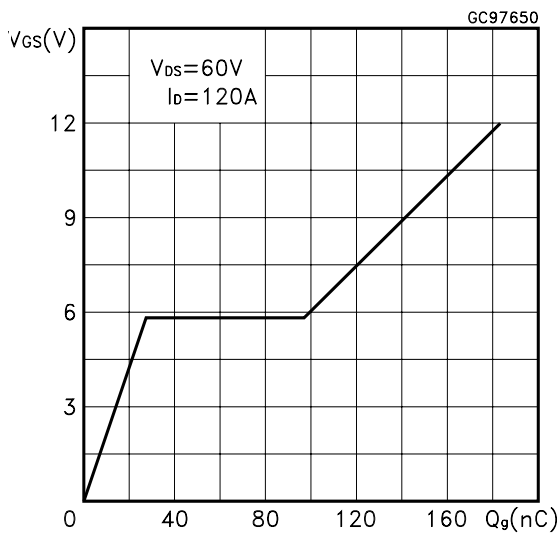
Transconductance



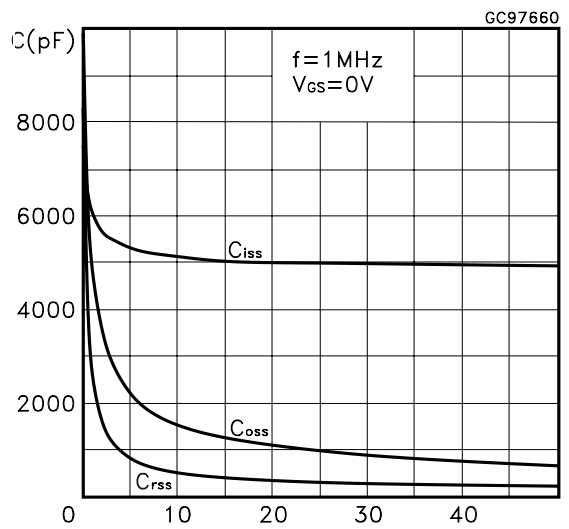
Static Drain-source On Resistance



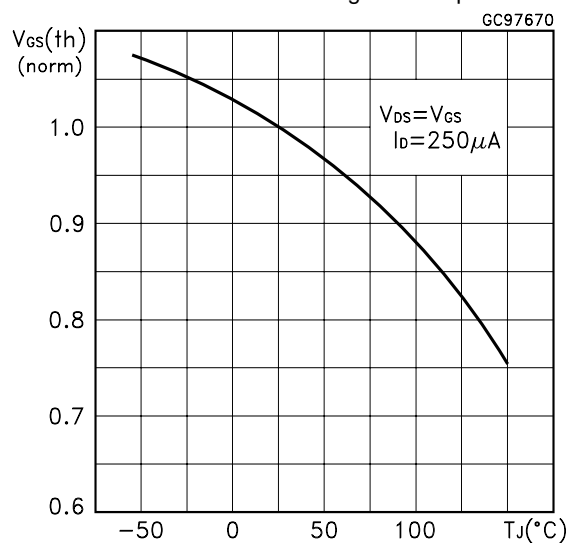
Gate Charge vs Gate-source Voltage



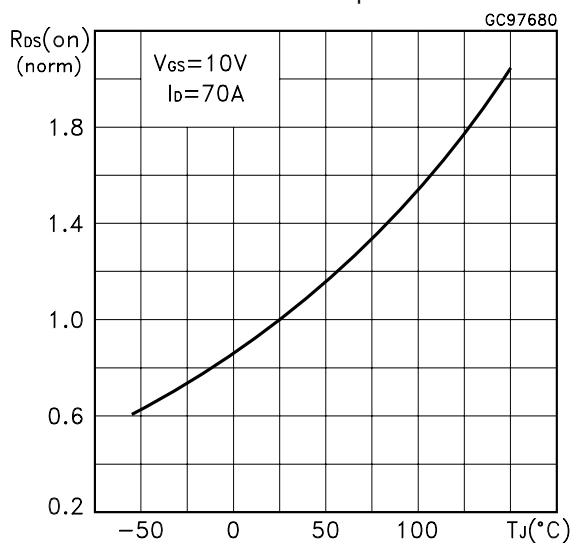
Capacitance Variations



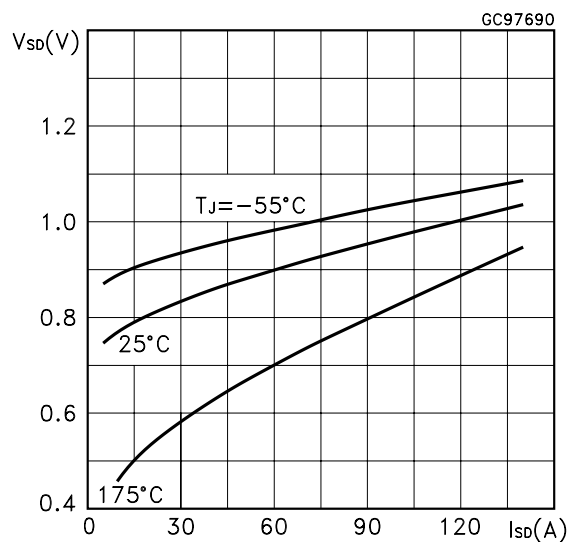
Normalized Gate Threshold Voltage vs Temperature



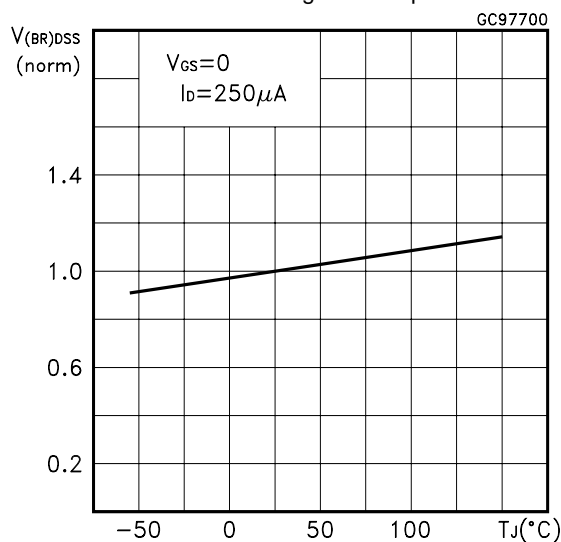
Normalized on Resistance vs Temperature



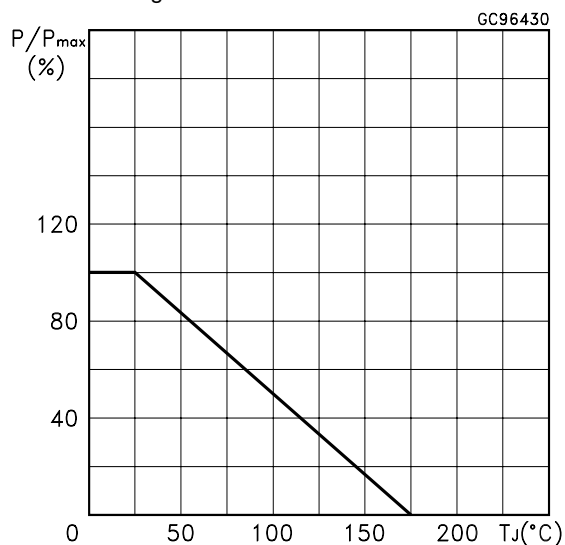
Source-drain Diode Forward Characteristics



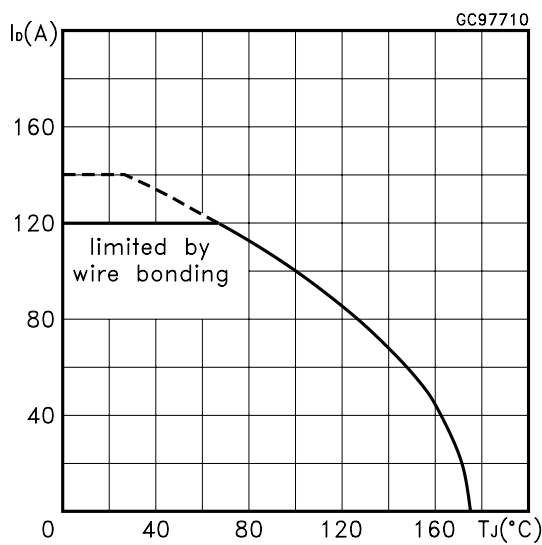
Normalized Breakdown Voltage vs Temperature.



Power Derating vs Tc

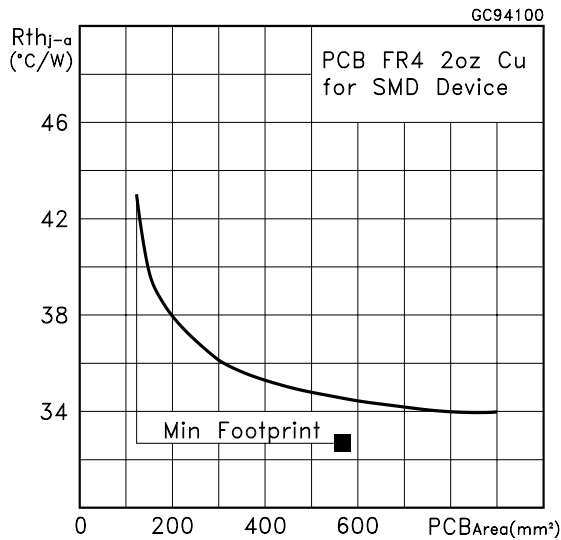


Max Id Current vs Tc.

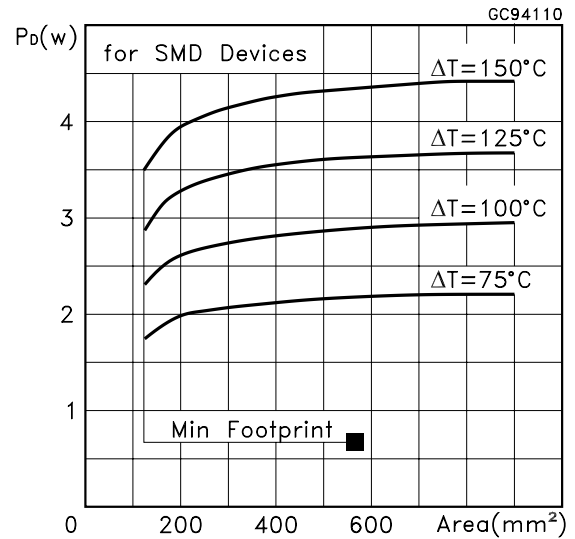


STB140NF75 STP140NF75 STB150NF75-1

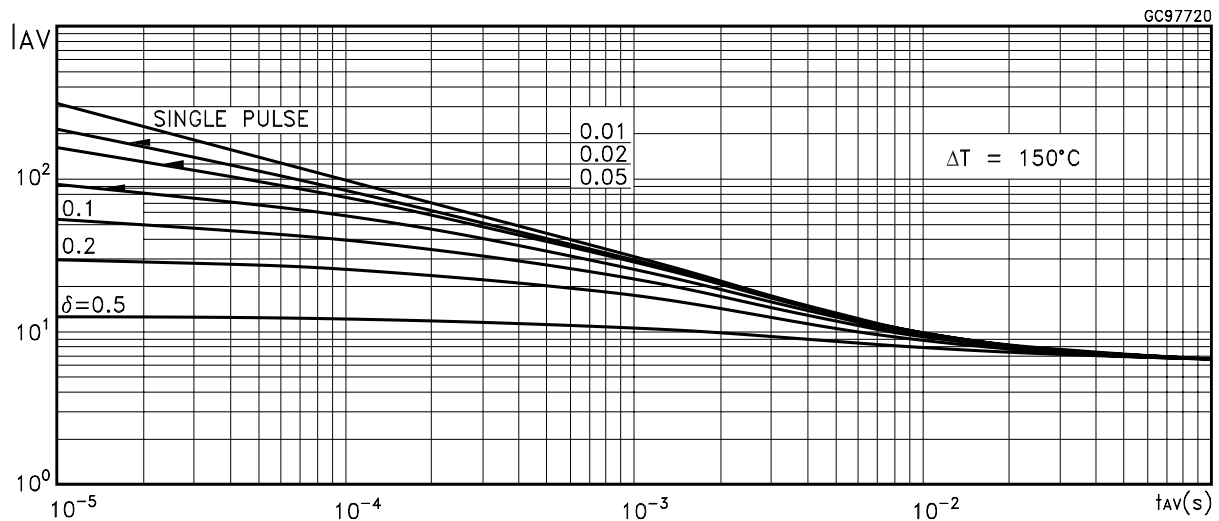
Thermal Resistance Rthj-a vs PCB Copper Area



Max Power Dissipation vs PCB Copper Area



Allowable Iav vs. Time in Avalanche



The previous curve gives the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$$P_{D(AVE)} = 0.5 * (1.3 * BV_{DSS} * I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$$

Where:

- I_{AV} is the Allowable Current in Avalanche
- $P_{D(AVE)}$ is the Average Power Dissipation in Avalanche (Single Pulse)
- t_{AV} is the Time in Avalanche

To derate above 25 °C, at fixed I_{AV} , the following equation must be applied:

$$I_{AV} = 2 * (T_{jmax} - T_{CASE}) / (1.3 * BV_{DSS} * Z_{th})$$

Where:

$Z_{th} = K * R_{th}$ is the value coming from Normalized Thermal Response at fixed pulse width equal to T_{AV} .



SPICE THERMAL MODEL

Parameter	Node	Value
CTHERM1	7 - 6	$1.49 \cdot 10^{-3}$
CTHERM2	6 - 5	$3.50 \cdot 10^{-2}$
CTHERM3	5 - 4	$5.94 \cdot 10^{-2}$
CTHERM4	4 - 3	$9.74 \cdot 10^{-2}$
CTHERM5	3 - 2	$8.86 \cdot 10^{-2}$
CTHERM6	2 - 1	$8.27 \cdot 10^{-1}$
R THERM1	7 - 6	0.0384
R THERM2	6 - 5	0.0624
R THERM3	5 - 4	0.072
R THERM4	4 - 3	0.0912
R THERM5	3 - 2	0.1008
R THERM6	2 - 1	0.1152

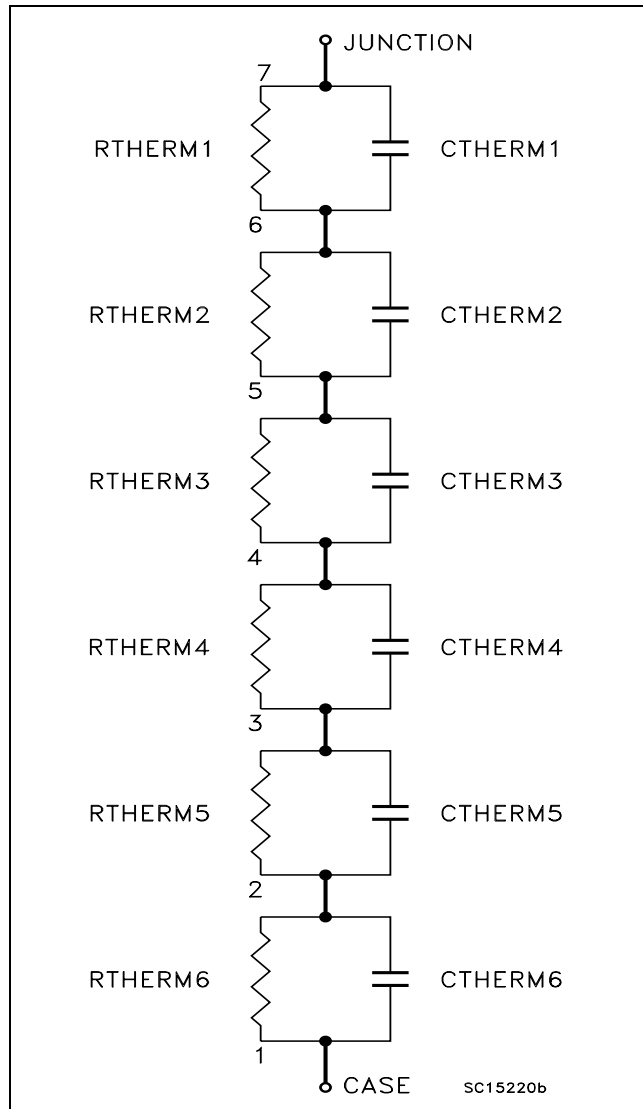


Fig. 1: Unclamped Inductive Load Test Circuit

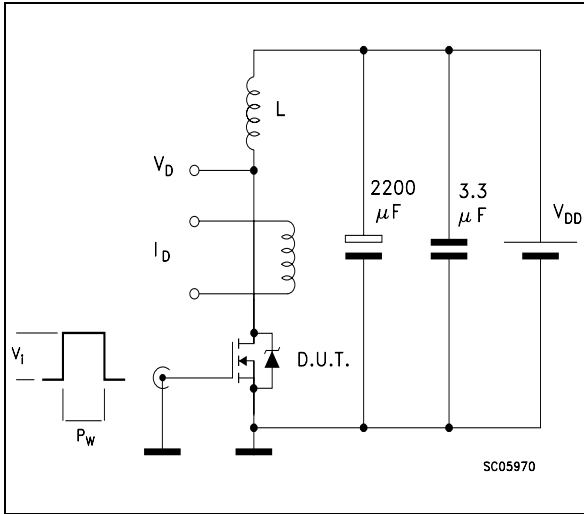


Fig. 2: Unclamped Inductive Waveform

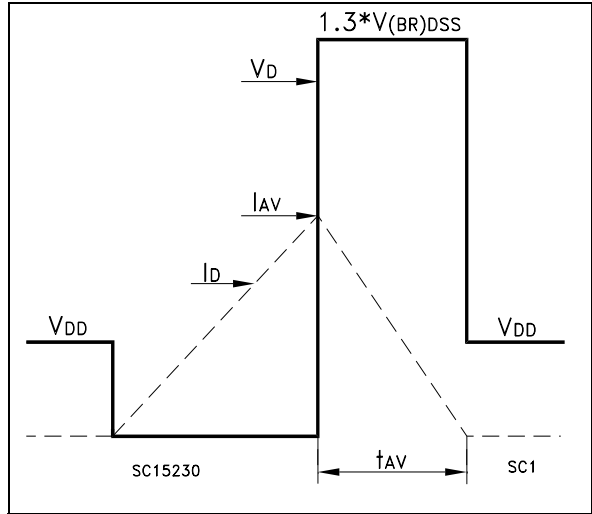


Fig. 3: Switching Times Test Circuits For Resistive Load

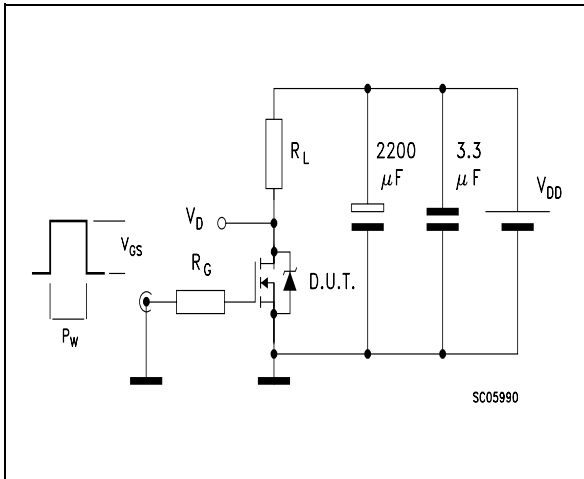


Fig. 3.1: Switching Time Waveform

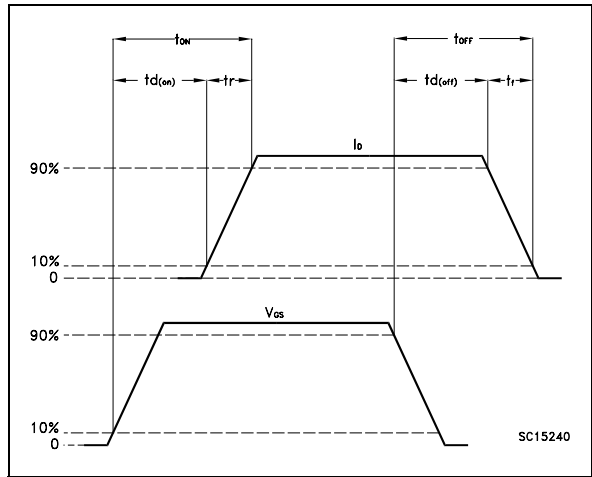


Fig. 4: Gate Charge Test Circuit

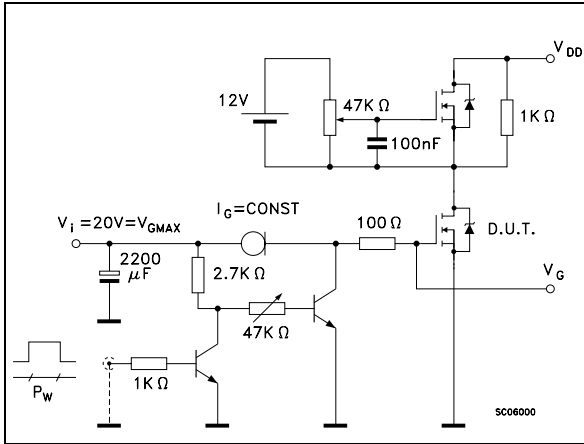


Fig. 4.1: Gate Charge Test Waveform

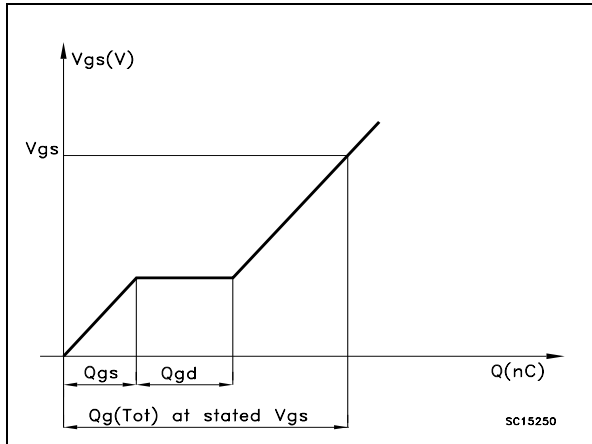


Fig. 5: Diode Switching Test Circuit

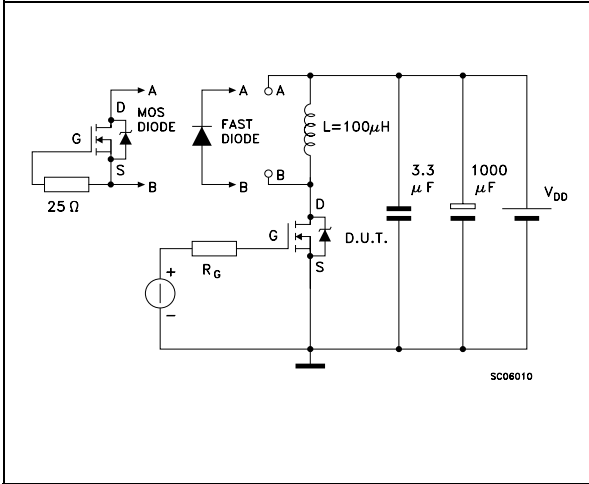
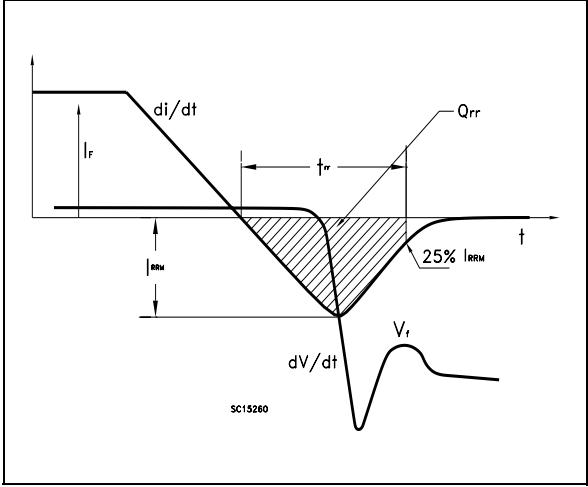
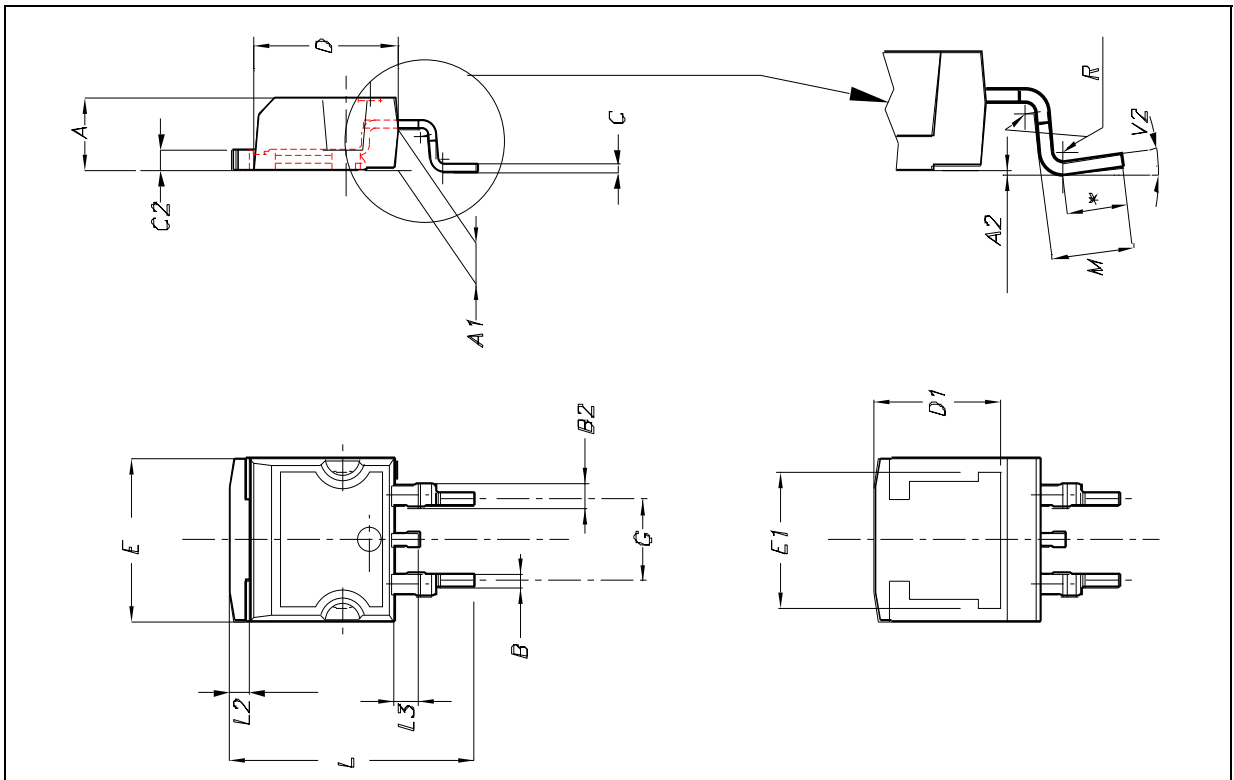


Fig. 5.1: Diode Recovery Times Waveform



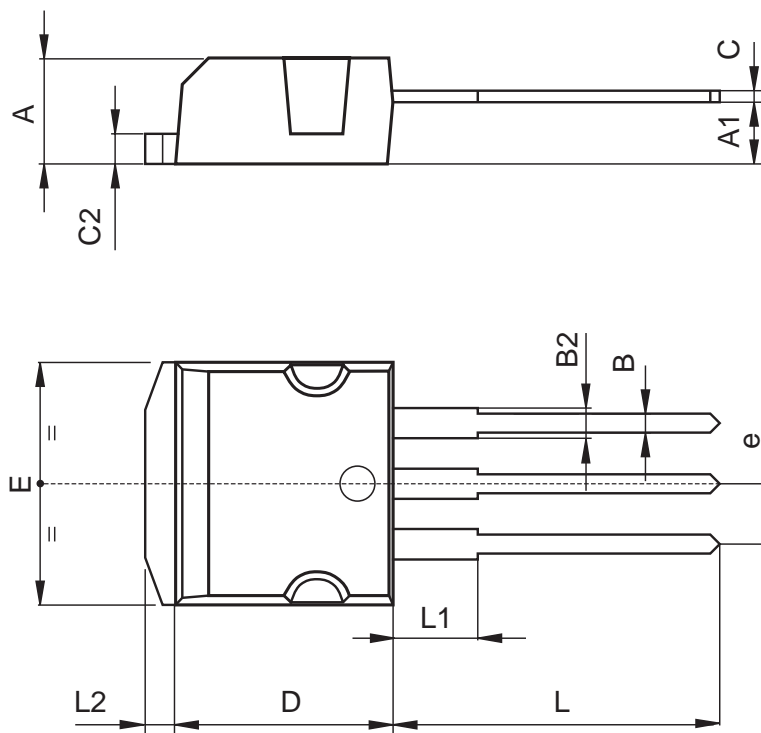
D²PAK MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°



TO-262 (I²PAK) MECHANICAL DATA

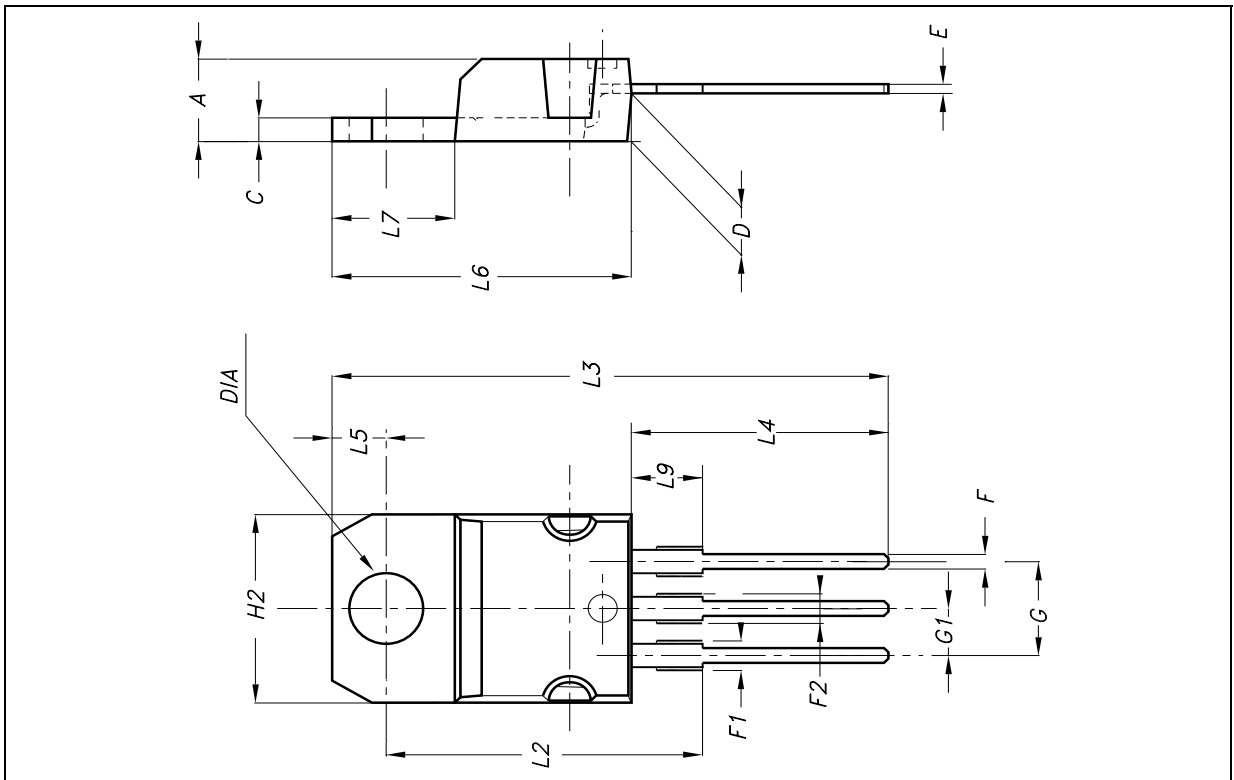
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



P011P5/E

TO-220 MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.40		2.70	0.094		0.106
H2	10		10.40	0.393		0.409
L2		16.40			0.645	
L3		28.90			1.137	
L4	13		14	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.20		6.60	0.244		0.260
L9	3.50		3.93	0.137		0.154
DIA	3.75		3.85	0.147		0.151



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics
© 2002 STMicroelectronics - All Rights Reserved

All other names are the property of their respective owners.

STMicroelectronics GROUP OF COMPANIES
Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>