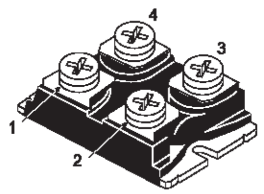
STE110NS20FD

N-CHANNEL 200V - 0.022Ω - 110A ISOTOP
MESH OVERLAY™ Power MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STE110NS20FD	200V	< 0.024Ω	110 A

- TYPICAL R_{DS}(on) = 0.022Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- ± 20V GATE TO SOURCE VOLTAGE RATING
- LOW INTRINSIC CAPACITANCE
- FAST BODY-DRAIN DIODE:LOW t_{rr}, Q_{rr}

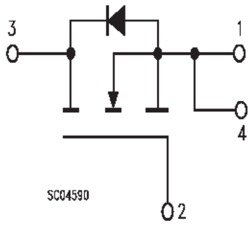


ISOTOP

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patented STrip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(ON) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLY (SMPS)
- DC-AC CONVERTER FOR WELDING EQUIPMENT AND UNINTERRUPTABLE POWER SUPPLY AND MOTOR DRIVE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source Voltage	±20	V
I_D	Drain Current (continuos) at T_C = 25°C	110	A
I_D	Drain Current (continuos) at T_C = 100°C	69	A
I_{DM} (•)	Drain Current (pulsed)	440	A
P_{TOT}	Total Dissipation at T_C = 25°C	500	W
	Derating Factor	4	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	25	V/ns
V_{ISO}	Insulation Winthstand Voltage (AC-RMS)	2500	V
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)$I_{SD} \leq 110A$, di/dt $\leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.25	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	110	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	750	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			10 100	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 50A		0.022	0.024	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, I_D = 50A		30		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		7900		pF
C_{oss}	Output Capacitance			1500		pF
C_{rss}	Reverse Transfer Capacitance			460		pF

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 100V, I_D = 50A R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		40		ns
t_r	Rise Time			130		ns
Q_g	Total Gate Charge	V_{DD} = 100V, I_D = 100A, V_{GS} = 10V		360	504	nC
Q_{gs}	Gate-Source Charge			35		nC
Q_{gd}	Gate-Drain Charge			135		nC

SWITCHING OFF

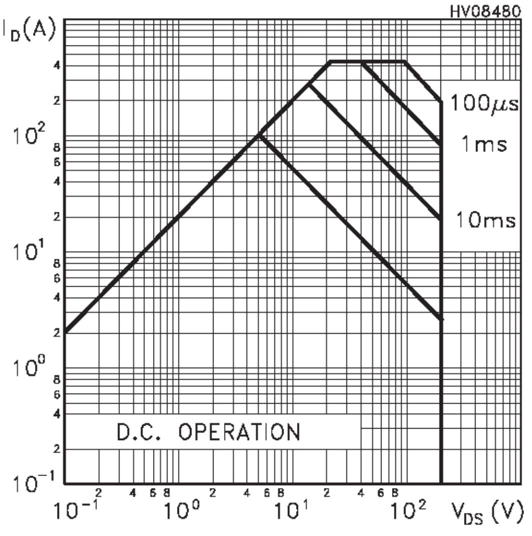
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 100V, I_D = 100A, R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		245		ns
t_f	Fall Time			140		ns
t_c	Cross-over Time			220		ns

SOURCE DRAIN DIODE

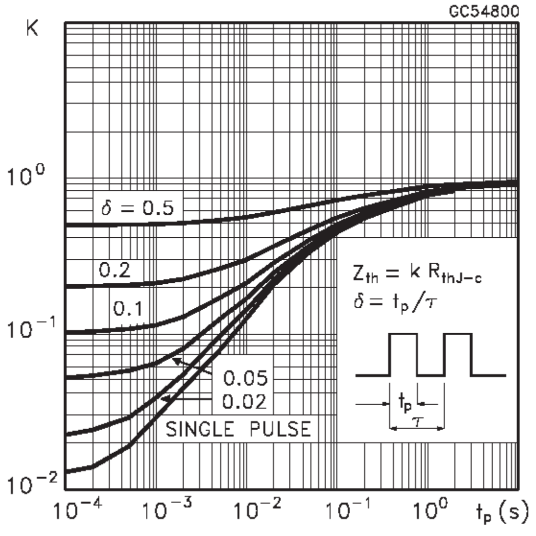
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				110	A
I_{SDM} (2)	Source-drain Current (pulsed)				440	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 100A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 100A, di/dt = 100A/µs, V_{DD} = 160V, T_j = 150°C (see test circuit, Figure 5)		225		ns
Q_{rr}	Reverse Recovery Charge			1.35		µC
I_{RRM}	Reverse Recovery Current			12		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

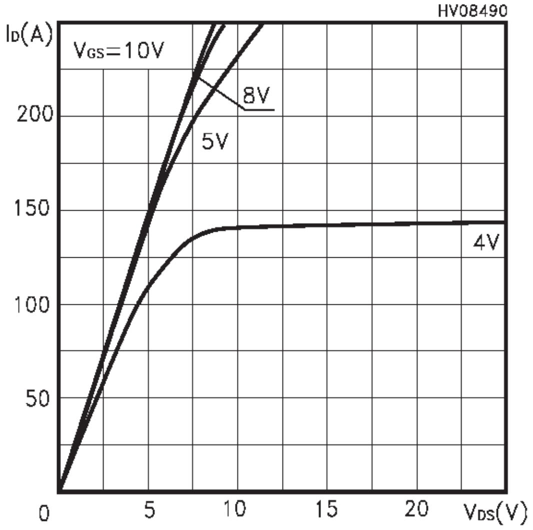
Safe Operating Area



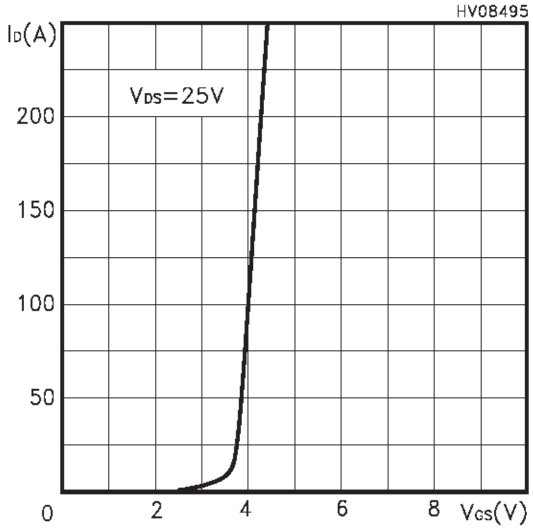
Thermal Impedance



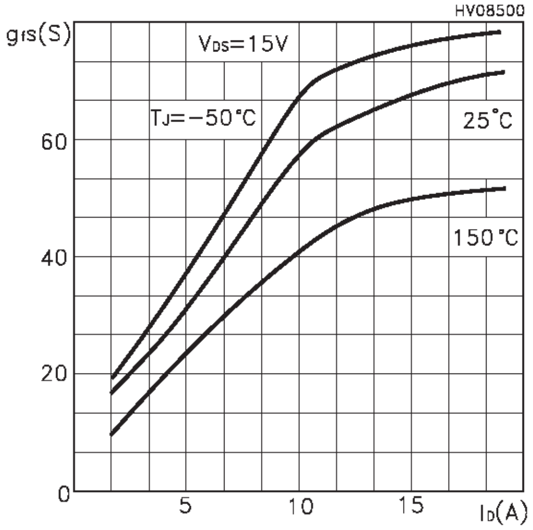
Output Characteristics



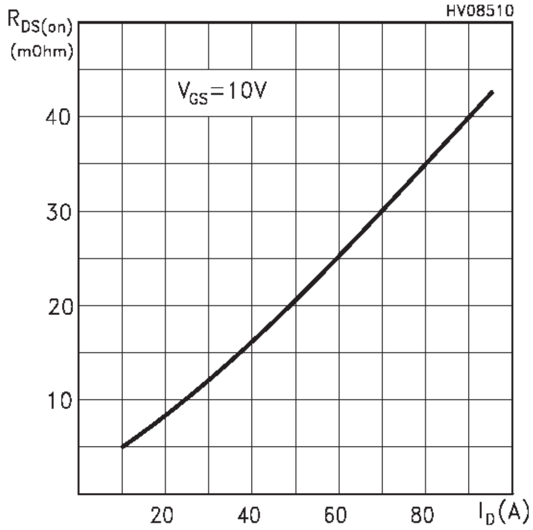
Transfer Characteristics



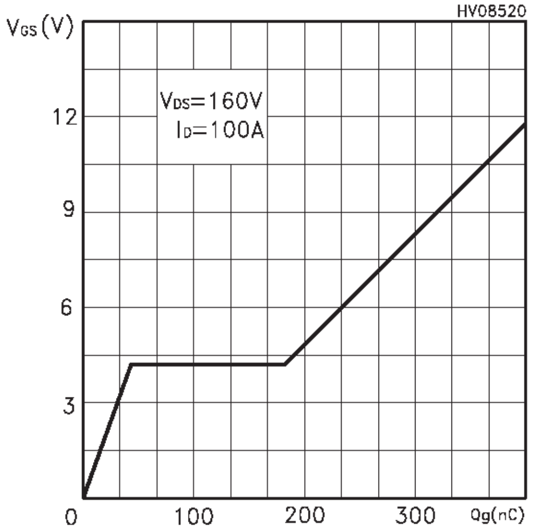
Transconductance



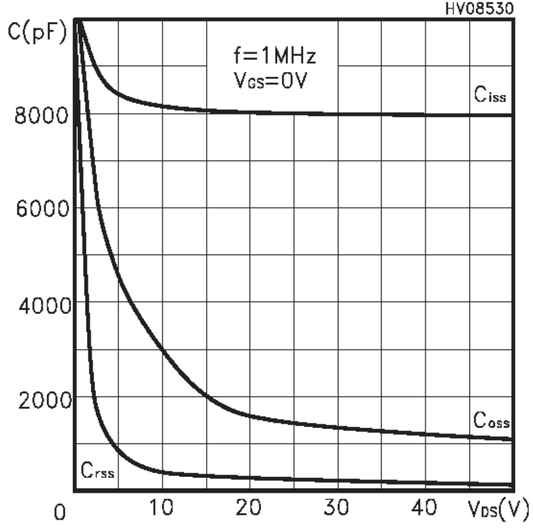
Static Drain-source On Resistance



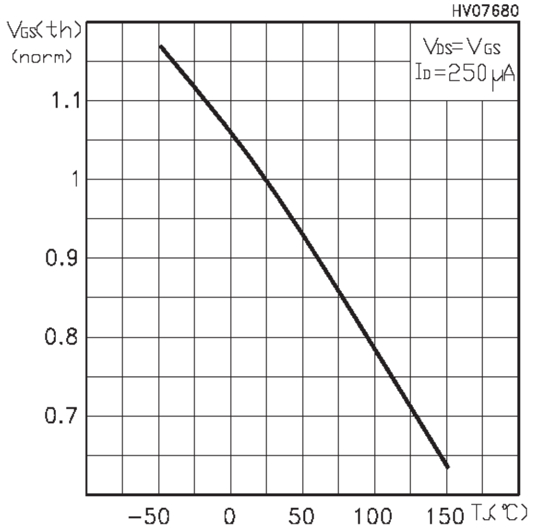
Gate Charge vs Gate-source Voltage



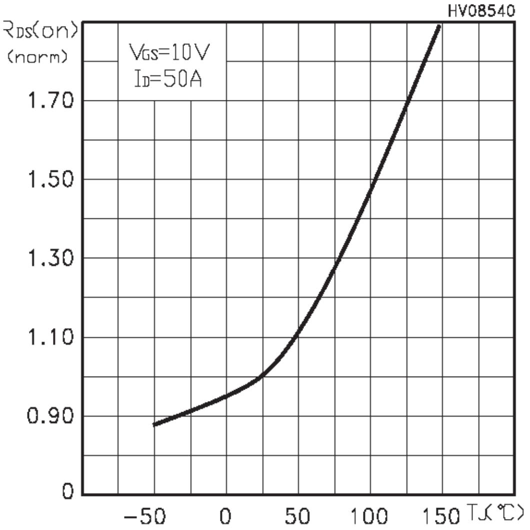
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

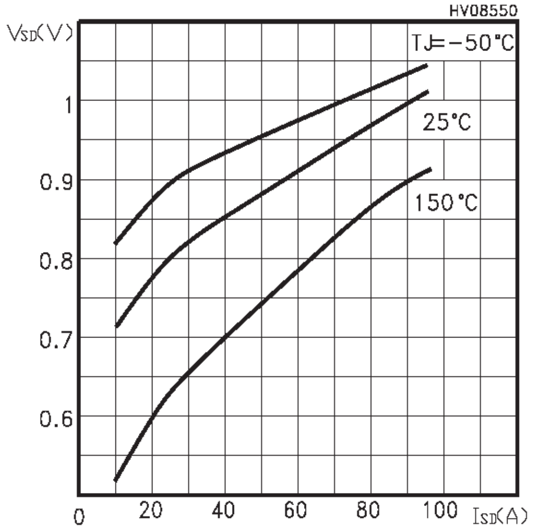


Fig. 1: Unclamped Inductive Load Test Circuit

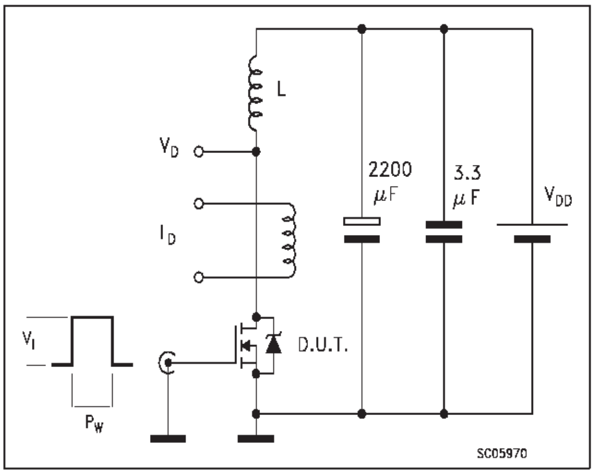


Fig. 2: Unclamped Inductive Waveform

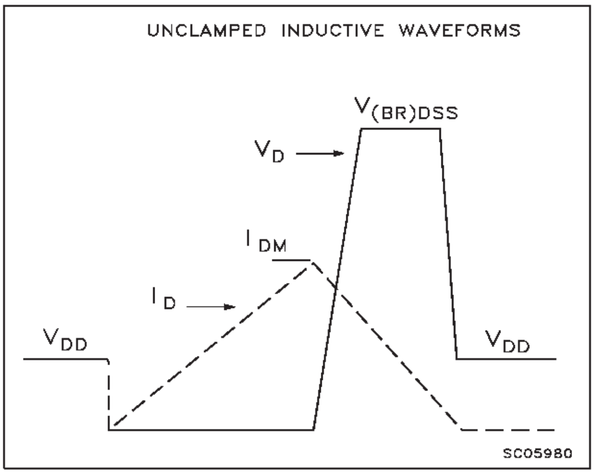


Fig. 3: Switching Times Test Circuit For Resistive Load

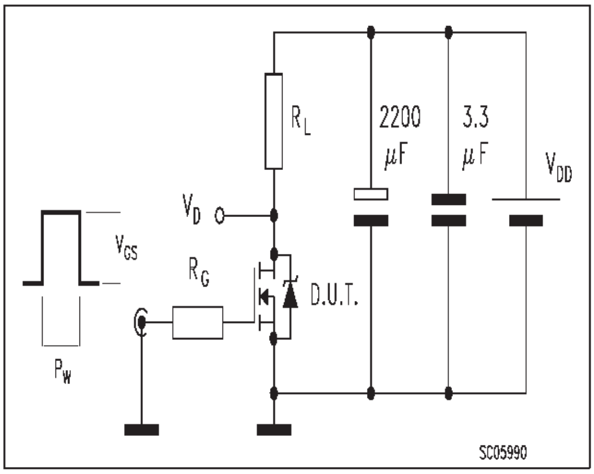


Fig. 4: Gate Charge test Circuit

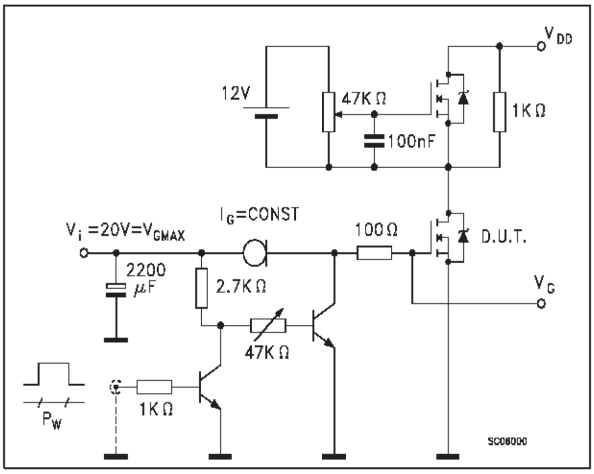
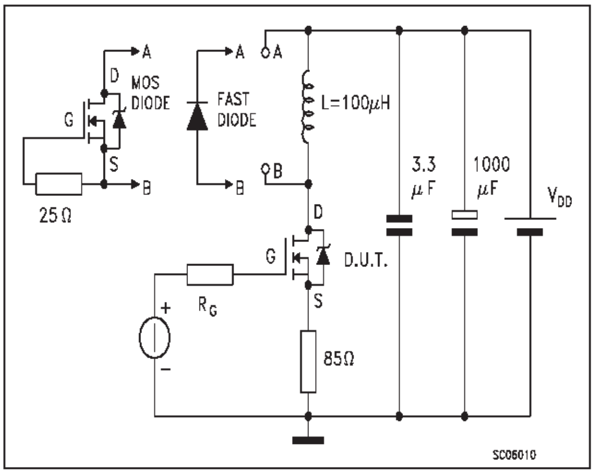
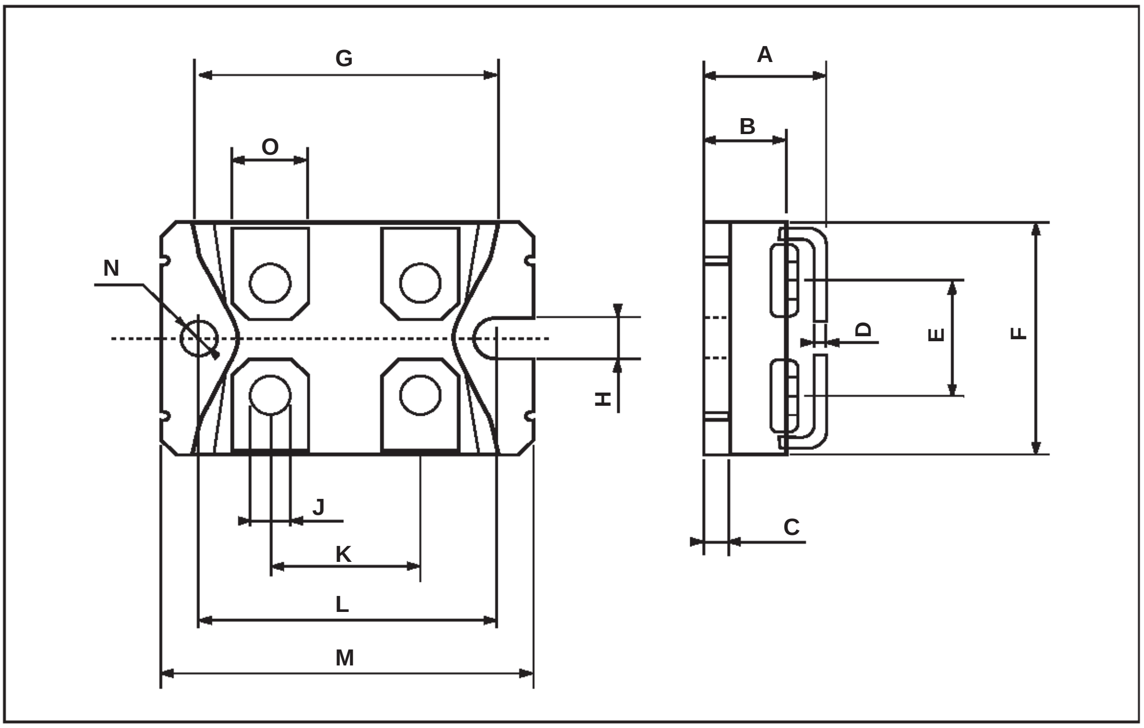


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

http://www.st.com