



STGD3NB60K

N-CHANNEL 3A - 600V - DPAK

SHORT CIRCUIT PROOF PowerMESH™ IGBT

PRELIMINARY DATA

TYPE	V _{CES}	V _{CE(sat)}	I _C
STD3NB60K	600 V	< 2.8 V	3 A

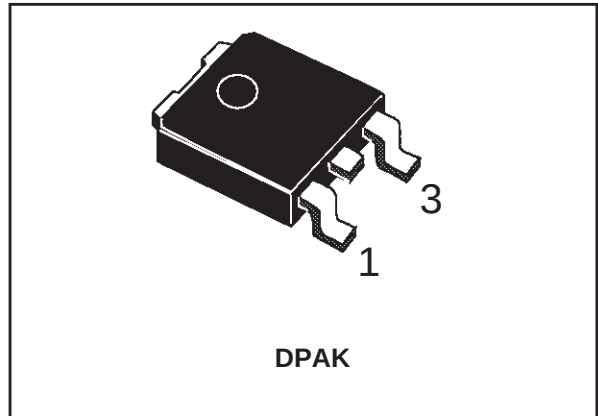
- HIGH INPUT IMPEDANCE (VOLTAGE DRIVEN)
- LOW ON-VOLTAGE DROP (V_{cesat})
- LOW ON-LOSSES
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- OFF LOSSES INCLUDE TAIL CURRENT
- VERY HIGH FREQUENCY OPERATION
- SHORT CIRCUIT RATED
- LATCH CURRENT FREE OPERATION

DESCRIPTION

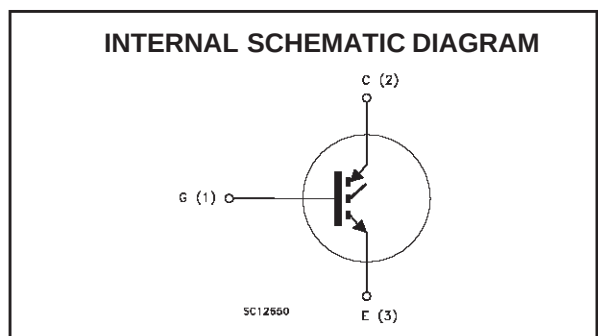
Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "K" identifies a family optimized for high frequency motor control applications with short circuit withstand capability.

APPLICATIONS

- HIGH FREQUENCY MOTOR CONTROLS
- SMPS and PFC



DPAK



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CES}	Collector-Emitter Voltage (V _{GS} = 0)	600	V
V _{ECR}	Emitter-Collector Voltage	20	V
V _{GE}	Gate-Emitter Voltage	±20	V
I _C	Collector Current (continuous) at T _C = 25°C	6	A
I _C	Collector Current (continuous) at T _C = 100°C	3	A
I _{CM} (■)	Collector Current (pulsed)	24	A
T _{SC}	Short Circuit Withstand	10	μs
P _{TOT}	Total Dissipation at T _C = 25°C	35	W
	Derating Factor	0.28	W/°C
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

STGD3NB60K

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	3.57	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	°C/W
Rthc-h	Thermal Resistance Case-heatsink Typ	0.5	°C/W

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{BR(CES)}	Collectro-Emitter Breakdown Voltage	I _C = 250 µA, V _{GE} = 0	600			V
I _{CES}	Collector cut-off (V _{GE} = 0)	V _{CE} = Max Rating, T _C = 25 °C V _{CE} = Max Rating, T _C = 125 °C			10 100	µA µA
I _{GES}	Gate-Emitter Leakage Current (V _{CE} = 0)	V _{GE} = ±20V, V _{CE} = 0			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GE(th)}	Gate Threshold Voltage	V _{CE} = V _{GE} , I _C = 250µA	5		7	V
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _{GE} = 15V, I _C = 3 A V _{GE} = 15V, I _C = 3 A, T _J =125°C		2.4 1.9	2.8	V V

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs}	Forward Transconductance	V _{CE} = 25 V, I _C =3 A	1.3	2.4		S
C _{ies}	Input Capacitance	V _{CE} = 25V, f = 1 MHz, V _{GE} = 0		235		pF
C _{oes}	Output Capacitance			33		pF
C _{res}	Reverse Transfer Capacitance			6.6		pF
Q _g	Total Gate Charge	V _{CE} = 480V, I _C = 3 A, V _{GE} = 15V		21	27	nC
Q _{ge}	Gate-Emitter Charge			T.B.D.		nC
Q _{gc}	Gate-Collector Charge			T.B.D.		nC
t _{scw}	Short Circuit Withstand Time	V _{ce} = 0.5 BV _{ces} , V _{GE} = 15 V, T _J = 125°C, R _G = 10 Ω	10			µs

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on Delay Time	V _{CC} = 480 V, I _C = 3 A R _G = 10Ω, V _{GE} = 15 V		16		ns
t _r	Rise Time			30		ns
(di/dt) _{on}	Turn-on Current Slope	V _{CC} = 480 V, I _C = 7 A R _G =10Ω V _{GE} = 15 V, T _J = 125°C		400		A/µs
E _{on}	Turn-on Switching Losses			37		µJ

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_c	Cross-over Time	$V_{CC} = 480\text{ V}$, $I_C = 3\text{ A}$, $R_{GE} = 10\ \Omega$, $V_{GE} = 15\text{ V}$		90		ns
$t_r(V_{off})$	Off Voltage Rise Time			36		ns
$t_{d(off)}$	Delay Time			53		ns
t_f	Fall Time			70		ns
$E_{off(**)}$	Turn-off Switching Loss			33		μJ
E_{ts}	Total Switching Loss			65		μJ
t_c	Cross-over Time	$V_{CC} = 480\text{ V}$, $I_C = 3\text{ A}$, $R_{GE} = 10\ \Omega$, $V_{GE} = 15\text{ V}$ $T_J = 125\text{ }^\circ\text{C}$		180		ns
$t_r(V_{off})$	Off Voltage Rise Time			82		ns
$t_{d(off)}$	Delay Time			58		ns
t_f	Fall Time			110		ns
$E_{off(**)}$	Turn-off Switching Loss			88		μJ
E_{ts}	Total Switching Loss			125		μJ

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by max. junction temperature.
 (***) Losses include Also the Tail (Jedec Standardization)

Fig. 1: Gate Charge test Circuit

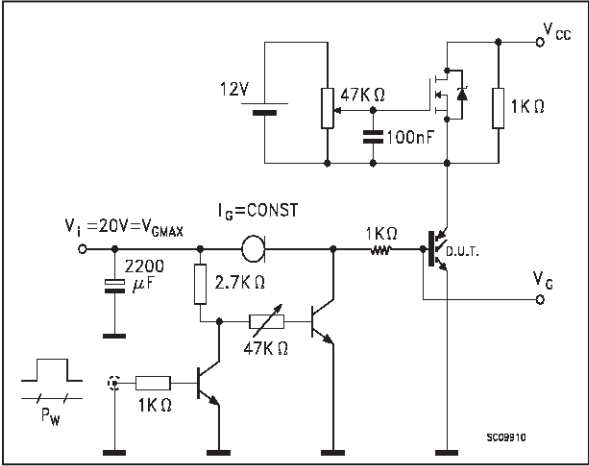
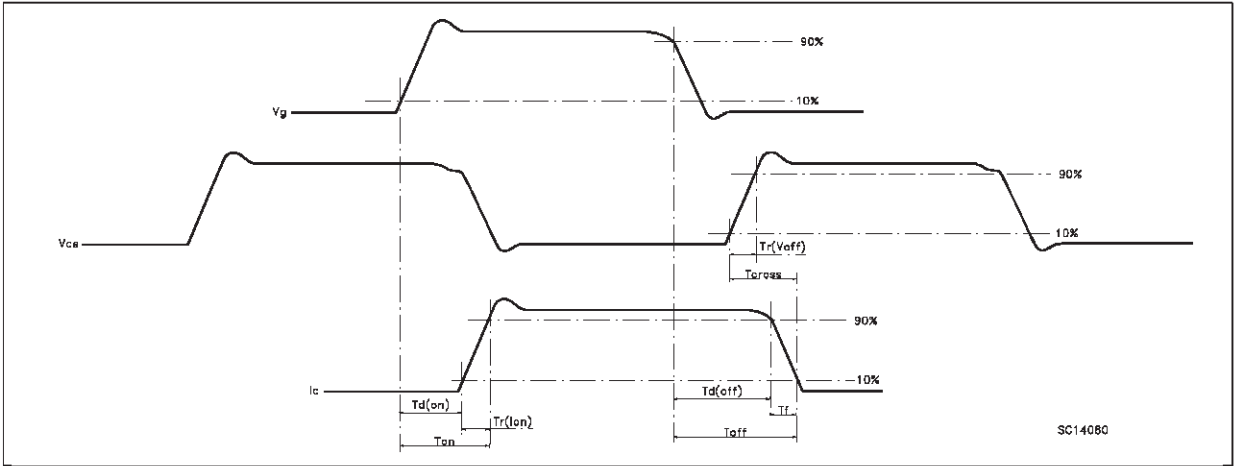
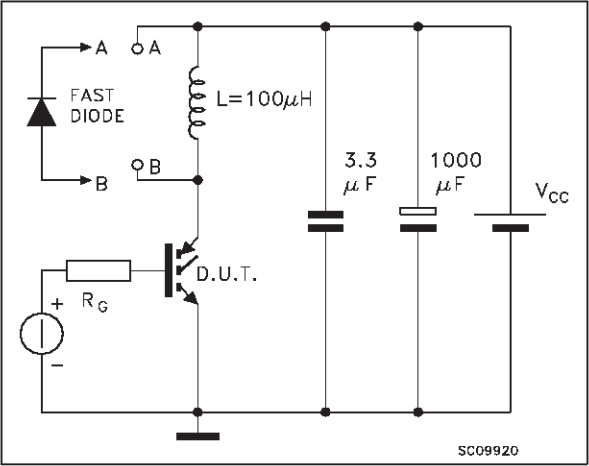
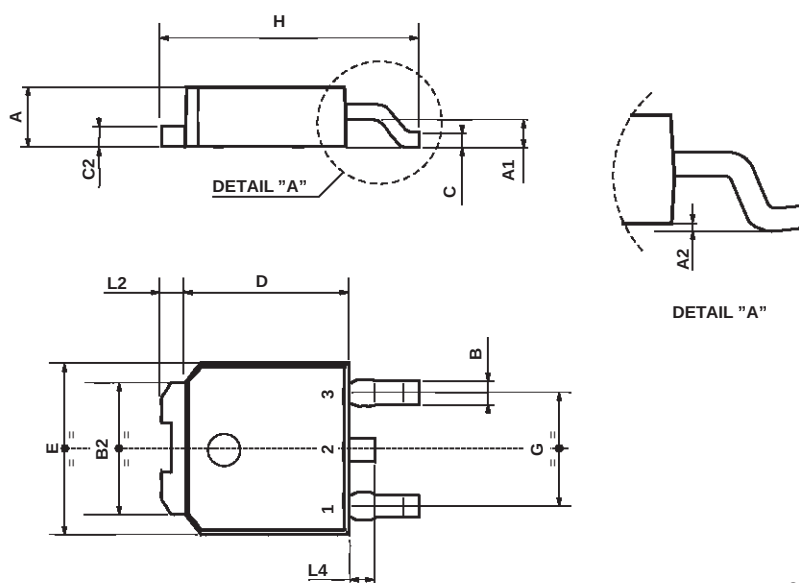


Fig. 2: Test Circuit For Inductive Load Switching



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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