



STW20NM50

N-CHANNEL 500V - 0.20Ω - 20A TO-247

MDmesh™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STW20NM50	500V	< 0.25Ω	20 A

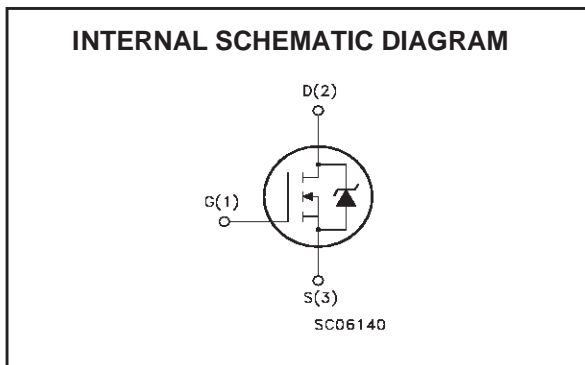
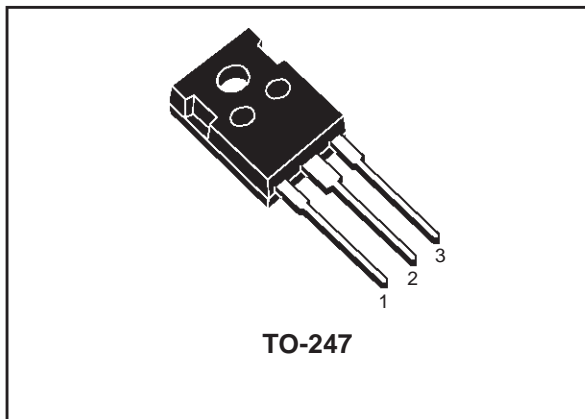
- TYPICAL R_{DS(on)} = 0.20Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate- source Voltage	±30	V
I _D	Drain Current (continuous) at T _C = 25°C	20	A
I _D	Drain Current (continuous) at T _C = 100°C	12.6	A
I _{DM} (i)	Drain Current (pulsed)	80	A
P _{TOT}	Total Dissipation at T _C = 25°C	214	W
	Derating Factor	1.44	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(*)Pulse width limited by safe operating area

(1) I_{SD} ≤ 20A, di/dt ≤ 400A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

STW20NM50

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.585	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	10	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = 5 A, V _{DD} = 35 V)	650	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 100	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 10A		0.20	0.25	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 10A		10		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1480		pF
C _{oss}	Output Capacitance			285		pF
C _{rss}	Reverse Transfer Capacitance			34		pF
C _{oss eq.} (2)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 400V		130		pF
R _G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.6		Ω

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

ELECTRICAL CHARACTERISTICS (CONTINUED)
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250V, I_D = 10A$		24		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		16		ns
Q_g	Total Gate Charge	$V_{DD} = 400V, I_D = 20A,$ $V_{GS} = 10V$		40	56	nC
Q_{gs}	Gate-Source Charge			13		nC
Q_{gd}	Gate-Drain Charge			19		nC

SWITCHING OFF

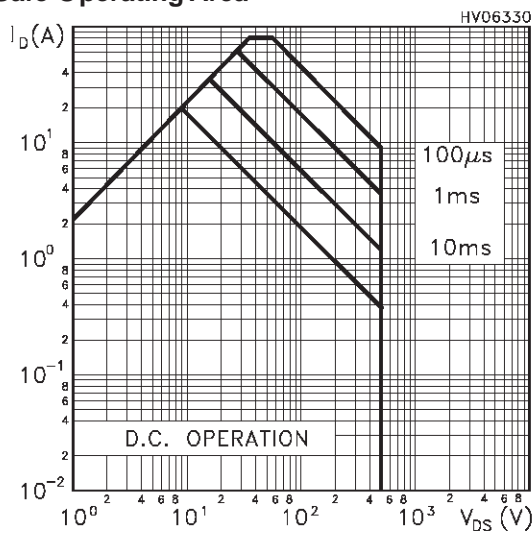
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400V, I_D = 20A,$		9		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		8.5		ns
t_c	Cross-over Time			23		ns

SOURCE DRAIN DIODE

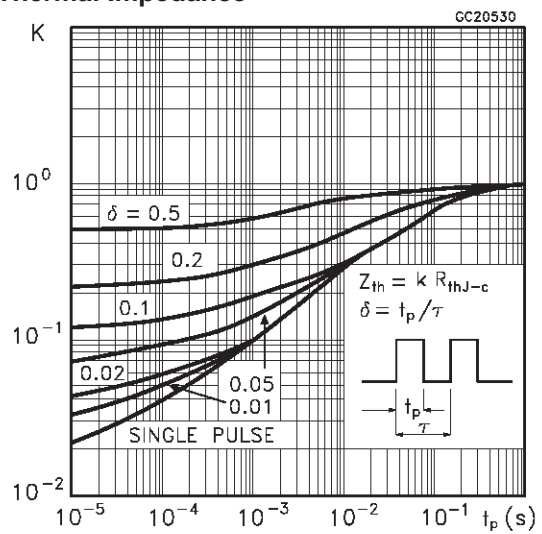
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				20	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				80	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 20A, V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 20A, di/dt = 100A/\mu s,$ $V_{DD} = 60V, T_j = 150^\circ C$ (see test circuit, Figure 5)		435		ns
Q_{rr}	Reverse Recovery Charge			5.9		μC
I_{RRM}	Reverse Recovery Current			27		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

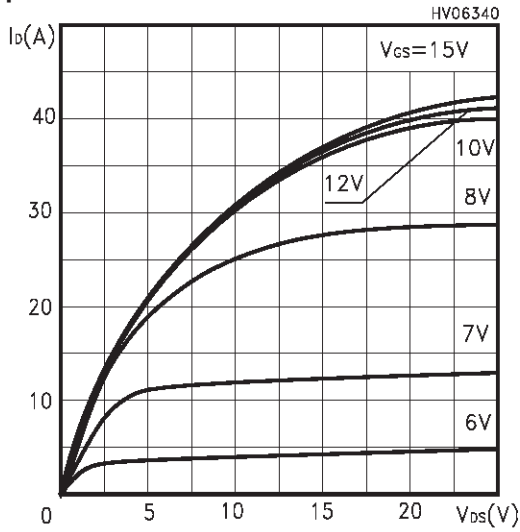
Safe Operating Area



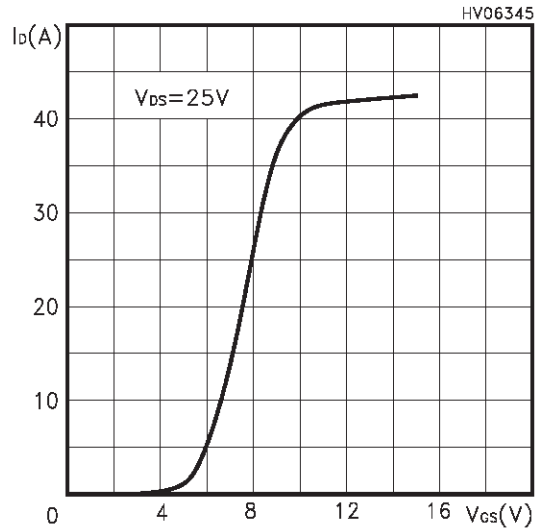
Thermal Impedance



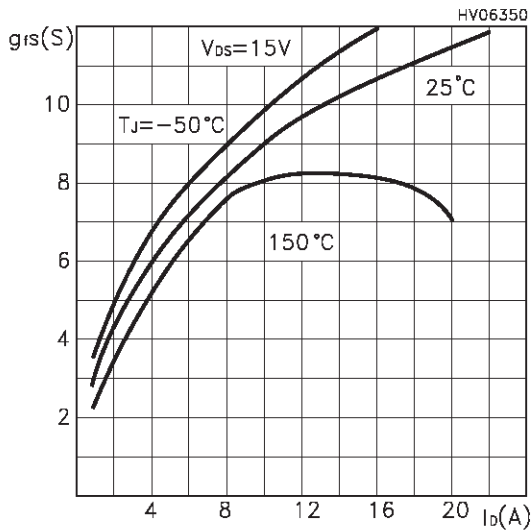
Output Characteristics



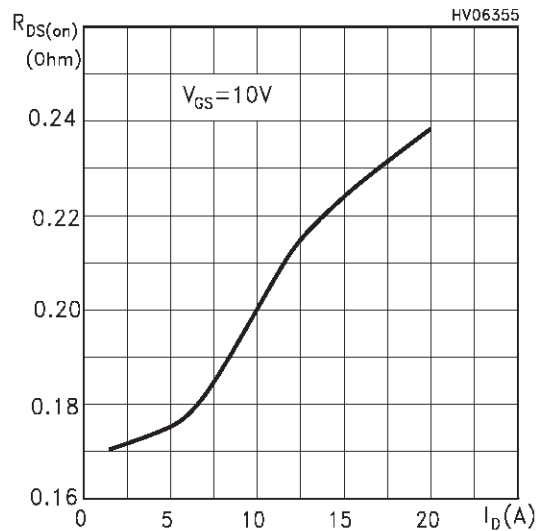
Transfer Characteristics



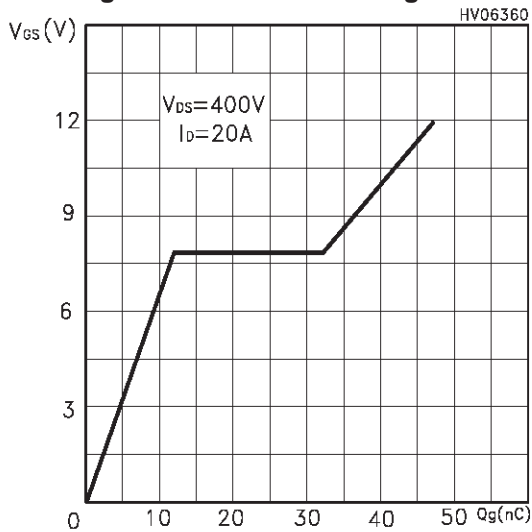
Transconductance



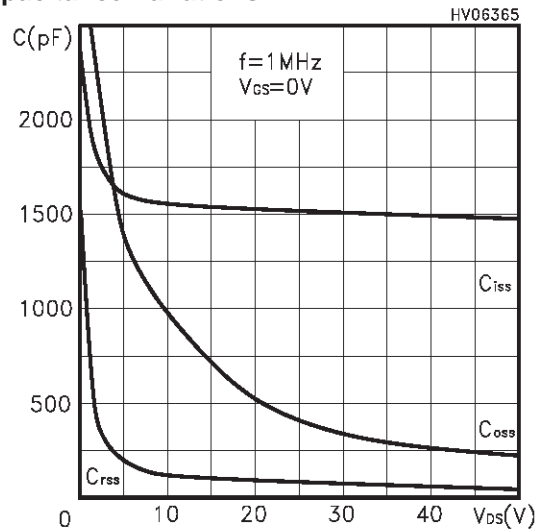
Static Drain-source On Resistance



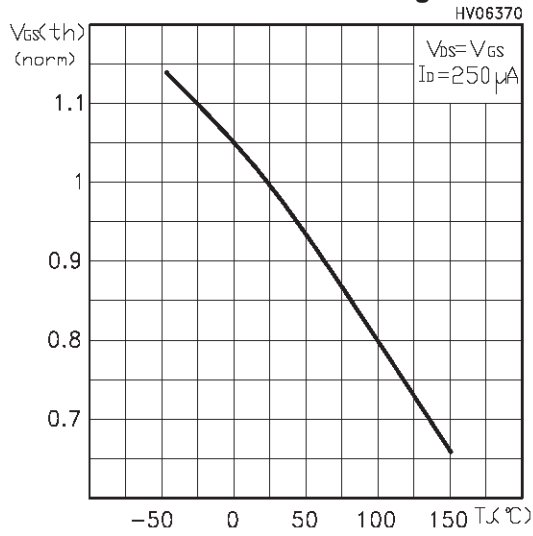
Gate Charge vs Gate-source Voltage



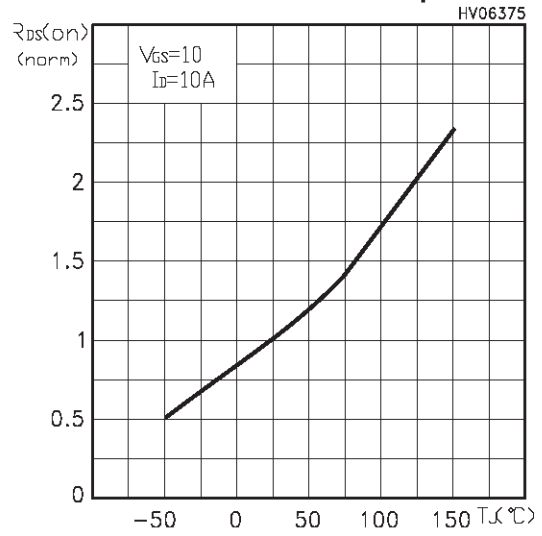
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

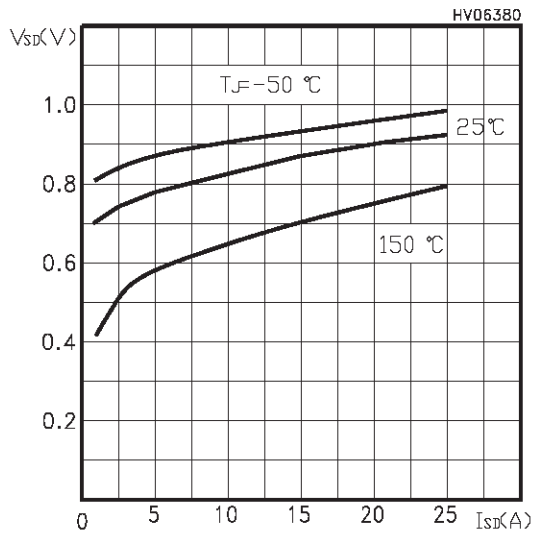


Fig. 1: Unclamped Inductive Load Test Circuit

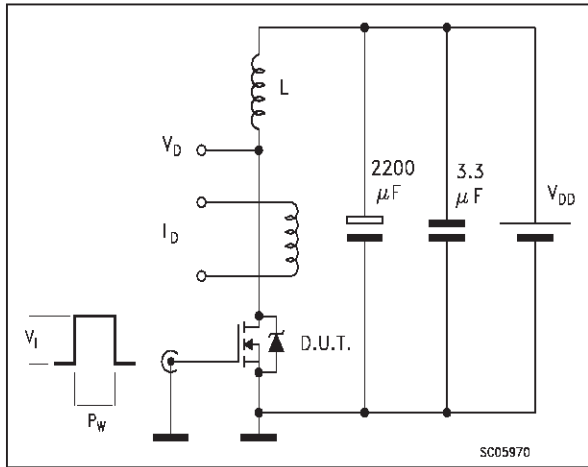


Fig. 2: Unclamped Inductive Waveform

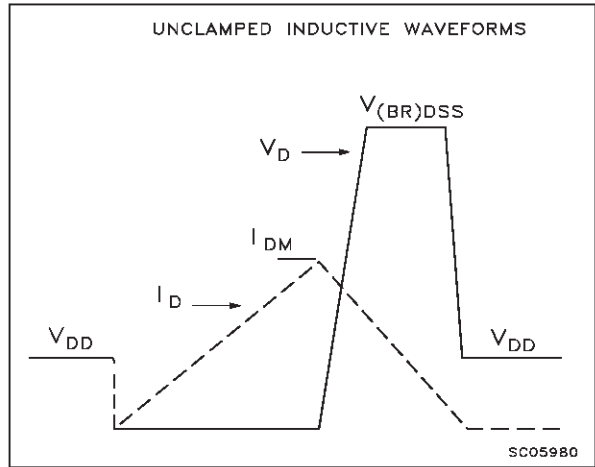


Fig. 3: Switching Times Test Circuit For Resistive Load

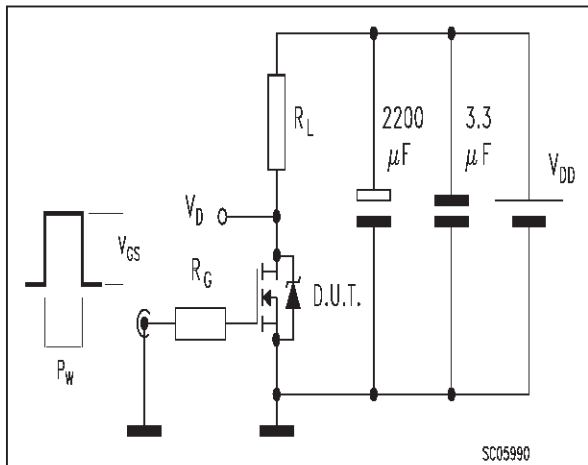


Fig. 4: Gate Charge test Circuit

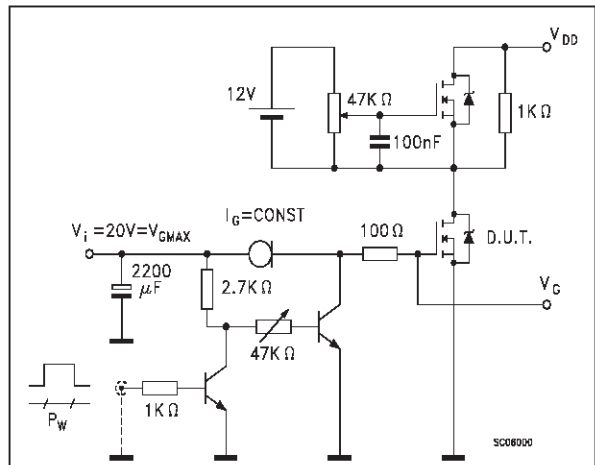
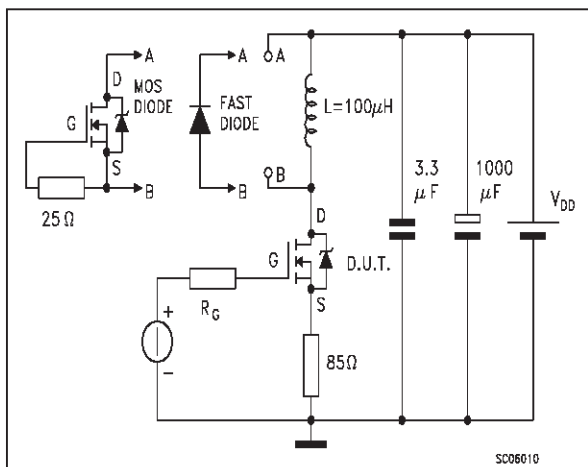
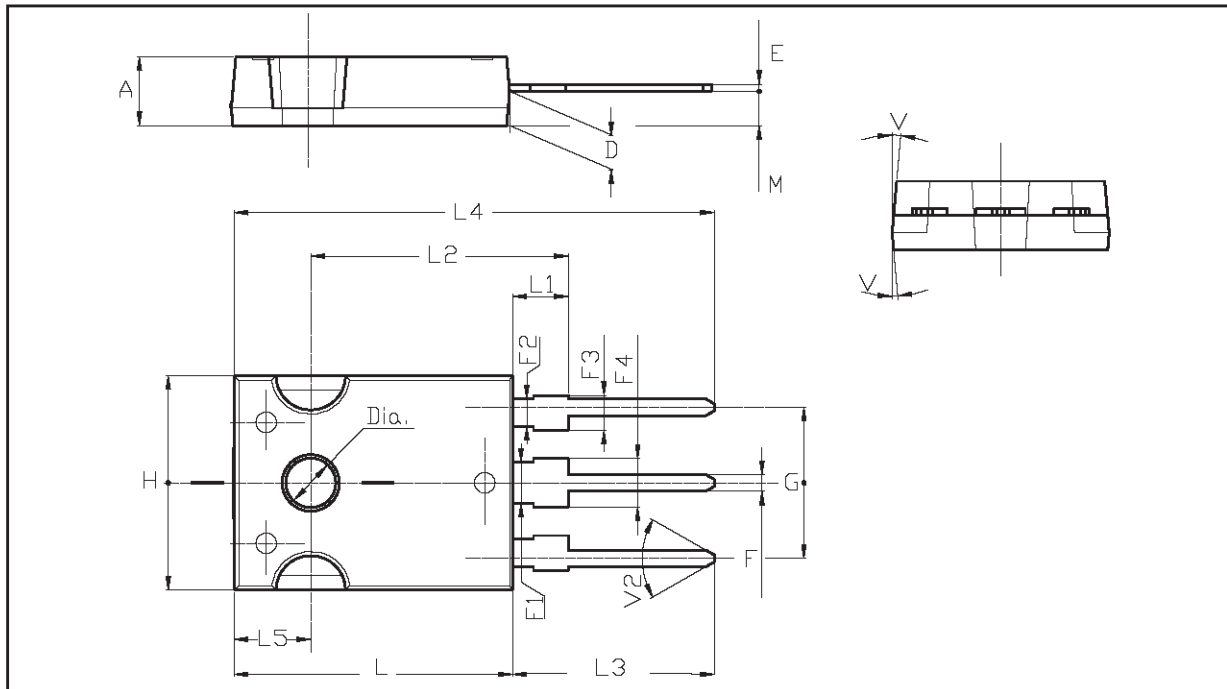


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
D	2.20		2.60	0.08		0.10
E	0.40		0.80	0.015		0.03
F	1		1.40	0.04		0.05
F1		3			0.11	
F2		2			0.07	
F3	2		2.40	0.07		0.09
F4	3		3.40	0.11		0.13
G		10.90			0.43	
H	15.45		15.75	0.60		0.62
L	19.85		20.15	0.78		0.79
L1	3.70		4.30	0.14		0.17
L2		18.50			0.72	
L3	14.20		14.80	0.56		0.58
L4		34.60			1.36	
L5		5.50			0.21	
M	2		3	0.07		0.11
V		5°			5°	
V2		60°			60°	
Dia	3.55		3.65	0.14		0.143



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