



128K x 16 Static RAM

Features

- Low voltage range:
— CY62136V: 2.7V-3.6V
- Ultra-low active, standby power
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power

Functional Description

The CY62136V is a high-performance CMOS static RAM organized as 131,072 words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}$ HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$

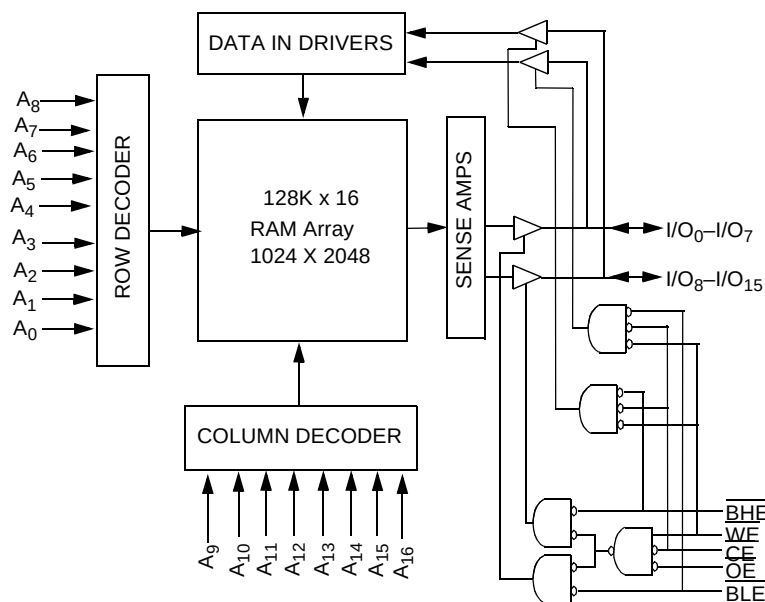
HIGH), outputs are disabled ($\overline{OE}$ HIGH), $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The CY62136V is available in 48-ball FBGA and standard 44-pin TSOP Type II (forward pinout) packaging.

Logic Block Diagram



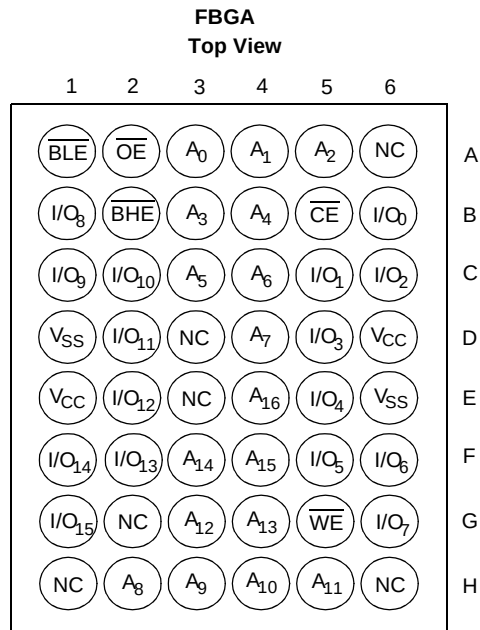
Pin Configurations

TSOP II (Forward)

Top View			
A_4	1	44	A_5
A_3	2	43	A_6
A_2	3	42	A_7
A_1	4	41	$\overline{OE}$
A_0	5	40	$\overline{BHE}$
$\overline{CE}$	6	39	$\overline{BLE}$
I/O_0	7	38	I/O_{15}
I/O_1	8	37	I/O_{14}
I/O_2	9	36	I/O_{13}
I/O_3	10	35	I/O_{12}
V_{CC}	11	34	V_{SS}
V_{SS}	12	33	V_{CC}
I/O_4	13	32	I/O_{11}
I/O_5	14	31	I/O_{10}
I/O_6	15	30	I/O_9
I/O_7	16	29	I/O_8
$\overline{WE}$	17	28	NC
A_{16}	18	27	A_8
A_{15}	19	26	A_9
A_{14}	20	25	A_{10}
A_{13}	21	24	A_{11}
A_{12}	22	23	NC

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Pin Configurations (continued)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature–65°C to +150°C
 Ambient Temperature with
 Power Applied..... –55°C to +125°C
 Supply Voltage to Ground Potential.....–0.5V to +4.6V

DC Voltage Applied to Outputs

in High Z State^[1].....–0.5V to V_{CC} + 0.5V
 DC Input Voltage^[1].....–0.5V to V_{CC} + 0.5V
 Output Current into Outputs (LOW).....20 mA
 Static Discharge Voltage.....>2001V
 (per MIL-STD-883, Method 3015)
 Latch-Up Current.....>200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC}
CY62136V	Industrial	–40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V _{CC} Range			Power	Power Dissipation (Industrial)			
					Operating (I _{CC})		Standby (I _{SB2})	
	V _{CC(min.)}	V _{CC(typ.)} ^[2]	V _{CC(max.)}		Typ. ^[2]	Maximum	Typ. ^[2]	Maximum
CY62136V	2.7V	3.0V	3.6V	LL	7 mA	15 mA	1 µA	15 µA

Notes:

- V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62136V			Unit	
				Min.	Typ. ^[2]	Max.		
V _{OH}	Output HIGH Voltage	I _{OH} = −1.0 mA	V _{CC} = 2.7V	2.4			V	
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 2.7V			0.4	V	
V _{IH}	Input HIGH Voltage		V _{CC} = 3.6V	2.2		V _{CC} + 0.5V	V	
V _{IL}	Input LOW Voltage		V _{CC} = 2.7V	−0.5		0.8	V	
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}		−1	±1	+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		−1	+1	+1	μA	
I _{CC}	V _{CC} Operating Supply Current	I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} , CMOS levels	V _{CC} = 3.6V		7	15	mA	
		I _{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA	
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC}-0.3V$, $V_{IN} \geq V_{CC}-0.3V$ or $V_{IN} \leq 0.3V$, f = f _{MAX}				100	μA	
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC}-0.3V$ $V_{IN} \geq V_{CC}-0.3V$ or $V_{IN} \leq 0.3V$, f = 0	V _{CC} = 3.6V	LL		1	15	μA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)}	6	pF
C _{OUT}	Output Capacitance		8	pF

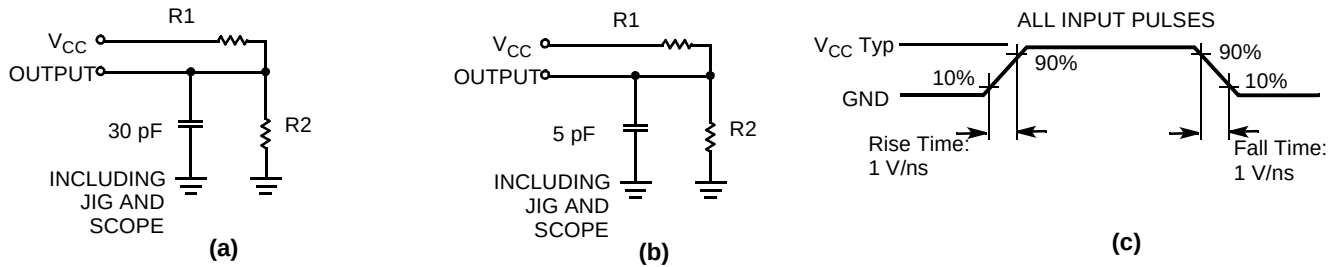
Thermal Resistance

Description	Test Conditions	Symbol	BGA	TSOPII	Unit
Thermal Resistance (Junction to Ambient) ^[3]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ _{JA}	55	60	°C/W
Thermal Resistance (Junction to Case) ^[3]		Θ _{JC}	16	22	°C/W

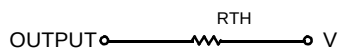
Note:

3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

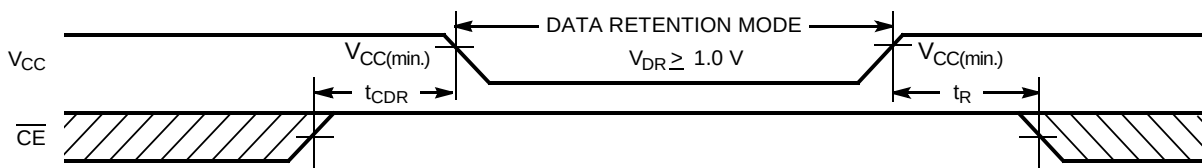


Parameters	3.0V	UNIT
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75V	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[5]		Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.0		3.6	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$ $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed $V_{CC} + 0.3V$	LL		0.5	7.5	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time			0			ns
$t_R^{[4]}$	Operation Recovery Time			70			ns

Data Retention Waveform

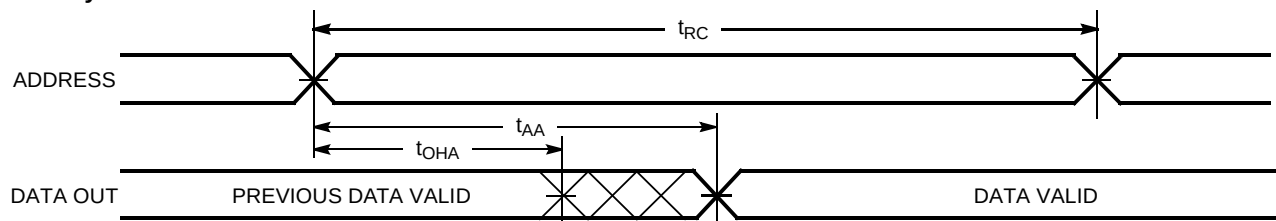


Notes:

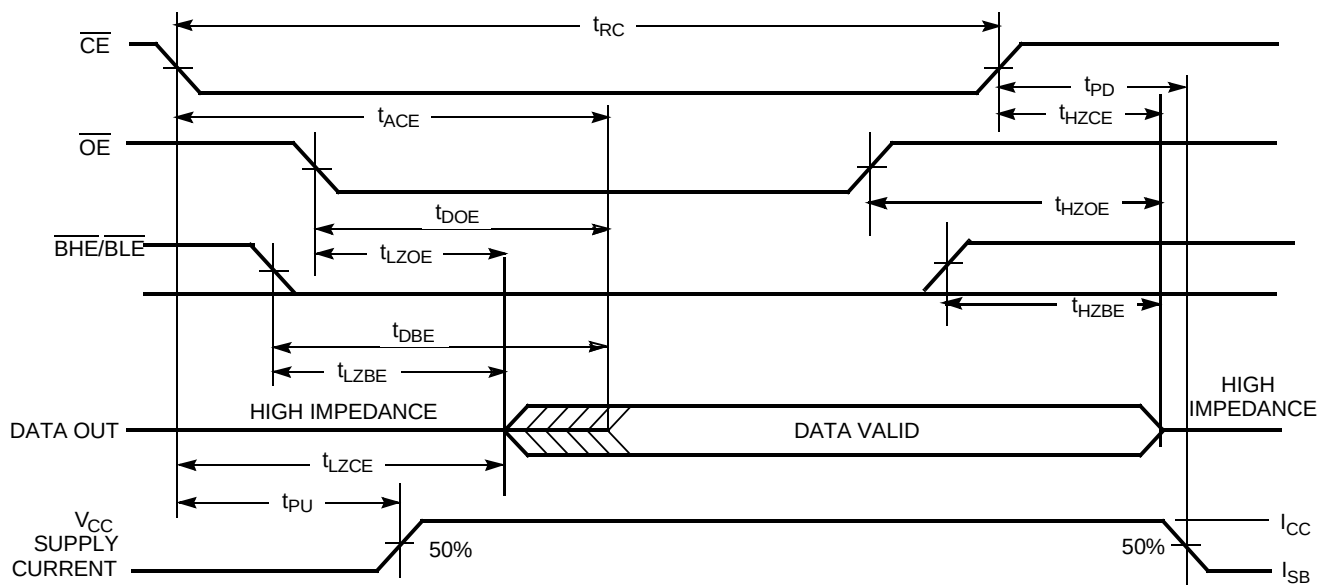
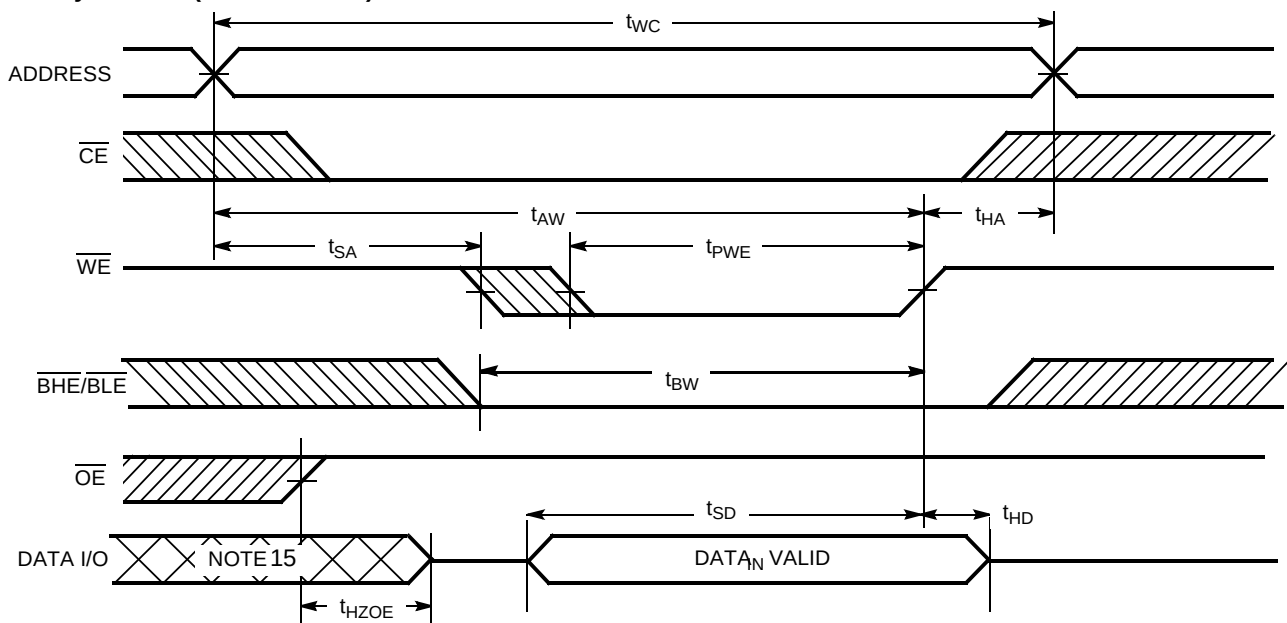
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ ms or stable at $V_{CC(min.)} \geq 100$ ms.
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

Switching Characteristics Over the Operating Range^[5]

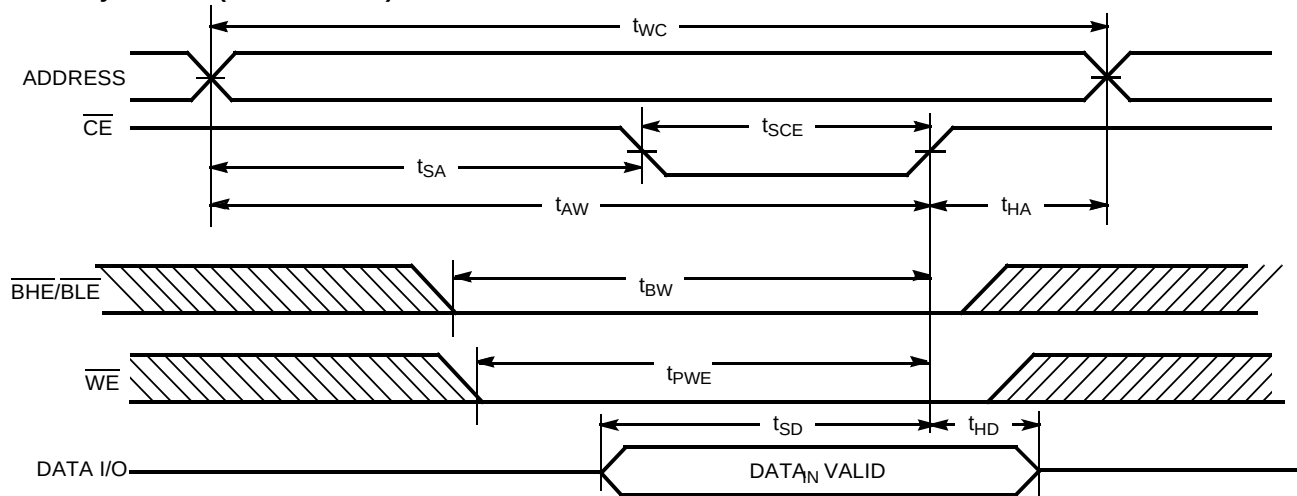
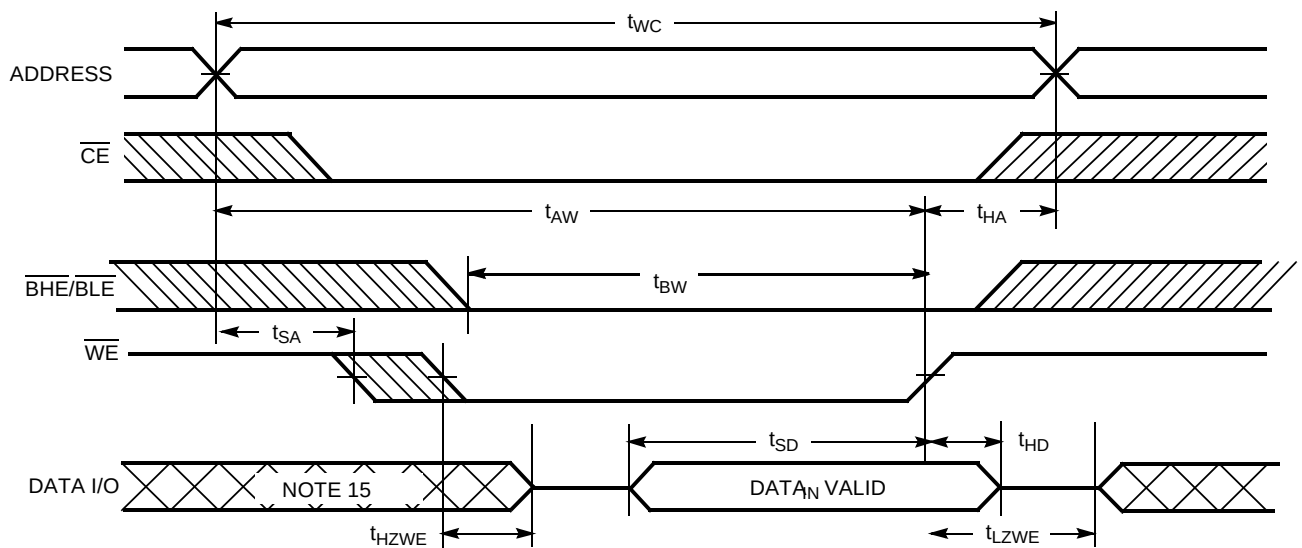
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[6]	5		5		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[6, 7]		25		25	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[6]	10		10		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[6, 7]		25		25	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		55		70	ns
t _{DBE}	$\overline{\text{BLE}}$ / $\overline{\text{BHE}}$ LOW to Data Valid		25		35	ns
t _{LZBE}	$\overline{\text{BLE}}$ / $\overline{\text{BHE}}$ LOW to Low Z ^[6, 7]	5		5		ns
t _{HZBE}	$\overline{\text{BLE}}$ / $\overline{\text{BHE}}$ HIGH to High Z ^[8]		25		25	ns
WRITE CYCLE ^[8, 9]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	40		50		ns
t _{BW}	$\overline{\text{BLE}}$ / $\overline{\text{BHE}}$ LOW to Write End	50		60		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[6, 7]		20		25	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[6]	5		10		ns

Switching Waveforms
Read Cycle No. 1^[10, 11]

Notes:

- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{LZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .
- Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
- $\overline{WE}$ is HIGH for read cycle.

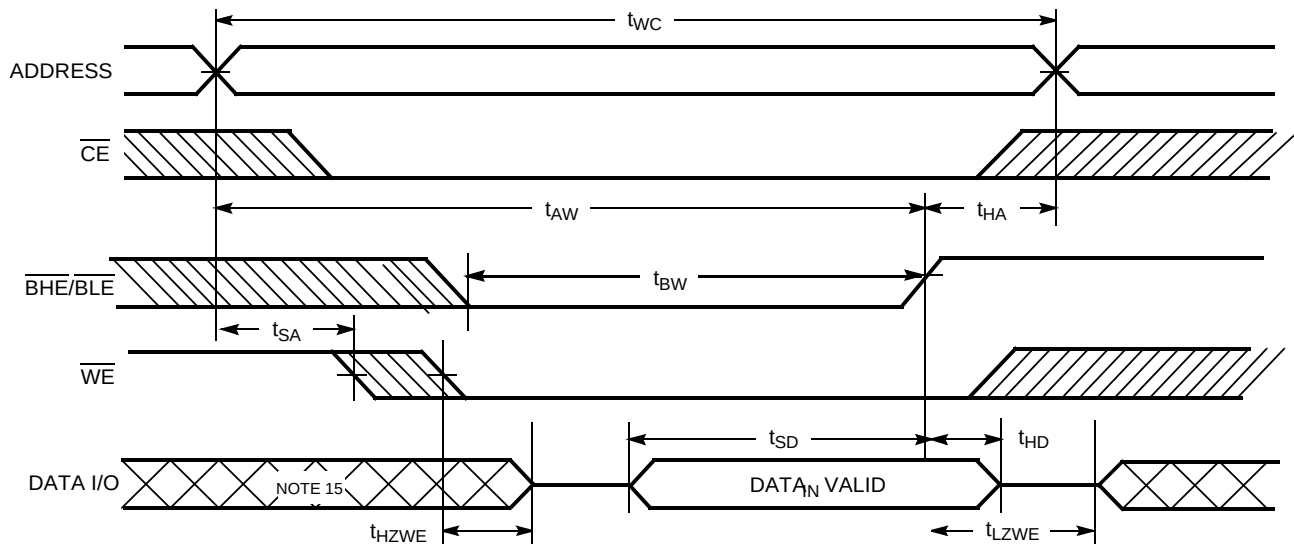
Switching Waveforms (continued)
Read Cycle No. 2 [11, 12]

Write Cycle No. 1 (WE Controlled) [8, 13, 14]

Notes:

12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is high impedance if $OE = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

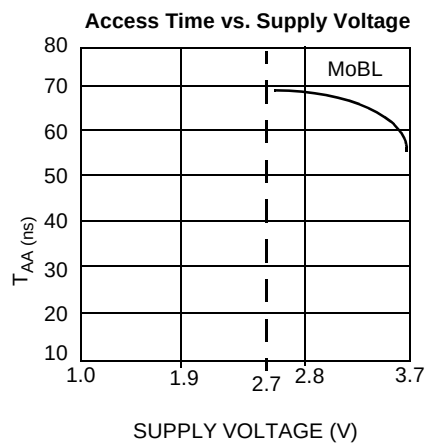
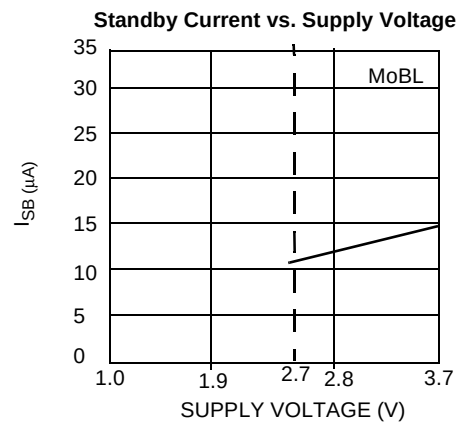
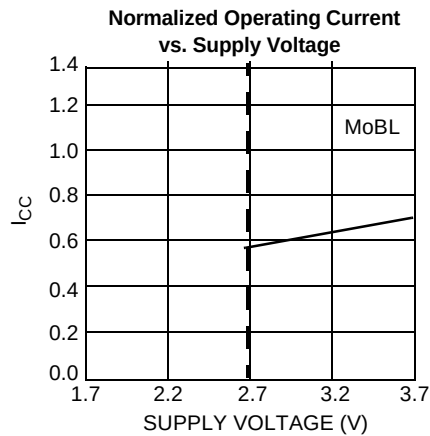
Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[8, 13, 14]

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[9, 14]


Switching Waveforms (continued)

Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[15]



Typical DC and AC Characteristics



Truth Table

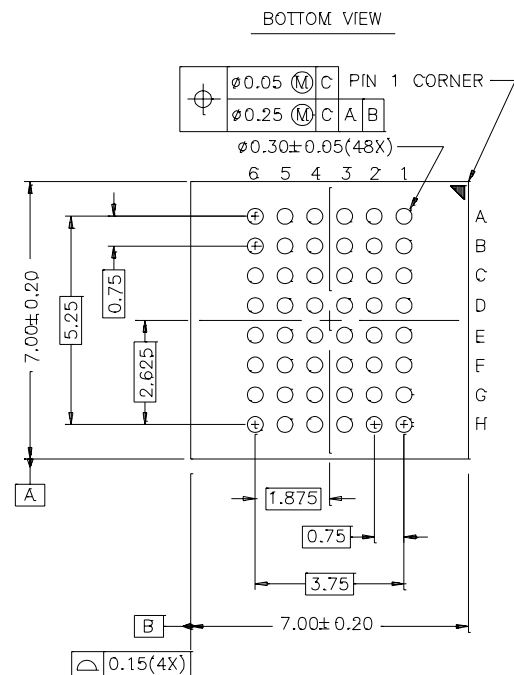
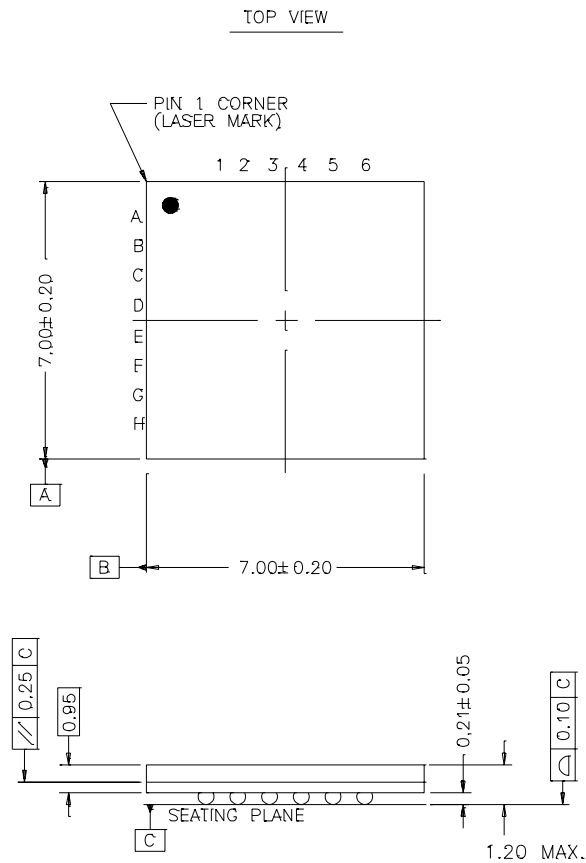
CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	L	H	H	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62136VLL-55ZI	Z44	44-Pin TSOP II	Industrial
	CY62136VLL-55BAI	BA48	48-Ball Fine Pitch BGA	
70	CY62136VLL-70ZI	Z44	44-Pin TSOP II	
	CY62136VLL-70BAI	BA48	48-Ball Fine Pitch BGA	

Package Diagrams

48-Ball (7.00 mm x 7.00 mm) FBGA BA48



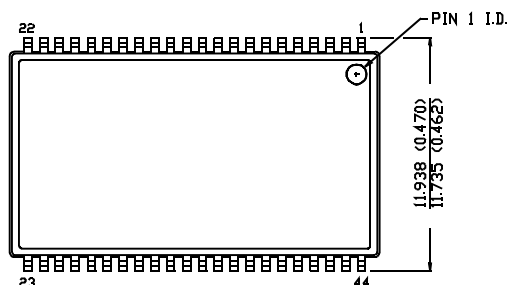
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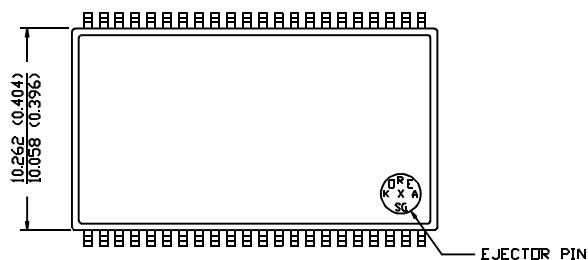
Package Diagrams (continued)

44-Pin TSOP II Z44

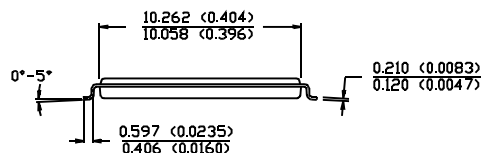
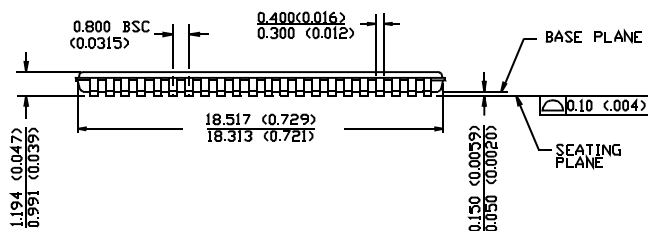
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A



Document Title: CY62136V MoBL™ 128K x 16 Static RAM Document Number: 38-05087				
REV.	ECN NO.	Issue Date	Oreg. of Change	Description of Change
**	107347	05/25/01	SZV	Change from Spec #: 38-00728 to 38-05087