



CYPRESS

PRELIMINARY

CY7C1345G

4-Mbit (128K x 36) Flow-Through Sync SRAM

Features

- 128K X 36 common I/O
- 3.3V -5% and +10% core power supply (V_{DD})
- 2.5V or 3.3V I/O supply (V_{DDQ})
- Fast clock-to-output times
 - 6.5 ns (133-MHz version)
 - 7.5 ns (117-MHz version)
 - 8.0 ns (100-MHz version)
- Provide high-performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Lead-Free 100-pin TQFP and 119-ball BGA packages
- “ZZ” Sleep Mode option

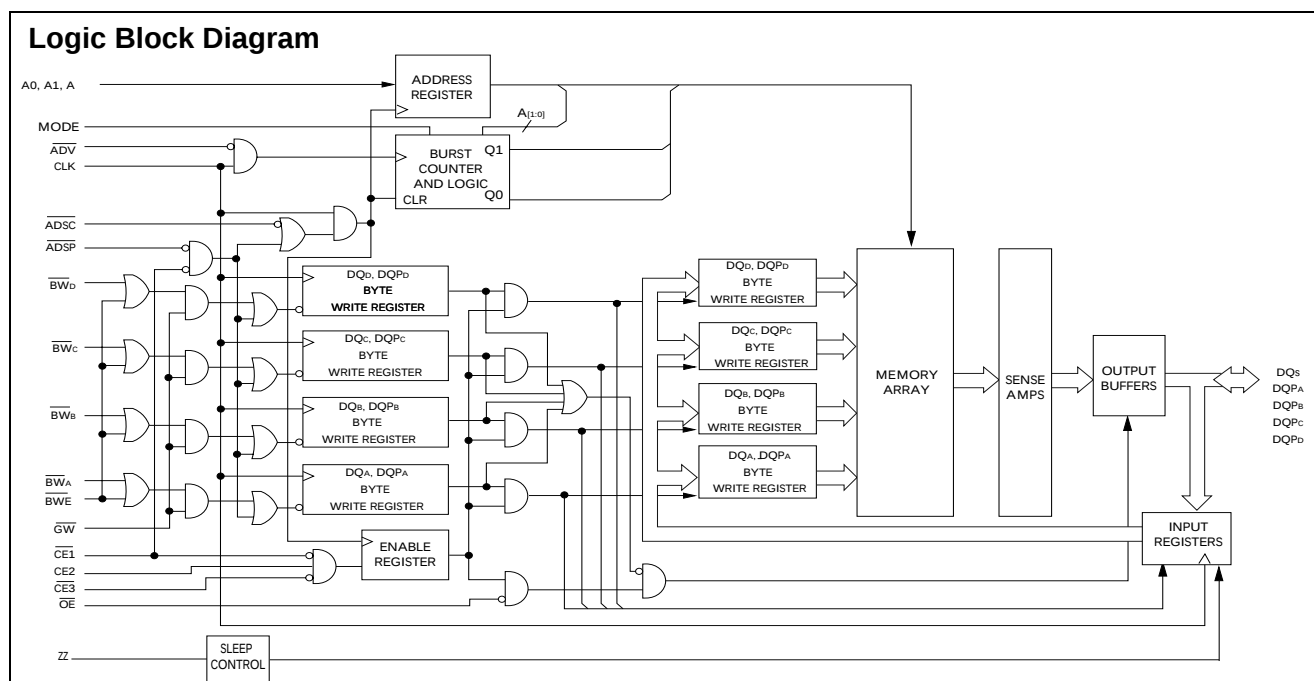
Functional Description^[1]

The CY7C1345G is a 131,072 x 36 synchronous cache RAM designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133-MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE}_1$), depth-expansion Chip Enables ($\overline{CE}_2$ and $\overline{CE}_3$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW}_X$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

The CY7C1345G allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe ($\overline{ADSP}$) or the cache Controller Address Strobe ($\overline{ADSC}$) inputs.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

The CY7C1345G operates from a +3.3V core power supply while all outputs may operate with either a +2.5 or +3.3V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.



Note:

1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

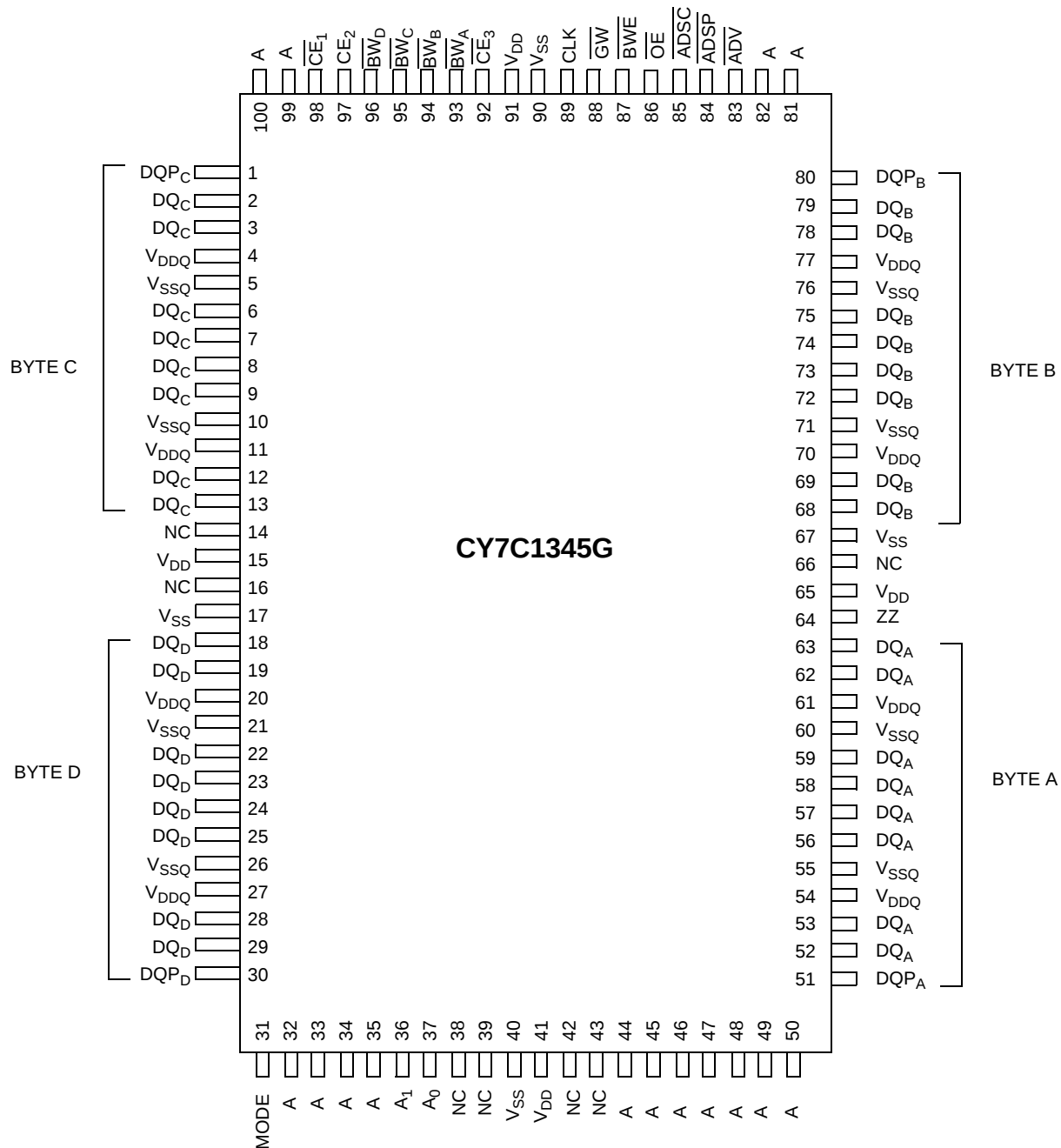
Selection Guide

	133 MHz	117 MHz	100 MHz	Unit
Maximum Access Time	6.5	7.5	8.0	ns
Maximum Operating Current	225	220	205	mA
Maximum Standby Current	40	40	40	mA

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

Pin Configurations

100-Pin TQFP



Pin Configurations (continued)

119-Ball BGA

	1	2	3	4	5	6	7
A	V _{DDQ}	A	A	$\overline{\text{ADSP}}$	A	A	V _{DDQ}
B	NC	CE ₂	A	$\overline{\text{ADSC}}$	A	$\overline{\text{CE}}_3$	NC
C	NC	A	A	V _{DD}	A	A	NC
D	DQ _C	DQP _C	V _{SS}	NC	V _{SS}	DQP _B	DQ _B
E	DQ _C	DQ _C	V _{SS}	$\overline{\text{CE}}_1$	V _{SS}	DQ _B	DQ _B
F	V _{DDQ}	DQ _C	V _{SS}	$\overline{\text{OE}}$	V _{SS}	DQ _B	V _{DDQ}
G	DQ _C	DQ _C	$\overline{\text{BW}}_C$	$\overline{\text{ADV}}$	$\overline{\text{BW}}_B$	DQ _B	DQ _B
H	DQ _C	DQ _C	V _{SS}	$\overline{\text{GW}}$	V _{SS}	DQ _B	DQ _B
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	DQ _D	DQ _D	V _{SS}	CLK	V _{SS}	DQ _A	DQ _A
L	DQ _D	DQ _D	$\overline{\text{BW}}_D$	NC	$\overline{\text{BW}}_A$	DQ _A	DQ _A
M	V _{DDQ}	DQ _D	V _{SS}	$\overline{\text{BWE}}$	V _{SS}	DQ _A	V _{DDQ}
N	DQ _D	DQ _D	V _{SS}	A1	V _{SS}	DQ _A	DQ _A
P	DQ _D	DQP _D	V _{SS}	A0	V _{SS}	DQP _A	DQ _A
R	NC	A	MODE	V _{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V _{DDQ}	NC	NC	NC	NC	NC	V _{DDQ}

Pin Definitions

Name	I/O	Description
A0, A1, A	Input-Synchronous	Address Inputs used to select one of the 128K address locations. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE ₁ , CE ₂ , and CE ₃ are sampled active. A _[1:0] feed the 2-bit counter.
$\overline{\text{BW}}_A$, $\overline{\text{BW}}_B$ $\overline{\text{BW}}_C$, $\overline{\text{BW}}_D$	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with BWE to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{\text{GW}}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{\text{BW}}_{[A:D]}$ and BWE).
$\overline{\text{BWE}}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{\text{CE}}_1$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE ₂ and CE ₃ to select/deselect the device. ADSP is ignored if $\overline{\text{CE}}_1$ is HIGH. $\overline{\text{CE}}_1$ is sampled only when a new external address is loaded.
CE ₂	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with CE ₁ and CE ₃ to select/deselect the device. CE ₂ is sampled only when a new external address is loaded.
$\overline{\text{CE}}_3$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE ₁ and CE ₂ to select/deselect the device. CE ₃ is sampled only when a new external address is loaded.
$\overline{\text{OE}}$	Input-Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{\text{ADV}}$	Input-Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.

Pin Definitions (continued)

Name	I/O	Description
ADSP	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK, active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when $\overline{CE}_1$ is deasserted HIGH.
ADSC	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK, active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	Input-Asynchronous	ZZ “sleep” Input, active HIGH. When asserted HIGH places the device in a non-time-critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs DQP _A , DQP _B , DQP _C , DQP _D	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP _[A:D] are placed in a tri-state condition.
V _{DD}	Power Supply	Power supply inputs to the core of the device.
V _{SS}	Ground	Ground for the core of the device.
V _{DDQ}	I/O Power Supply	Power supply for the I/O circuitry.
V _{SSQ}	I/O Ground	Ground for the I/O circuitry.
MODE	Input-Static	Selects Burst Order. When tied to GND selects linear burst sequence. When tied to V _{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
NC		No Connects. Not Internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{C0}) is 6.5 ns (133-MHz device).

The CY7C1345G supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium® and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW_[A:D]) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. ADSP is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ are all asserted active, and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data will be available at the data outputs a maximum to t_{CDV} after clock rise. ADSP is ignored if $\overline{CE}_1$ is HIGH.

Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ are all asserted active, and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and BW_x) are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the appropriate data will be latched and written into the device. Byte writes are allowed. During byte writes, BW_A controls DQ_A and BW_B controls DQ_B, BW_C controls DQ_C, and BW_D controls DQ_D. All I/Os are tri-stated during a byte write. Since this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ are all asserted active, (2) ADSC is asserted LOW, (3) $\overline{ADSP}$ is deasserted HIGH, and (4) the write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_x$) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to $DQ_{[D:A]}$ will be written into the specified address location. Byte writes are allowed. During byte writes, $\overline{BW}_A$ controls DQ_A , $\overline{BW}_B$ controls DQ_B , $\overline{BW}_C$ controls DQ_C , and $\overline{BW}_D$ controls DQ_D . All I/Os are tri-stated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1345G provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE will select an interleaved burst order. Leaving MODE unconnected will cause the device to default to a interleaved burst sequence.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A_1, A_0	Second Address A_1, A_0	Third Address A_1, A_0	Fourth Address A_1, A_0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A_1, A_0	Second Address A_1, A_0	Third Address A_1, A_0	Fourth Address A_1, A_0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. $\overline{CE}$ s, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		40	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ Active to snooze current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit snooze current	This parameter is sampled	0		ns

Truth Table^[2, 3, 4, 5, 6]

Cycle Description	Address Used	$\overline{CE}_1$	CE_2	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	tri-state
Deselected Cycle, Power-down	None	L	L	X	L	L	X	X	X	X	L-H	tri-state
Deselected Cycle, Power-down	None	L	X	H	L	L	X	X	X	X	L-H	tri-state
Deselected Cycle, Power-down	None	L	L	X	L	H	L	X	X	X	L-H	tri-state
Deselected Cycle, Power-down	None	X	X	X	L	H	L	X	X	X	L-H	tri-state
Snooze Mode, Power-down	None	X	X	X	H	X	X	X	X	X	X	tri-state
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	tri-state
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	tri-state
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	tri-state
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	tri-state
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	tri-state
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	tri-state
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes:

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE} = 1$ when any one or more Byte Write enable signals ($\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$) and $\overline{BWE} = L$ or $\overline{GW} = L$. $\overline{WRITE} = H$ when all Byte write enable signals ($\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$), $\overline{BWE}$, $\overline{GW} = H$.
- The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
- The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_{[A:D]}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
- $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Partial Truth Table for Read/Write^[2, 7]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte (A, DQP _A)	H	L	H	H	H	L
Write Byte (B, DQP _B)	H	L	H	H	L	H
Write Bytes (B, A, DQP _A , DQP _B)	H	L	H	H	L	L
Write Byte (C, DQP _C)	H	L	H	L	H	H
Write Bytes (C, A, DQP _C , DQP _A)	H	L	H	L	H	L
Write Bytes (C, B, DQP _C , DQP _B)	H	L	H	L	L	H
Write Bytes (C, B, A, DQP _C , DQP _B , DQP _A)	H	L	H	L	L	L
Write Byte (D, DQP _D)	H	L	L	H	H	H
Write Bytes (D, A, DQP _D , DQP _A)	H	L	L	H	H	L
Write Bytes (D, B, DQP _D , DQP _B)	H	L	L	H	L	H
Write Bytes (D, B, A, DQP _D , DQP _B , DQP _A)	H	L	L	H	L	L
Write Bytes (D, B, DQP _D , DQP _B)	H	L	L	L	H	H
Write Bytes (D, B, A, DQP _D , DQP _C , DQP _A)	H	L	L	L	H	L
Write Bytes (D, C, A, DQP _D , DQP _B , DQP _A)	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Note:

7. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_x$ is valid. Appropriate write will be done based on which byte write is active.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage on V_{DD} Relative to GND -0.5V to +4.6V

DC Voltage Applied to Outputs
in tri-state -0.5V to $V_{DDQ} + 0.5V$

DC Input Voltage -0.5V to $V_{DD} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current >200 mA

Operating Range

Range	Ambient Temperature ¹	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V -5%/+10%	2.5V -5% to V_{DD}
Industrial	-40°C to +85°C		

Electrical Characteristics Over the Operating Range [8, 9]

Parameter	Description	Test Conditions	CY7C1345F		Unit
			Min.	Max.	
V_{DD}	Power Supply Voltage		3.135	3.6	V
V_{DDQ}	I/O Supply Voltage		2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	$V_{DDQ} = 3.3V$, $V_{DD} = \text{Min.}$, $I_{OH} = -4.0 \text{ mA}$	2.4		V
		$V_{DDQ} = 2.5V$, $V_{DD} = \text{Min.}$, $I_{OH} = -1.0 \text{ mA}$	2.0		V
V_{OL}	Output LOW Voltage	$V_{DDQ} = 3.3V$, $V_{DD} = \text{Min.}$, $I_{OL} = 8.0 \text{ mA}$		0.4	V
		$V_{DDQ} = 2.5V$, $V_{DD} = \text{Min.}$, $I_{OL} = 1.0 \text{ mA}$		0.4	V
V_{IH}	Input HIGH Voltage	$V_{DDQ} = 3.3V$	2.0	$V_{DD} + 0.3V$	V
		$V_{DDQ} = 2.5V$	1.7	$V_{DD} + 0.3V$	V
V_{IL}	Input LOW Voltage ^[8]	$V_{DDQ} = 3.3V$	-0.3	0.8	V
		$V_{DDQ} = 2.5V$	-0.3	0.7	V
I_X	Input Load Current (except ZZ and MODE)	$GND \leq V_I \leq V_{DDQ}$	-5	5	μA
	Input Current of MODE	Input = V_{SS}	-30		μA
		Input = V_{DD}		5	μA
	Input Current of ZZ	Input = V_{SS}	-5		μA
		Input = V_{DD}		30	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{DD}$, Output Disabled	-5	5	μA
I_{DD}	V_{DD} Operating Supply Current	$V_{DD} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{CYC}$	7.5-ns cycle, 133 MHz	225	mA
			8.0-ns cycle, 117 MHz	220	mA
			10-ns cycle, 100 MHz	205	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$, inputs switching	7.5-ns cycle, 133 MHz	90	mA
			8.0-ns cycle, 117 MHz	85	mA
			10-ns cycle, 100 MHz	80	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{DD} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$, inputs static	All speeds	40	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{DDQ} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = f_{MAX}$, inputs switching	7.5-ns cycle, 133 MHz	75	mA
			8.0-ns cycle, 117 MHz	70	mA
			10-ns cycle, 100 MHz	65	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{DD} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$, inputs static	All speeds	45	mA

Shaded areas contain advance information.

Notes:

8. Overshoot: $V_{IH}(AC) < V_{DD} + 1.5V$ (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2V$ (Pulse width less than $t_{CYC}/2$).

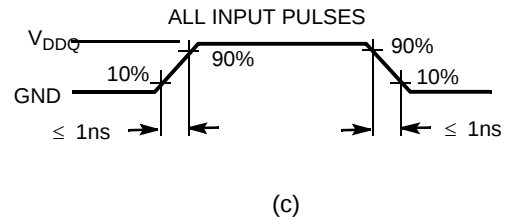
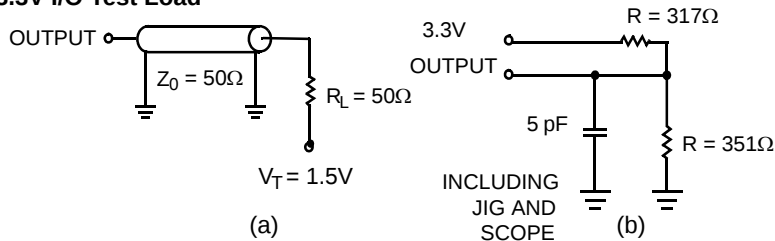
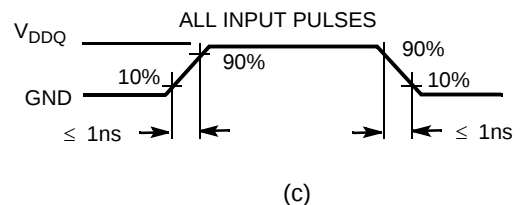
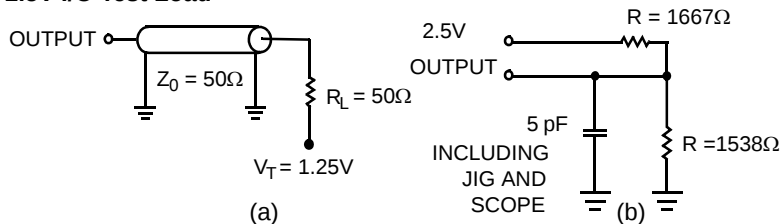
9. $T_{Power-up}$: Assumes a linear ramp from 0v to $V_{DD}(\text{min.})$ within 200ms. During this time $V_{IH} \leq V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

Thermal Resistance^[10]

Parameter	Description	Test Conditions	TQFP Package	BGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	TBD	°C/W

Capacitance^[10]

Parameter	Description	Test Conditions	TQFP Package	BGA Package	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{V}$, $V_{DDQ} = 3.3\text{V}$	5	5	pF
C_{CLK}	Clock Input Capacitance		5	5	pF
$C_{I/O}$	Input/Output Capacitance		5	7	pF

AC Test Loads and Waveforms
3.3V I/O Test Load

2.5V I/O Test Load

Switching Characteristics Over the Operating Range^[15, 16]

Parameter	Description	133 MHz		117 MHz		100 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{POWER}	$V_{DD}(\text{Typical})$ to the first Access ^[11]	1		1		1		ms
Clock								
t_{CYC}	Clock Cycle Time	7.5		8.5		10		ns
t_{CH}	Clock HIGH	2.5		3.0		4.0		ns
t_{CL}	Clock LOW	2.5		3.0		4.0		ns
Output Times								
t_{CDV}	Data Output Valid After CLK Rise		6.5		7.5		8.0	ns
t_{DOH}	Data Output Hold After CLK Rise	2.0		2.0		2.0		ns
t_{CLZ}	Clock to Low-Z ^[12, 13, 14]	0		0		0		ns

Notes:

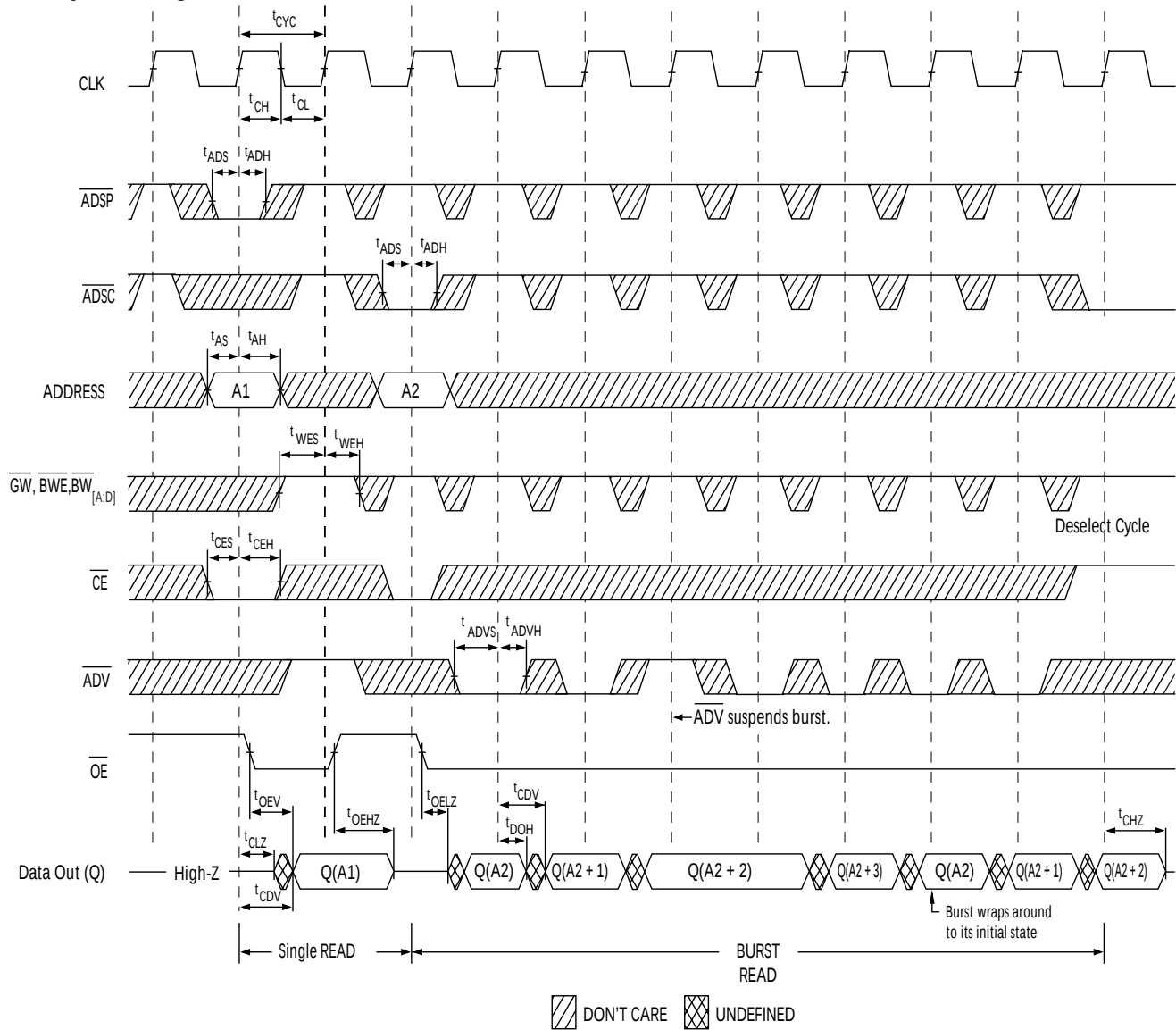
- Tested initially and after any design or process change that may affect these parameters.
- This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD}(\text{minimum})$ initially before a read or write operation can be initiated.
- t_{CHZ} , t_{CLZ} , t_{OELZ} , and t_{OEZH} are specified with AC test conditions shown in (b) of AC Test Loads. Transition is measured $\pm 200\text{ mV}$ from steady-state voltage.
- At any given voltage and temperature, t_{OEZH} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
- This parameter is sampled and not 100% tested.
- Timing reference level is 1.5V when $V_{DDQ} = 3.3\text{V}$ and is 1.25V when $V_{DDQ} = 2.5\text{V}$.
- Test conditions shown in (a) of AC Test Loads unless otherwise noted.

Switching Characteristics Over the Operating Range (continued)^[15, 16]

Parameter	Description	133 MHz		117 MHz		100 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CHZ}	Clock to High-Z ^[12, 13, 14]		3.5		3.5		3.5	ns
t _{OE$\overline{V}$}	OE LOW to Output Valid		3.5		3.5		3.5	ns
t _{OE$\overline{LZ}$}	OE LOW to Output Low-Z ^[12, 13, 14]	0		0		0		ns
t _{OE$\overline{HZ}$}	OE HIGH to Output High-Z ^[12, 13, 14]		3.5		3.5		3.5	ns
Set-up Times								
t _{AS}	Address Set-up Before CLK Rise	1.5		2.0		2.0		ns
t _{ADS}	ADSP, ADSC Set-up Before CLK Rise	1.5		2.0		2.0		ns
t _{ADVS}	ADV Set-up Before CLK Rise	1.5		2.0		2.0		ns
t _{WES}	GW, BWE, BW _x Set-up Before CLK Rise	1.5		2.0		2.0		ns
t _{DS}	Data Input Set-up Before CLK Rise	1.5		2.0		2.0		ns
t _{CES}	Chip Enable Set-up	1.5		2.0		2.0		ns
Hold Times								
t _{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t _{ADH}	ADSP, ADSC Hold After CLK Rise	0.5		0.5		0.5		ns
t _{WEH}	GW, BWE, BW _x Hold After CLK Rise	0.5		0.5		0.5		ns
t _{ADVH}	ADV Hold After CLK Rise	0.5		0.5		0.5		ns
t _{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t _{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		0.5		ns

Timing Diagrams

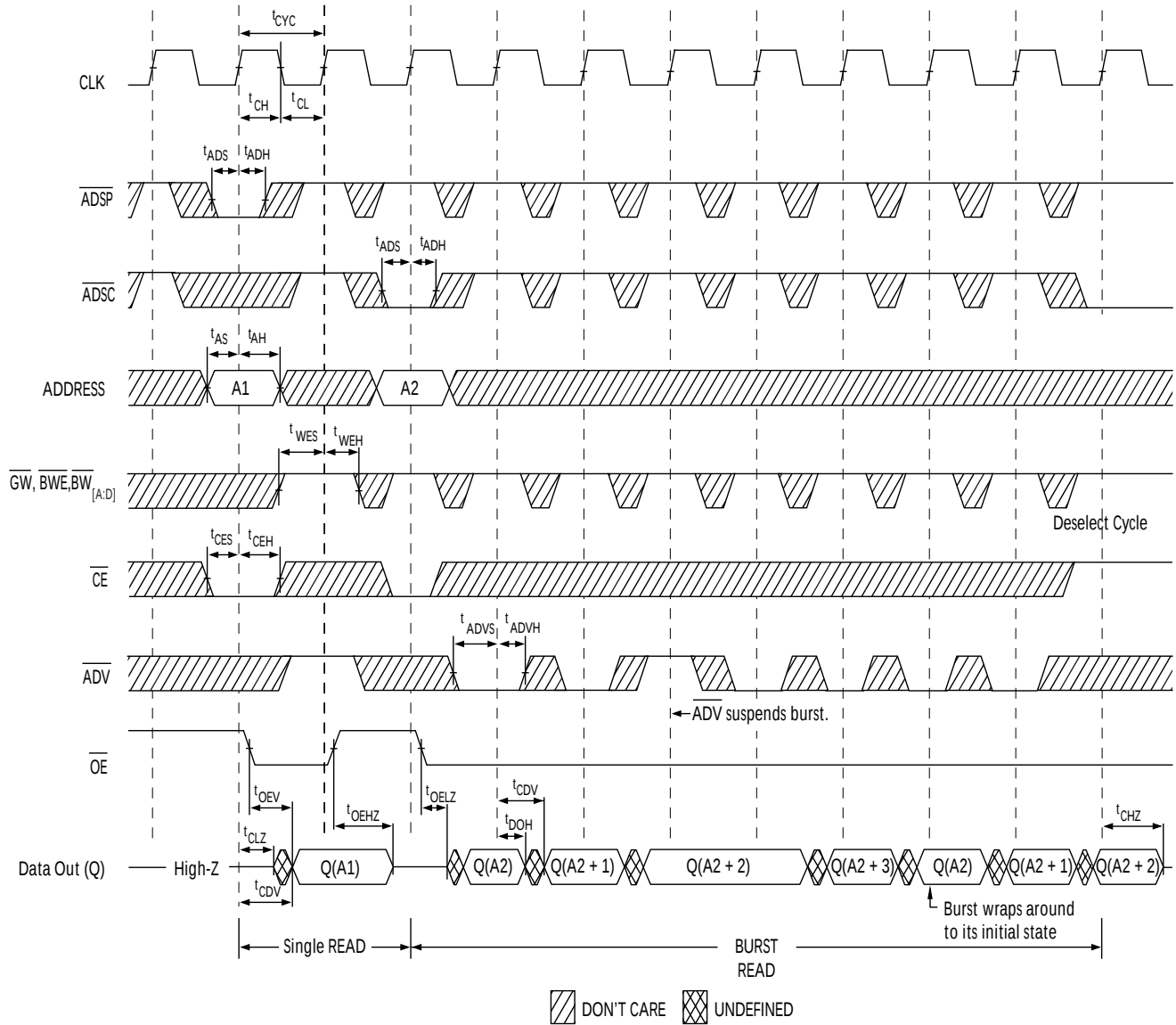
Read Cycle Timing^[17]

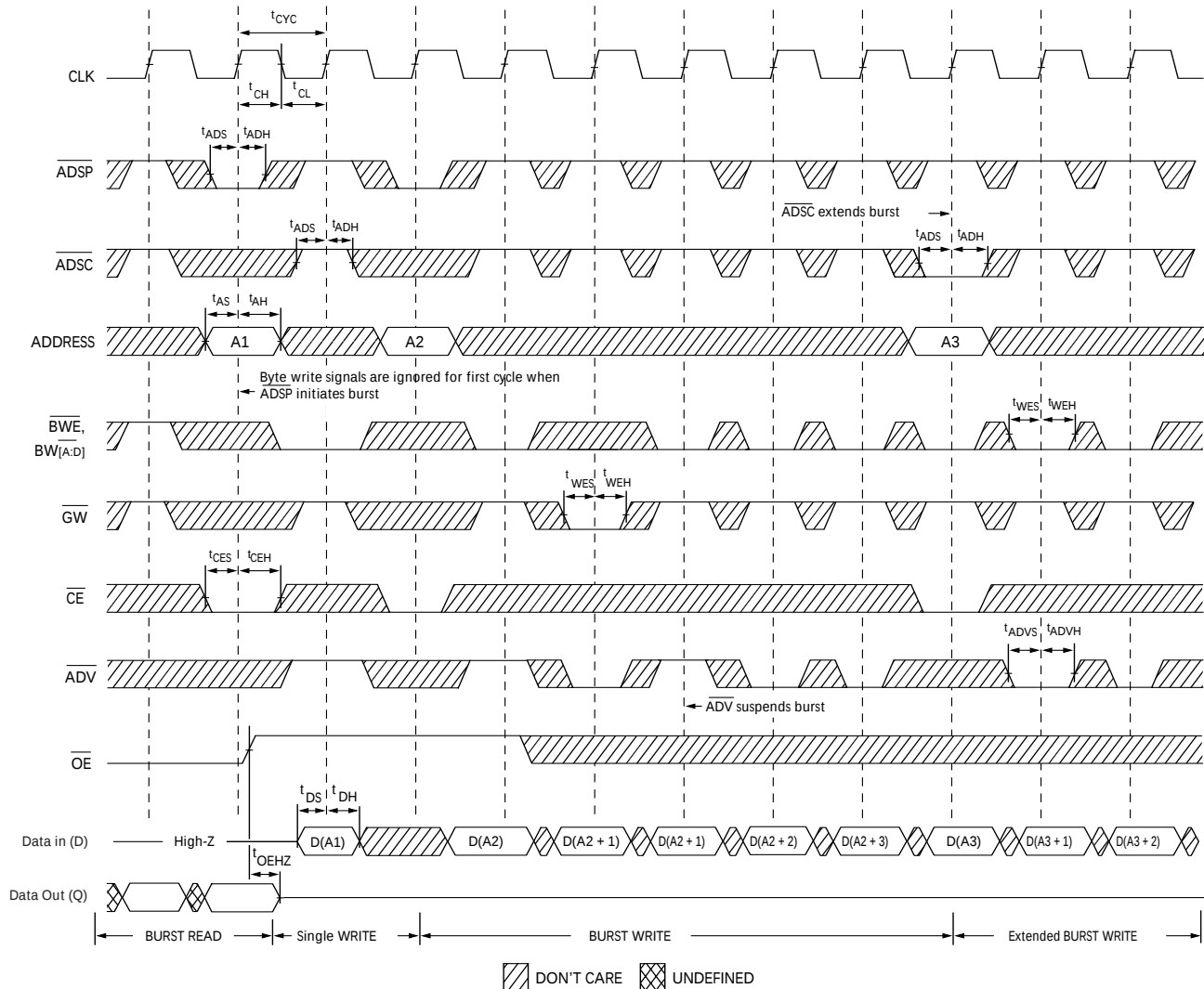


Notes:

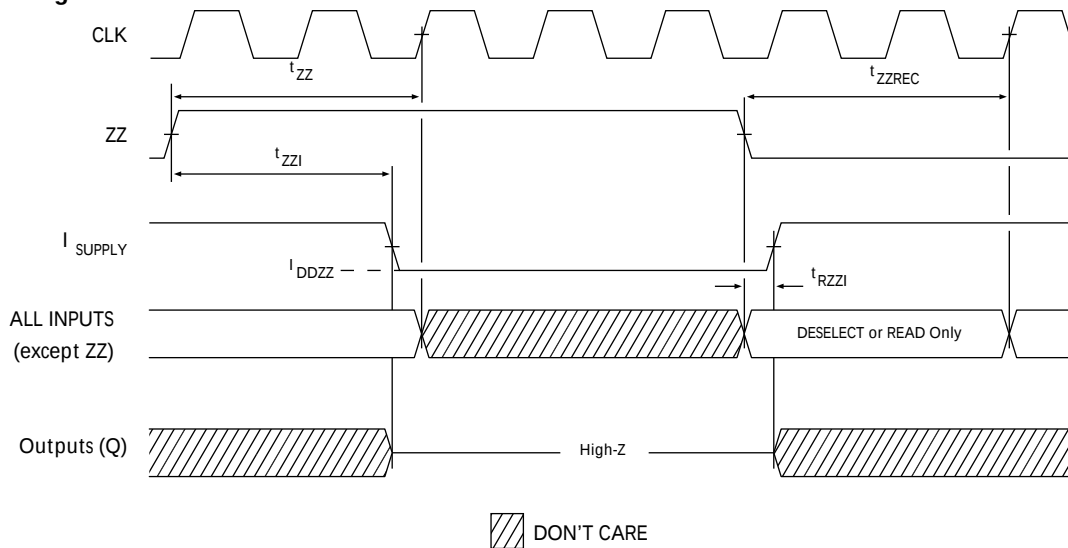
17. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

18. Full width write can be initiated by either GW LOW; or by GW HIGH, BWE LOW and $\overline{BW}_x$ LOW.

Timing Diagrams (continued)
Write Cycle Timing^[17, 18]


Timing Diagrams (continued)
Read/Write Timing^[17, 19, 20]

Notes:

19. The data bus (Q) remains in high-Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
 20. GW is HIGH.

Timing Diagrams (continued)
ZZ Mode Timing [21, 22]

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CY7C1345G-133AXC	A101	Lead-free 100-Lead Thin Quad Flat Pack (14 x 20 x 1.4mm)	Commercial
	CY7C1345G-133BGC	BG119	119-Ball PBGA (14 x 22 x 2.4mm)	
	CY7C1345G-133BGXC	BG119	Lead-free 119-Ball PBGA (14 x 22 x 2.4mm)	
	CY7C1345G-133AXI	A101	Lead-free 100-Lead Thin Quad Flat Pack (14 x 20 x 1.4mm)	Industrial
	CY7C1345G-133BGI	BG119	119-Ball PBGA (14 x 22 x 2.4mm)	
	CY7C1345G-133BGXI	BG119	Lead-free 119-Ball PBGA (14 x 22 x 2.4mm)	
117	CY7C1345G-117AXC	A101	Lead-free 100-Lead Thin Quad Flat Pack (14 x 20 x 1.4mm)	Commercial
	CY7C1345G-117BGC	BG119	119-Ball PBGA (14 x 22 x 2.4mm)	
	CY7C1345G-117BGXC	BG119	Lead-free 119-Ball PBGA (14 x 22 x 2.4mm)	
	CY7C1345G-117AXI	A101	Lead-free 100-Lead Thin Quad Flat Pack (14 x 20 x 1.4mm)	Industrial
	CY7C1345G-117BGI	BG119	119-Ball PBGA (14 x 22 x 2.4mm)	
	CY7C1345G-117BGXI	BG119	Lead-free 119-Ball PBGA (14 x 22 x 2.4mm)	
100	CY7C1345G-100AXC	A101	Lead-free 100-Lead Thin Quad Flat Pack (14 x 20 x 1.4mm)	Commercial
	CY7C1345G-100BGC	BG119	119-Ball PBGA (14 x 22 x 2.4mm)	
	CY7C1345G-100BGXC	BG119	Lead-free 119-Ball PBGA (14 x 22 x 2.4mm)	
	CY7C1345G-100AXI	A101	Lead-free 100-Lead Thin Quad Flat Pack (14 x 20 x 1.4mm)	Industrial
	CY7C1345G-100BGI	BG119	119-Ball PBGA (14 x 22 x 2.4mm)	
	CY7C1345G-100BGXI	BG119	Lead-free 119-Ball PBGA (14 x 22 x 2.4mm)	

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts. Lead-Free BG pkg will be available in 2005.

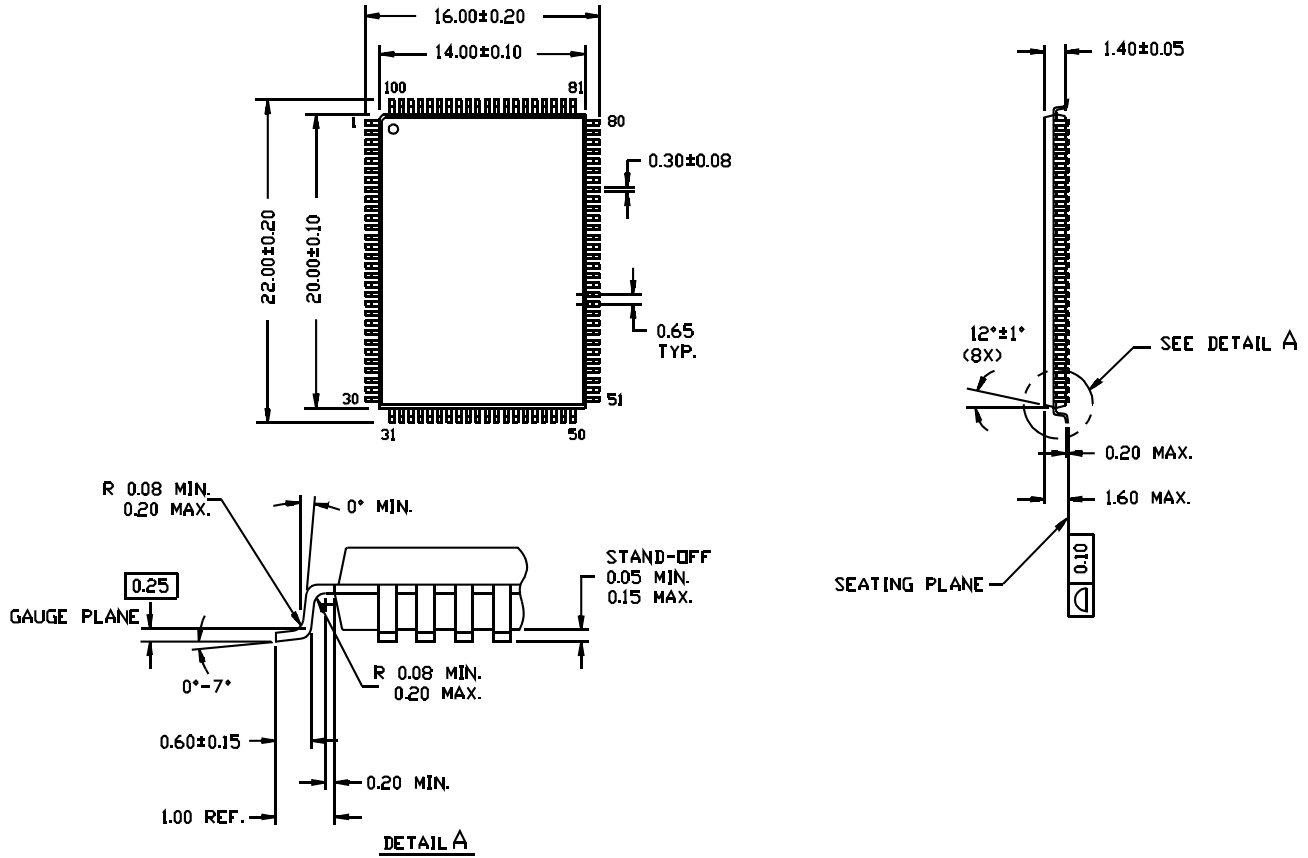
Notes:

21. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
 22. DQs are in high-Z when exiting ZZ sleep mode.

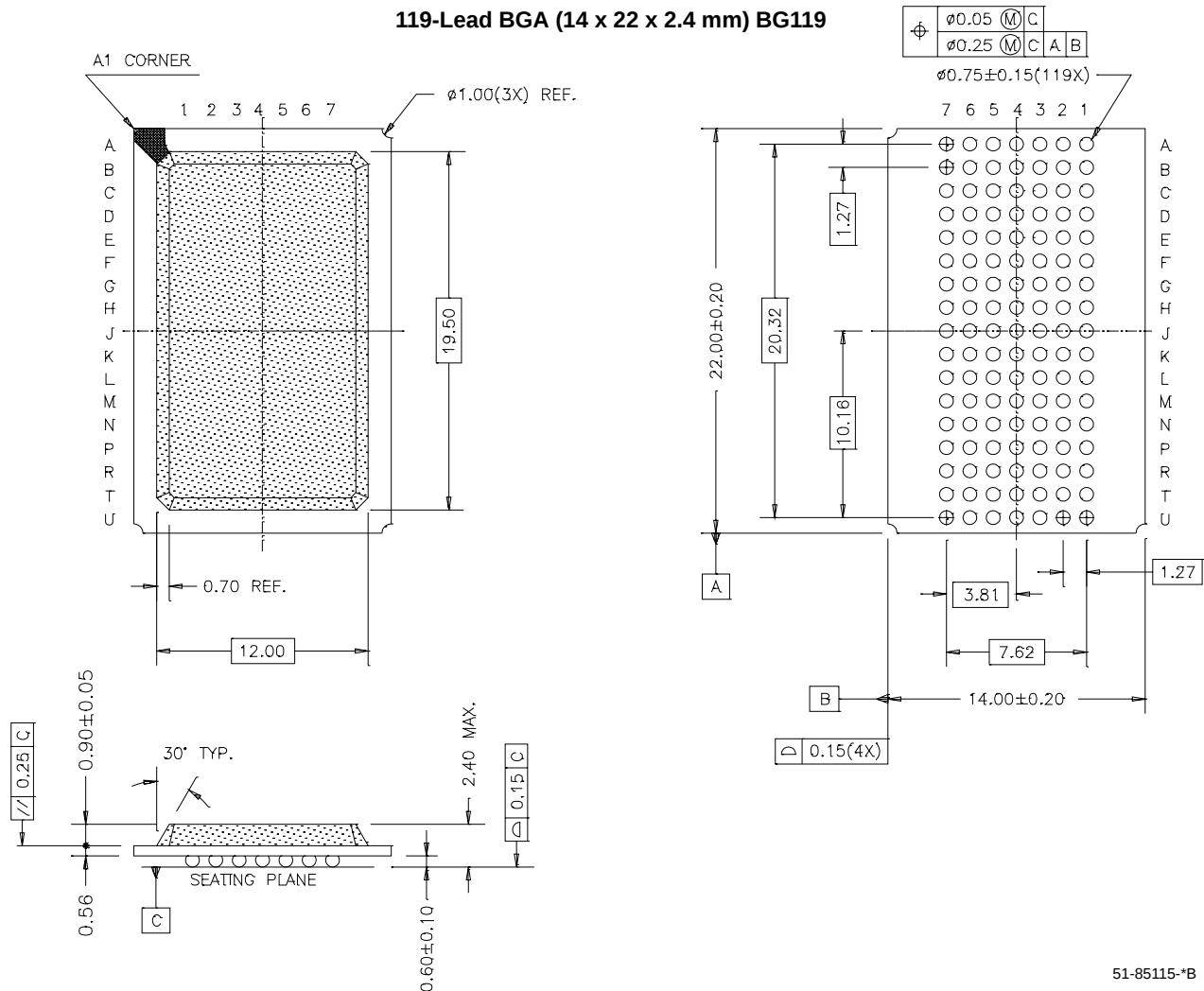
Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

DIMENSIONS ARE IN MILLIMETERS.



51-85050-*A

Package Diagrams (continued)
119-Lead BGA (14 x 22 x 2.4 mm) BG119


51-85115-*B

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Document History Page

Document Title: CY7C1345G 4-Mbit (128K x 36) Flow-Through Sync SRAM Document Number: 38-05517				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	224365	See ECN	RKF	New data sheet
*A	278513	See ECN	VBL	Deleted 66 MHz Changed TQFP package to lead-free TQFP in Ordering Information section Added BG lead-free package