

64K x 16 HIGH-SPEED CMOS STATIC RAM

JANUARY 2005

FEATURES

IS61C6416AL and IS64C6416AL

- High-speed access time: 12 ns, 15ns
- Low Active Power: 175 mW (typical)
- Low Standby Power: 1 mW (typical)
CMOS standby

IS62C6416AL and IS65C6416AL

- High-speed access time: 35 ns, 45ns
- Low Active Power: 50 mW (typical)
- Low Standby Power: 100 μ W (typical)
CMOS standby
- TTL compatible interface levels
- Single 5V $\pm$ 10% power supply
- Fully static operation: no clock or refresh required
- Available in 44-pin SOJ package and 44-pin TSOP (Type II)
- Commercial, Industrial and Automotive temperature ranges available
- Lead-free available

DESCRIPTION

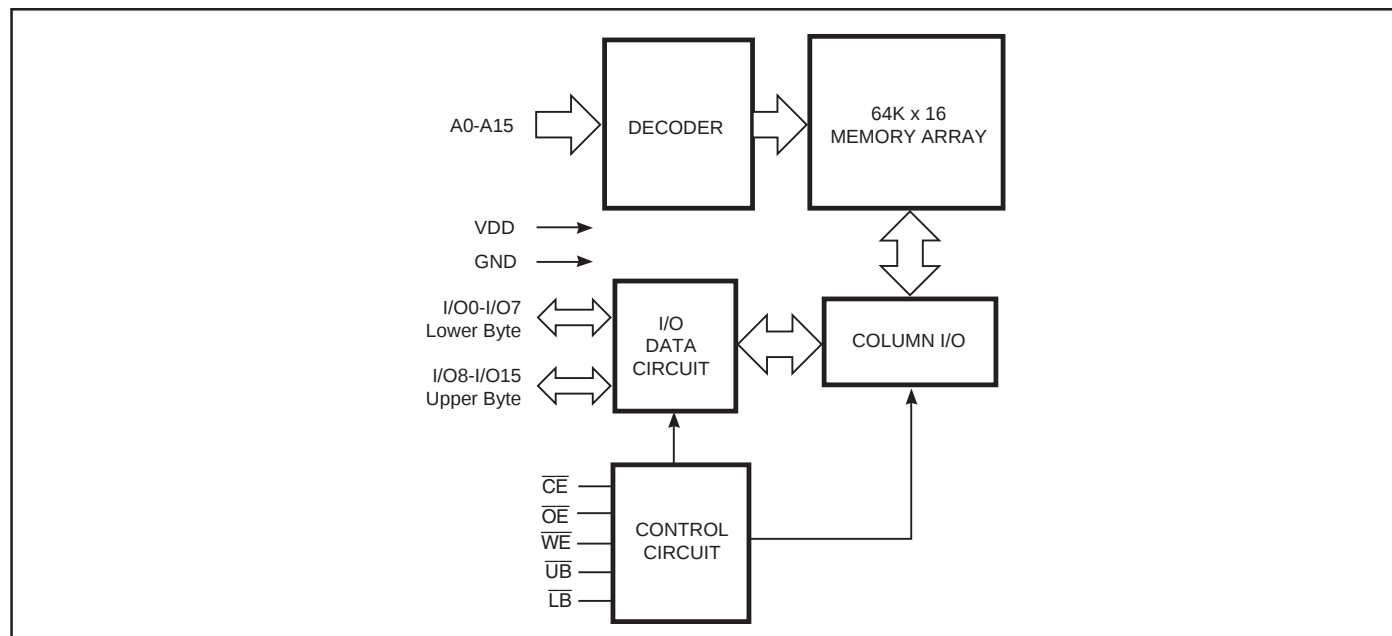
The *ISSI* IS61C6416AL, IS62C6416AL, IS64C6416AL and IS65C6416AL are high-speed, 1,048,576-bit static RAMs organized as 65,536 words by 16 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS61C6416AL, IS62C6416AL, IS64C6416AL and IS65C6416AL are packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP (Type II).

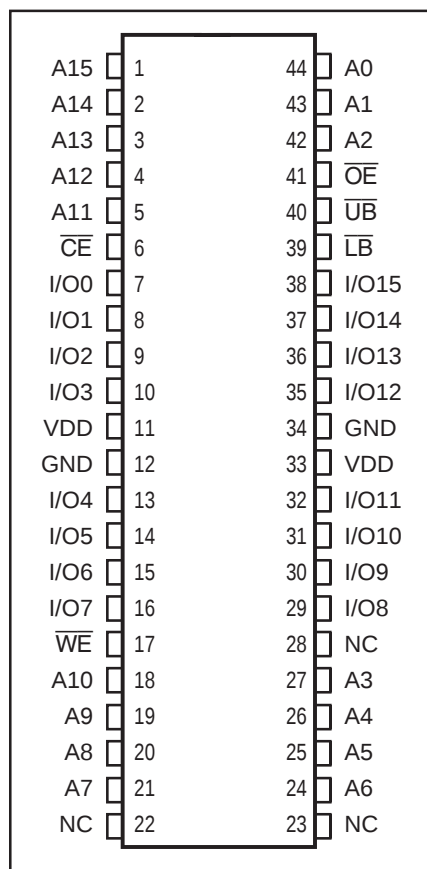
FUNCTIONAL BLOCK DIAGRAM



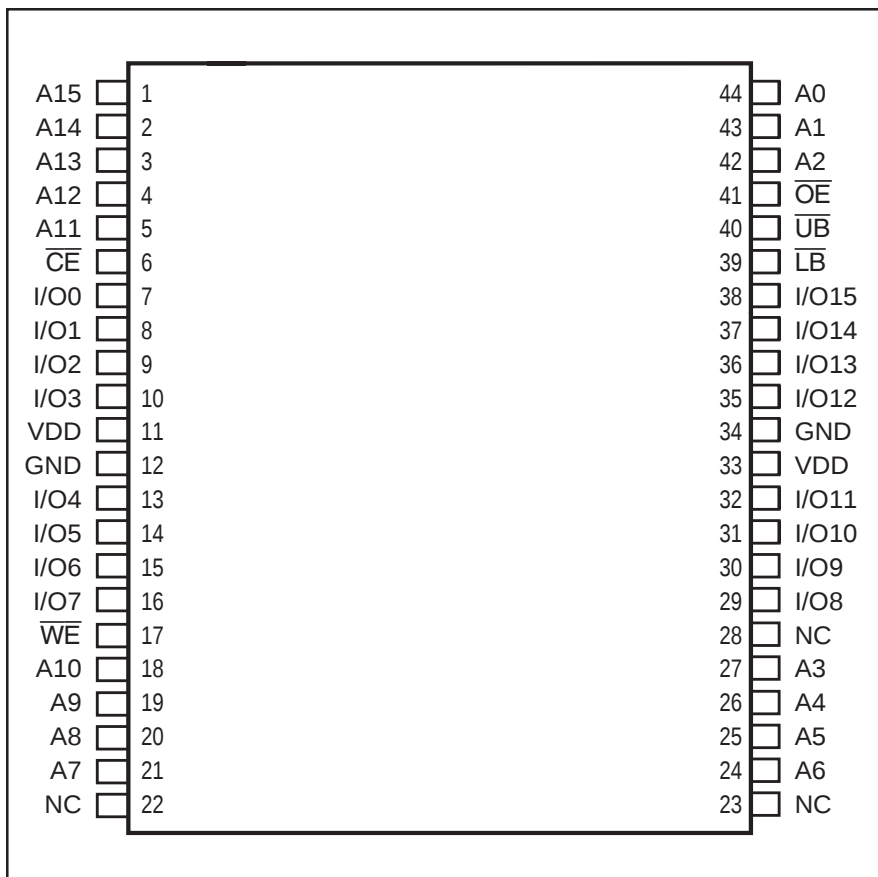
Copyright © 2005 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

PIN CONFIGURATIONS

44-Pin SOJ



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A15	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CE	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input

LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V_{DD} Current
						I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	High-Z	High-Z	Isb1, Isb2
Output Disabled	H	L	H	X	X	High-Z	High-Z	Icc1, Icc2
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	Dout	High-Z	Icc1, Icc2
	H	L	L	H	L	High-Z	Dout	
	H	L	L	L	L	Dout	Dout	
Write	L	L	X	L	H	Din	High-Z	Icc1, Icc2
	L	L	X	H	L	High-Z	Din	
	L	L	X	L	L	Din	Din	

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (IS61C/62C6416AL)

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

OPERATING RANGE (IS64C/65C6416AL)

Range	Ambient Temperature	V_{DD}
Automotive	-40°C to +125°C	5V ± 10%

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -4.0 mA		2.4	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 8.0 mA		—	0.4	V
V _{IH}	Input HIGH Voltage			2.2	V _{DD} + 0.5	V
V _{IL}	Input LOW Voltage ⁽¹⁾			-0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	Com.	-1	1	μA
			Ind.	-2	2	
			Auto.	-5	5	
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} Outputs Disabled	Com.	-1	1	μA
			Ind.	-2	2	
			Auto.	-5	5	

Note:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

IS61C6416AL/IS64C6416AL

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-12 ns		-15 ns		Unit
				Min.	Max.	Min.	Max.	
I _{CC1}	V _{DD} Operating Supply Current	V _{DD} = V _{DD MAX.} , $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = 0	Com.	—	40			mA
			Ind.	—	45			
			Auto.			—	50	
I _{CC2}	V _{DD} Dynamic Operating Supply Current	V _{DD} = V _{DD MAX.} , $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	50			mA
			Ind.	—	55			
			Auto. typ. ⁽²⁾	—	35	—	60	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = V _{DD MAX.} , V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	1			mA
			Ind.	—	1			
			Auto.			—	1	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = V _{DD MAX.} , $\overline{CE} \leq V_{DD} - 0.2V$, V _{IN} $\geq V_{DD} - 0.2V$, or V _{IN} $\leq 0.2V$, f = 0	Com.	—	350			μA
			Ind.	—	400			
			Auto. typ. ⁽²⁾	—	200	—	450	

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 5V, T_A = 25% and not 100% tested.

IS62C6416AL/IS65C6416AL

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-35 ns		-45 ns		Unit
				Min.	Max.	Min.	Max.	
I _{CC}	Average operating Current	$\overline{CE}$ = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0 mA	Com.	—	10			mA
			Ind.	—	15			
			Auto.			—	20	
I _{CC1}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = f _{MAX} V _{IN} = V _{IH} or V _{IL}	Com.	—	35			mA
			Ind.	—	40			
			Auto.			—	45	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} , $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	1			mA
			Ind.	—	1.5			
			Auto.			—	2	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} $\geq V_{DD} - 0.2V$, or V _{IN} $\leq V_{SS} + 0.2V$, f = 0	Com.	—	5			μA
			Ind.	—	10			
			Auto.			—	15	

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-12		-15		-35		-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	12	—	15	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	35	—	45	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	12	—	15	—	35	—	45	ns
t_{DOE}	$\overline{OE}$ Access Time	—	6	—	7	—	10	—	20	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	0	6	0	6	0	10	0	15	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	3	—	5	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE}$ to High-Z Output	0	7	0	8	0	10	0	15	ns
$t_{LZCE}^{(2)}$	$\overline{CE}$ to Low-Z Output	2	—	2	—	3	—	5	—	ns
t_{BA}	$\overline{LB}, \overline{UB}$ Access Time	—	6	—	6	—	35	—	45	ns
t_{HZB}	$\overline{LB}, \overline{UB}$ to High-Z Output	0	6	0	7	0	10	0	15	ns
t_{LZB}	$\overline{LB}, \overline{UB}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

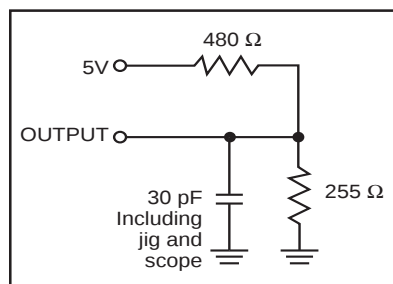


Figure 1

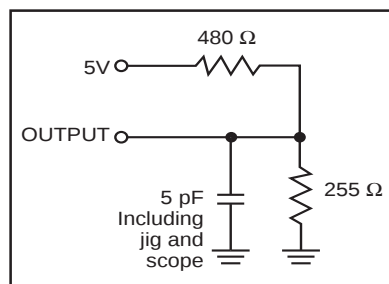
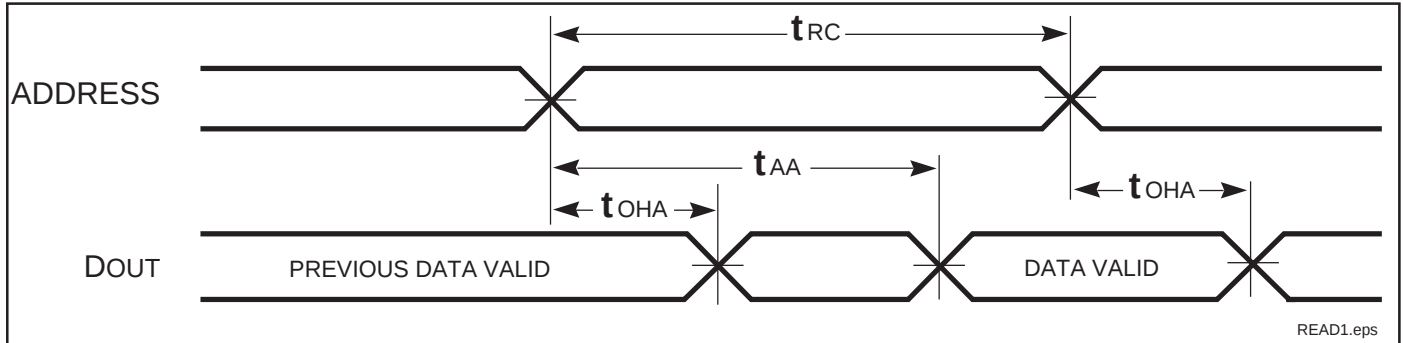


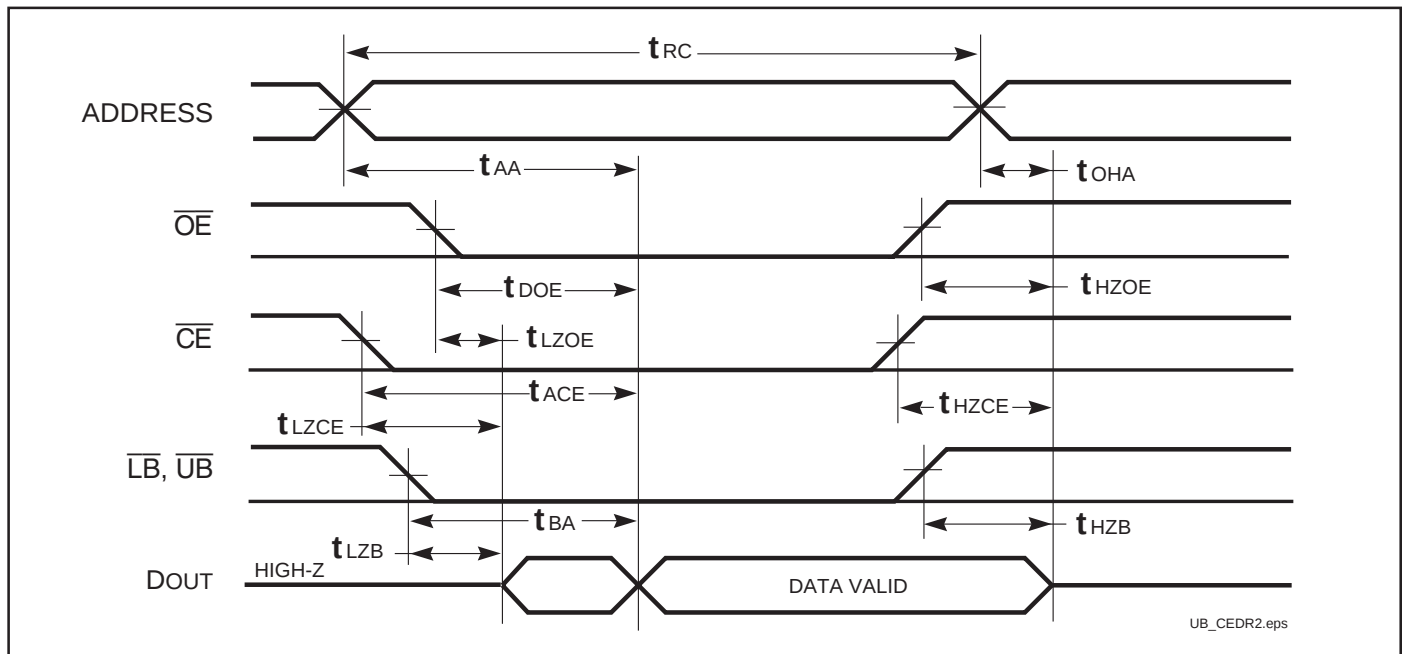
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

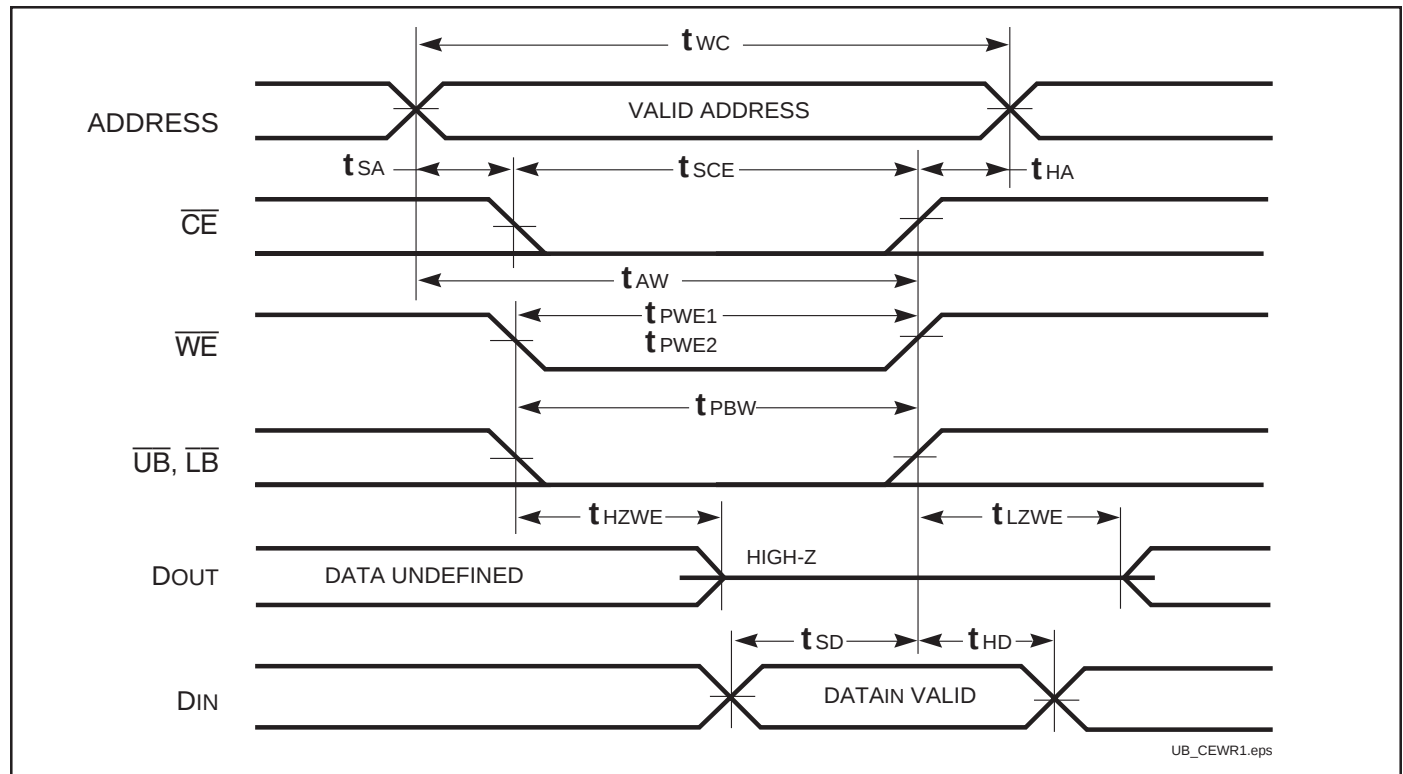
Symbol	Parameter	-12		-15		-35		-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	12	—	15	—	35	—	45	—	ns
t _{SCE}	$\overline{CE}$ to Write End	9	—	12	—	25	—	35	—	ns
t _{AW}	Address Setup Time to Write End	9	—	12	—	25	—	35	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t _{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	9	—	12	—	25	—	35	—	ns
t _{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =High)	9	—	12	—	25	—	35	—	ns
t _{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =Low)	9	—	12	—	25	—	35	—	ns
t _{SD}	Data Setup to Write End	6	—	9	—	20	—	25	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{HZWE} ⁽²⁾	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	20	—	20	ns
t _{LZWE} ⁽²⁾	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

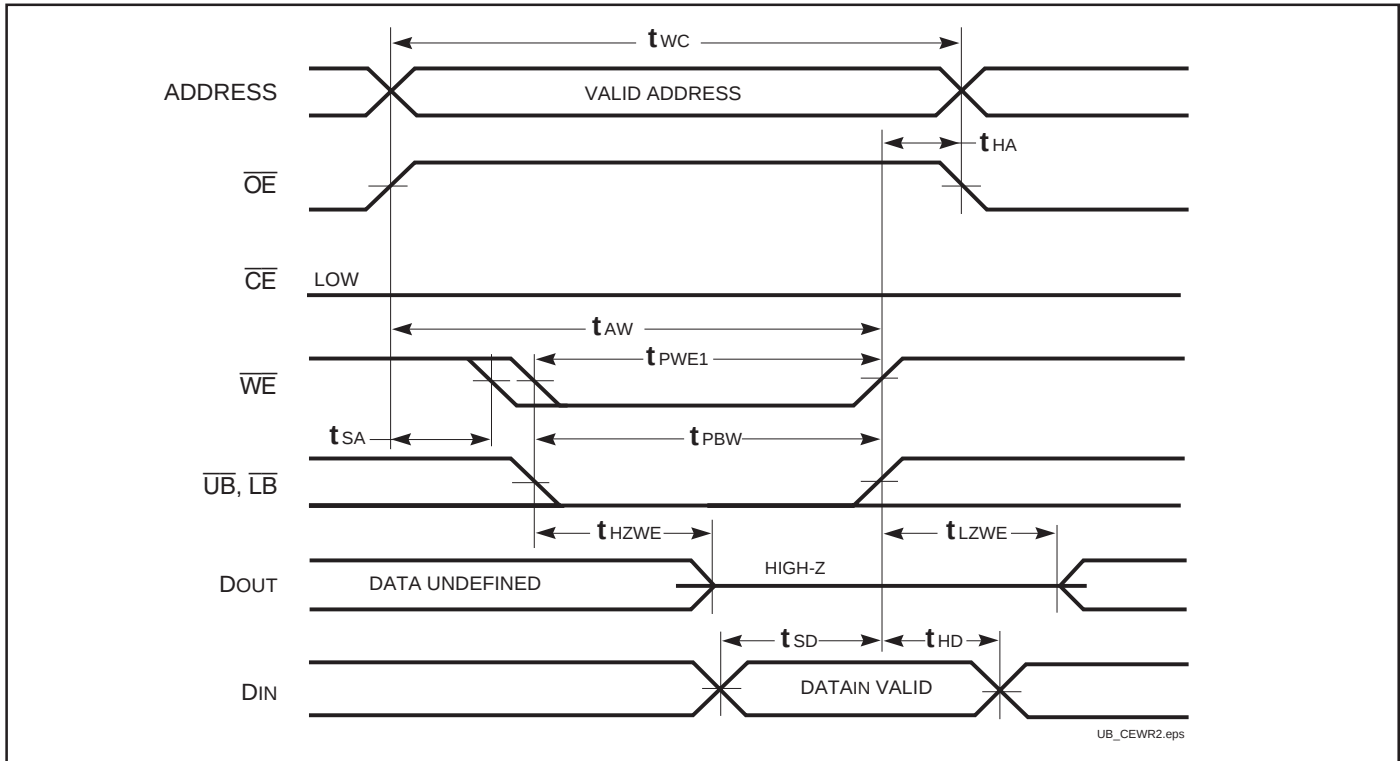
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)^(1,2)



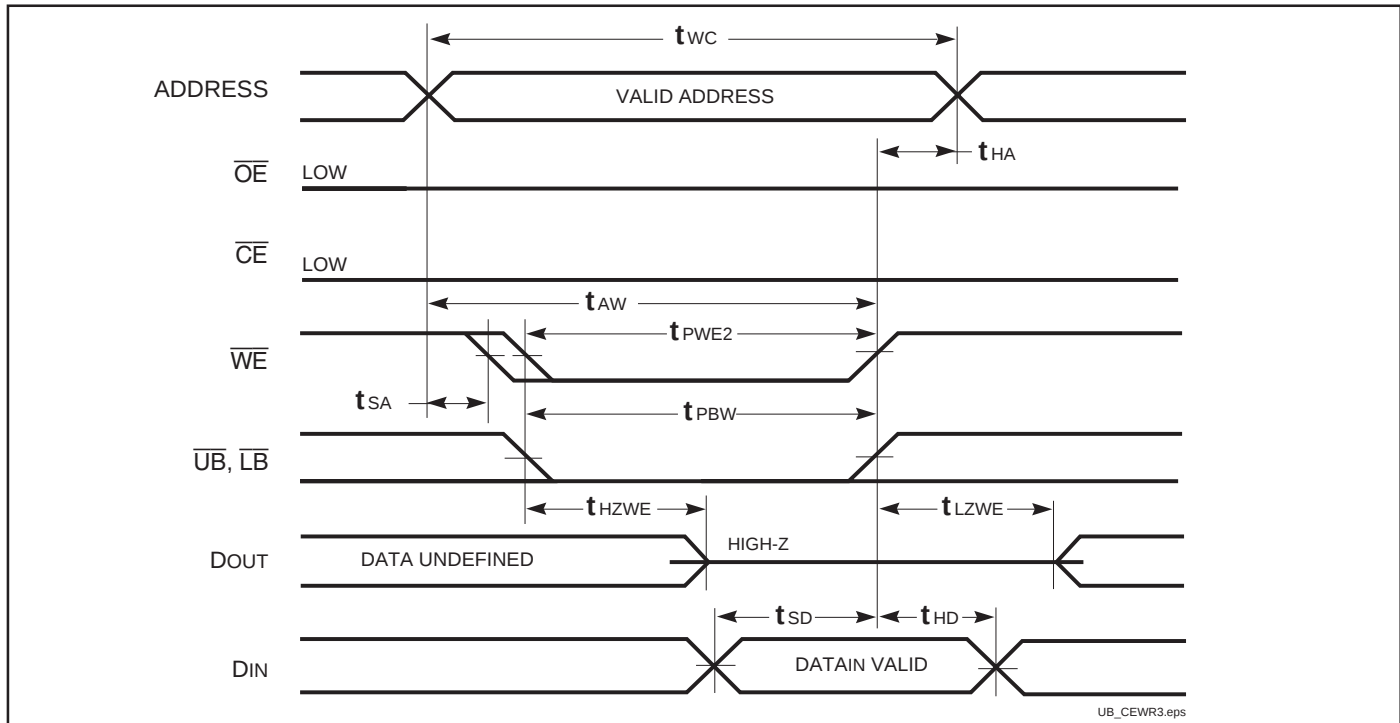
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) ^(1,2)



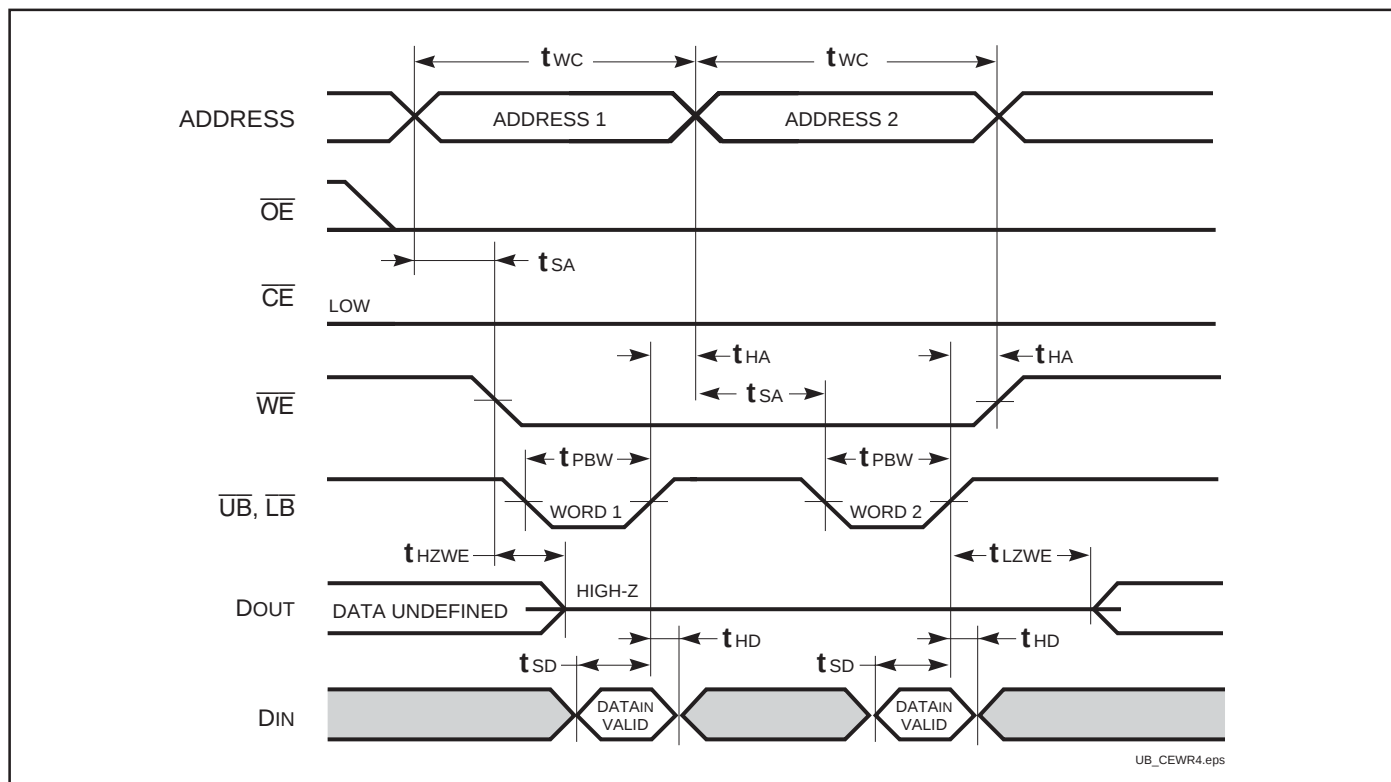
WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) ⁽¹⁾



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 4 ($\overline{UB}/\overline{LB}$ Back to Back Write)



Symbol	Parameter	Test Condition	Min.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform	2.0	5.5	V
I _{BR}	Data Retention Current	V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ V _{IN} ≥ V _{DD} − 0.2V, or V _{IN} ≤ V _{SS} + 0.2V	Com. Ind. Auto. typ. ⁽¹⁾	90 100 125	μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform	t _{RC}	—	ns

1. Typical Values are measured at $V_{DD}=5V$, $T_A=25^{\circ}C$ and not 100% tested.

The diagram illustrates the timing for Data Retention Mode. It shows three signals over time: VDD, VDR, and CE. VDD starts at 4.5V, drops to 2.2V during the retention mode, and returns to 4.5V. VDR starts at 2.2V, drops to 1.1V during the retention mode, and returns to 2.2V. CE starts at GND, rises to VDD during the retention mode, and returns to GND. The retention mode is defined by the period when VDD is at 2.2V and CE is at VDD. The duration of the retention mode is labeled t_{SDR}. The duration of the retention mode is also labeled t_{RDR}. The condition $\overline{CE} \geq VDD - 0.2V$ is indicated during the retention mode.

ORDERING INFORMATION: IS61C6416AL

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
12	IS61C6416AL-12K	400-mil Plastic SOJ
	IS61C6416AL-12T	44-pin TSOP-II

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61C6416AL-12KI	400-mil Plastic SOJ
	IS61C6416AL-12KLI	400-mil Plastic SOJ, Lead-free
	IS61C6416AL-12TI	44-pin TSOP-II
	IS61C6416AL-12TLI	44-pin TSOP-II, Lead-free

ORDERING INFORMATION: IS64C6416AL

Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
15	IS64C6416AL-15KA3	400-mil Plastic SOJ
	IS64C6416AL-15TA3	44-pin TSOP-II

ORDERING INFORMATION: IS62C6416AL
Commercial Range: 0°C to +70°C

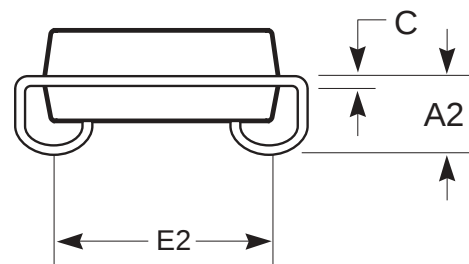
Speed (ns)	Order Part No.	Package
35	IS62C6416AL-35K	400-mil Plastic SOJ
35	IS62C6416AL-35T	44-pin TSOP-II

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
35	IS62C6416AL-35KI	400-mil Plastic SOJ
35	IS62C6416AL-35TI	44-pin TSOP-II

ORDERING INFORMATION: IS65C6416AL
Automotive Range: -40°C to +125°C

Speed (ns)	Order Part No.	Package
45	IS65C6416AL-45KA3	400-mil Plastic SOJ
45	IS65C6416AL-45TA3	44-pin TSOP-II

Package Code: K

Rev. F
10/29/03

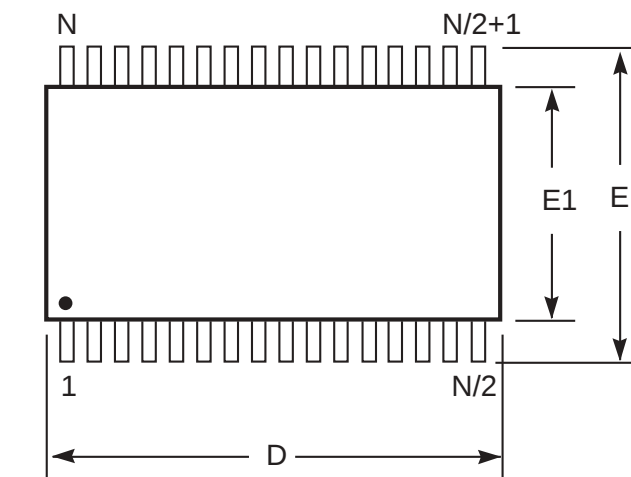
Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)	40				42				44			
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

Copyright © 2003 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

PACKAGING INFORMATION

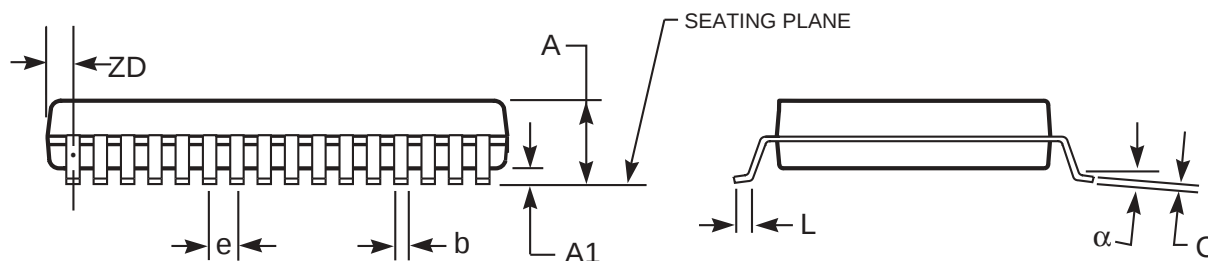
Plastic TSOP

Package Code: T (Type II)



Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

Copyright © 2003 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.