IS61SPD25632T/D IS61LPD25632T/D
IS61SPD25636T/D IS61LPD25636T/D
IS61SPD51218T/D IS61LPD51218T/D

ISSI®

256K x 32, 256K x 36, 512K x 18 SYNCHRONOUS PIPELINE, DOUBLE-CYCLE DESELECT STATIC RAM

PRELIMINARY INFORMATION
SEPTEMBER 2000

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA package
- Single +3.3V, +10%, –5% power supply
- Power-down snooze mode
- 3.3V I/O For SPD
- 2.5V I/O For LPD
- Double cycle deselect
- Snooze MODE for reduced-power standby
- T version (three chip selects)
- D version (two chip selects)

DESCRIPTION

The *ISSI* IS61SPD25632, IS61SPD25636, S61SPD51218, IS61LPD25632, IS61LPD25636, and IS61LPD51218 are high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, secondary cache for the Pentium™, 680X0™, and PowerPC™ microprocessors. The IS61SPD25632 and IS61LPD25632 are organized as 262,144 words by 32 bits and the IS61SPD25636 and IS61LPD25636 are organized as 262,144 words by 36 bits. The IS61SPD51218 and IS61LPS51218 are organized as 524,288 words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable ($\overline{BWE}$).input combined with one or more individual byte write signals ($\overline{BWx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

Symbol	Parameter	-166*	-150	-133	-5	Units
t_{KQ}	Clock Access Time	3.5	3.8	4	5	ns
t_{KC}	Cycle Time	6	6.7	7.5	10	ns
	Frequency	166	150	133	100	MHz

*This speed available only in SPD version

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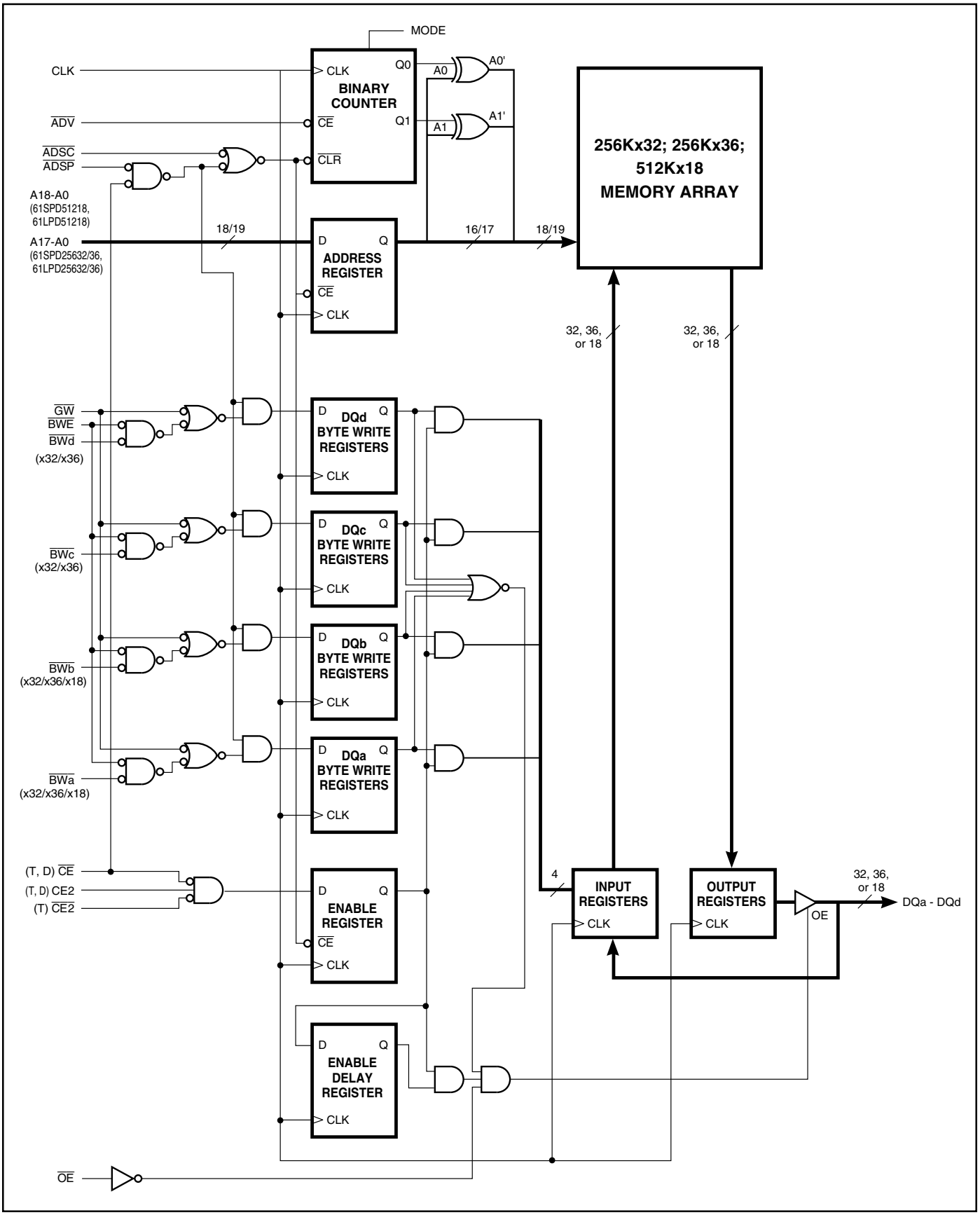
BLOCK DIAGRAM

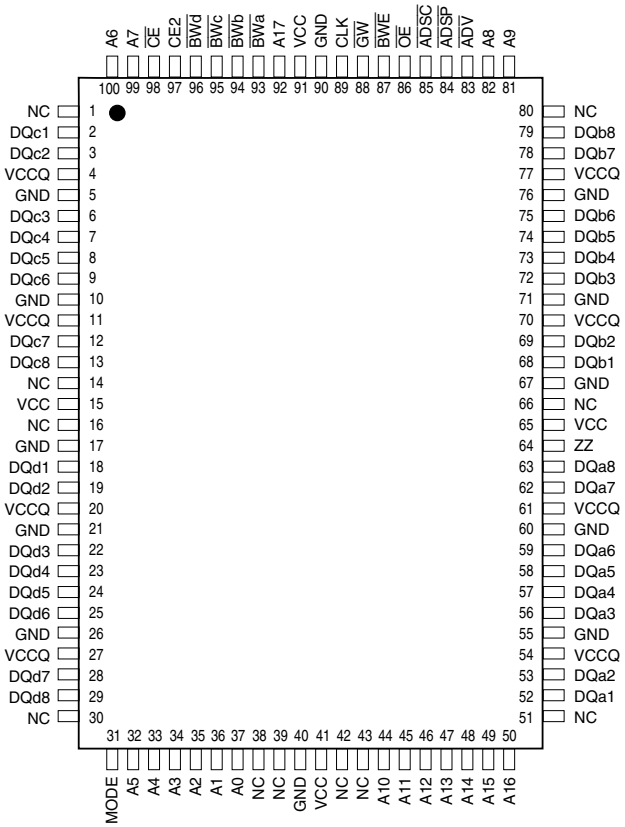


PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	A6	A4	$\overline{ADSP}$	A8	A16	VCCQ
B	NC	CE2	A3	$\overline{ADSC}$	A9	A17	NC
C	NC	A7	A2	VCC	A12	A15	NC
D	DQc1	NC	GND	NC	GND	NC	DQb8
E	DQc2	DQc3	GND	$\overline{CE}$	GND	DQb6	DQb7
F	VCCQ	DQc4	GND	$\overline{OE}$	GND	DQb5	VCCQ
G	DQc5	DQc6	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb4	DQb3
H	DQc7	DQc8	GND	$\overline{GW}$	GND	DQb2	DQb1
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	DQd1	DQd2	GND	CLK	GND	DQa7	DQa8
L	DQd4	DQd3	$\overline{BWd}$	NC	$\overline{BWa}$	DQa5	DQa6
M	VCCQ	DQd5	GND	$\overline{BWE}$	GND	DQa4	VCCQ
N	DQd6	DQd7	GND	A1	GND	DQa3	DQa2
P	DQd8	NC	GND	A0	GND	NC	DQa1
R	NC	A5	MODE	VCC	NC	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ
U	VCCQ	NC	NC	NC	NC	NC	VCCQ

100-Pin TQFP (D Version)



256K x 32

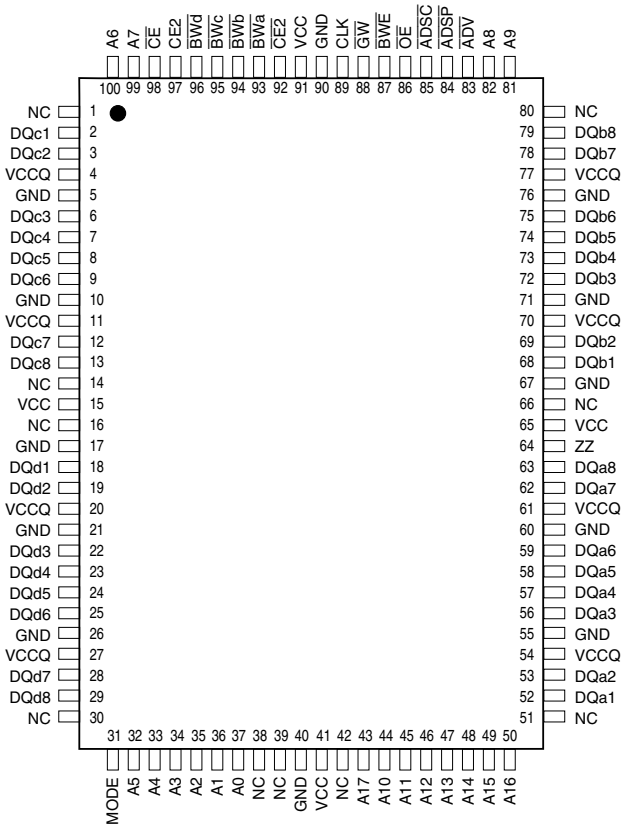
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
GND_Q	Isolated Output Buffer Ground

PIN CONFIGURATION

100-Pin TQFP (T Version)



256K x 32

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$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

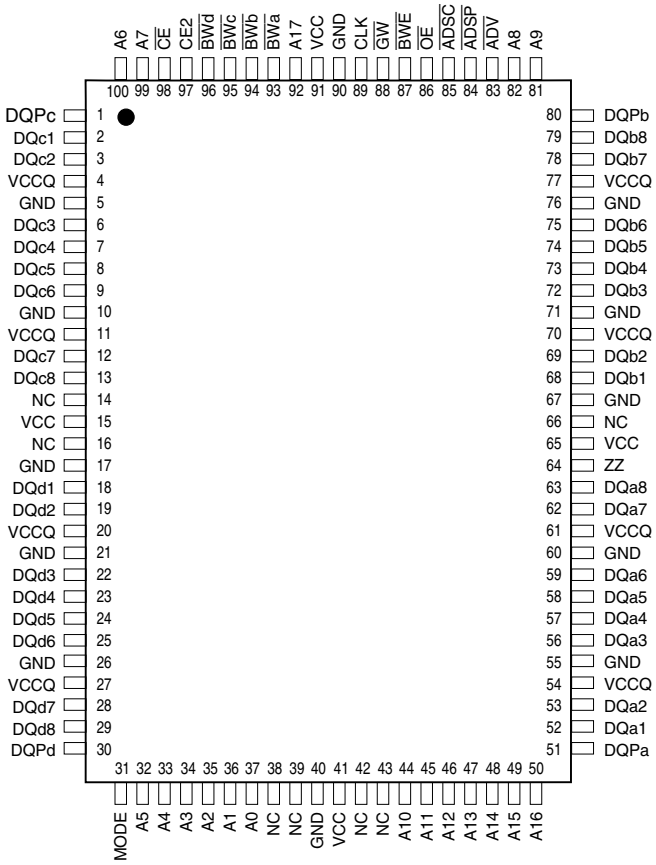
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
GND_Q	Isolated Output Buffer Ground

PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	A6	A4	$\overline{ADSP}$	A8	A16	VCCQ
B	NC	CE2	A3	$\overline{ADSC}$	A9	A17	NC
C	NC	A7	A2	VCC	A12	A15	NC
D	DQc1	DQPc	GND	NC	GND	DQPb	DQb8
E	DQc2	DQc3	GND	$\overline{CE}$	GND	DQb6	DQb7
F	VCCQ	DQc4	GND	$\overline{OE}$	GND	DQb5	VCCQ
G	DQc5	DQc6	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb4	DQb3
H	DQc7	DQc8	GND	$\overline{GW}$	GND	DQb2	DQb1
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	DQd1	DQd2	GND	CLK	GND	DQa7	DQa8
L	DQd4	DQd3	$\overline{BWd}$	NC	$\overline{BWa}$	DQa5	DQa6
M	VCCQ	DQd5	GND	$\overline{BWE}$	GND	DQa4	VCCQ
N	DQd6	DQd7	GND	A1	GND	DQa3	DQa2
P	DQd8	DQPd	GND	A0	GND	DQPa	DQa1
R	NC	A5	MODE	VCC	NC	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ
U	VCCQ	NC	NC	NC	NC	NC	VCCQ

100-Pin TQFP (D Version)



256K x 36

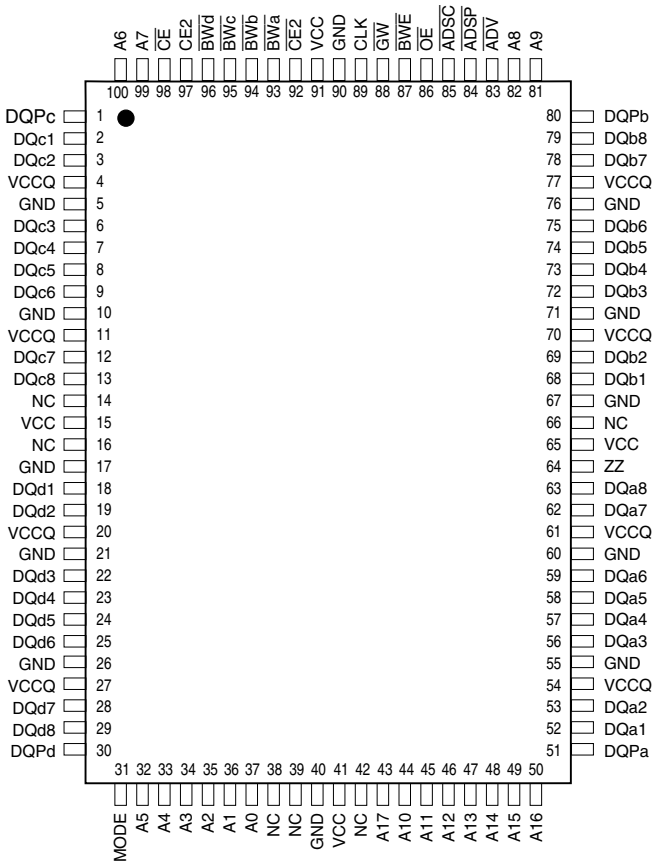
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION

100-Pin TQFP (T Version)



256K x 36

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

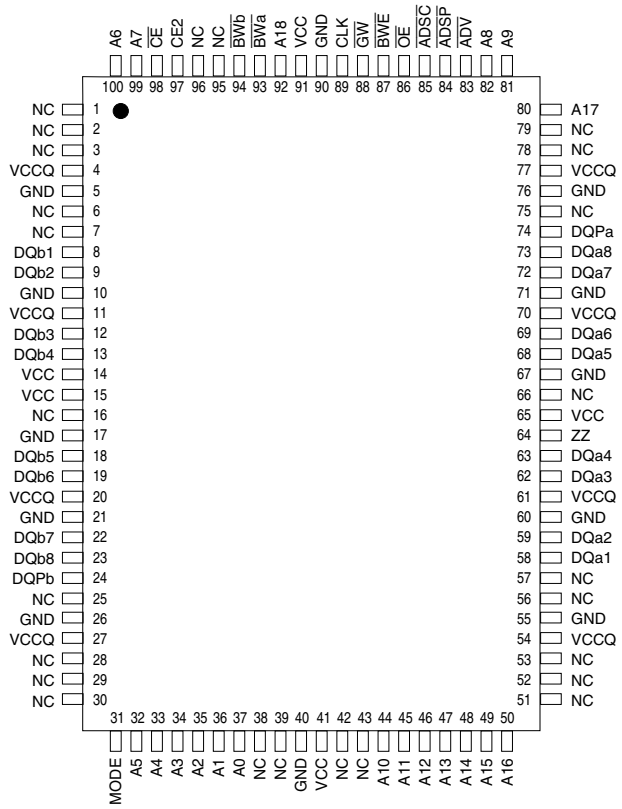
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	A6	A4	$\overline{ADSP}$	A8	A16	VCCQ
B	NC	CE2	A3	$\overline{ADSC}$	A9	A18	NC
C	NC	A7	A2	VCC	A12	A15	NC
D	DQb1	NC	GND	NC	GND	DQPa	NC
E	NC	DQb2	GND	$\overline{CE}$	GND	NC	DQa8
F	VCCQ	NC	GND	$\overline{OE}$	GND	DQa7	VCCQ
G	NC	DQb3	BWb	$\overline{ADV}$	GND	NC	DQa6
H	DQb4	NC	GND	$\overline{GW}$	GND	DQa5	NC
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	NC	DQb5	GND	CLK	GND	NC	DQa4
L	DQb6	NC	GND	NC	BWa	DQa3	NC
M	VCCQ	DQb7	GND	$\overline{BWE}$	GND	NC	VCCQ
N	DQb8	NC	GND	A1	GND	DQa2	NC
P	NC	DQPb	GND	A0	GND	NC	DQa1
R	NC	A5	MODE	VCC	NC	A13	NC
T	NC	A11	A10	NC	A14	A17	ZZ
U	VCCQ	NC	NC	NC	NC	NC	VCCQ

100-Pin TQFP (D Version)



512K x 18

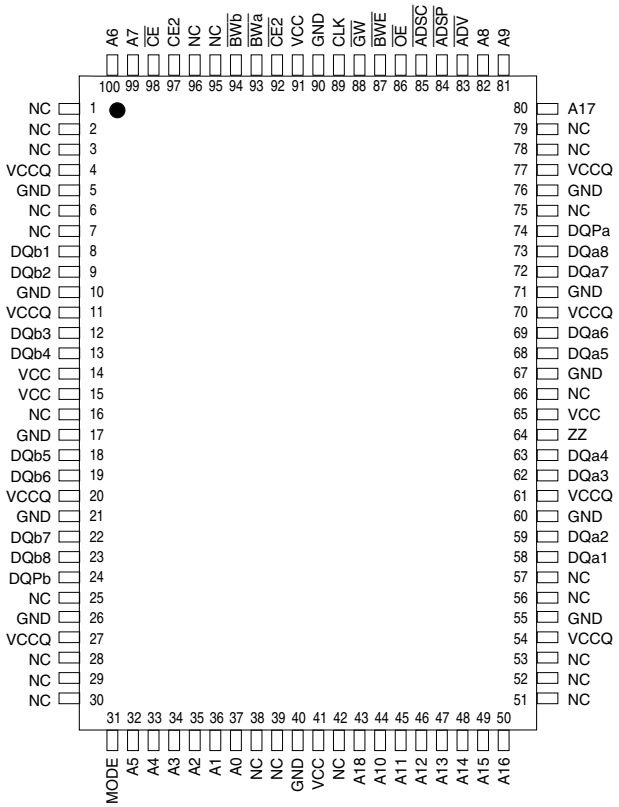
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A18	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWb}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQb	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPb	Parity Data I/O DQPa is parity for DQa1-8; DQPb is parity for DQb1-8

PIN CONFIGURATION

100-Pin TQFP (T Version)



512K x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A18	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWb}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQb	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPb	Parity Data I/O DQPa is parity for DQa1-8; DQPb is parity for DQb1-8

TRUTH TABLE

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	Q
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	D
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	D

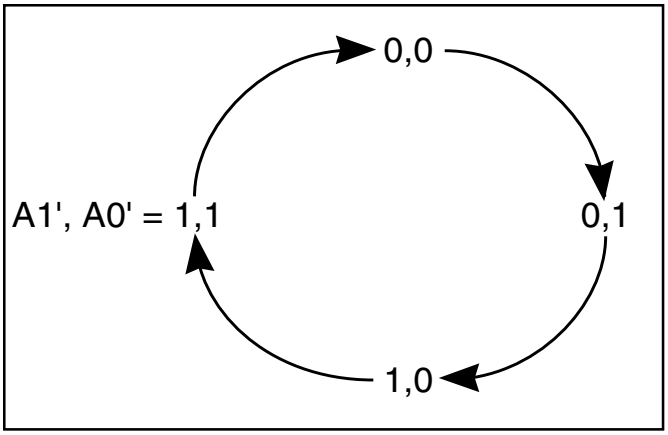
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = Vcc or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{CCQ} + 0.5	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs	–0.5 to V_{CC} + 0.5	V
V_{CC}	Voltage on Vcc Supply Relatiive to GND	–0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	Vcc	Vccq
Commercial	0°C to +70°C	3.3V, +10%, –5%	2.375–3.6V
Industrial	–40°C to +85°C	3.3V, +10%, –5%	2.375–3.6V

DC ELECTRICAL CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{CCQ} = 2.5V		1.7	—	V
		I_{OH} = –4.0 mA, V_{CCQ} = 3.3V		2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA, V_{CCQ} = 2.5V		—	0.7	V
		I_{OL} = 8.0 mA, V_{CCQ} = 3.3V		—	0.4	V
V_{IH}	Input HIGH Voltage	V_{CCQ} = 2.5V		1.7	V_{CCQ} + 0.3	V
		V_{CCQ} = 3.3V		2.0	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CCQ} = 2.5V		–0.3	0.7	V
		V_{CCQ} = 3.3V		–0.3	0.8	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CCQ}(2)	Com.	–2	2	µA
			Ind.	–5	5	
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CCQ}, $\overline{OE}$ = V_{IH}	Com.	–2	2	µA
			Ind.	–5	5	

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		-166* Max.	-150 Max.	-133 Max.	-100 Max.	Unit
I_{CC}	AC Operating Supply Current	Device Selected, All Inputs = V_{IL} or V_{IH} $\overline{OE}$ = V_{IH}, Vcc = Max. Cycle Time ≥ t_{KC} min.	Com.	400	370	350	300	mA
			Ind.	—	400	380	330	mA
I_{SB}	Standby Current	Device Deselected, Vcc = Max., All Inputs = V_{IH} or V_{IL} CLK Cycle Time ≥ t_{KC} min.	Com.	110	105	90	80	mA
			Ind.	—	110	95	85	mA

*This speed available only in SPD version

Notes:
1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to Vcc.
2. The MODE pin should be tied to Vcc or GND. It exhibits ±10 µA maximum leakage current when tied to - GND + 0.2V or ≥ Vcc – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V for 3.3V I/O V_{CCQ}/2V for 2.5V I/O
Output Load	See Figures 1 and 2

AC TEST LOADS

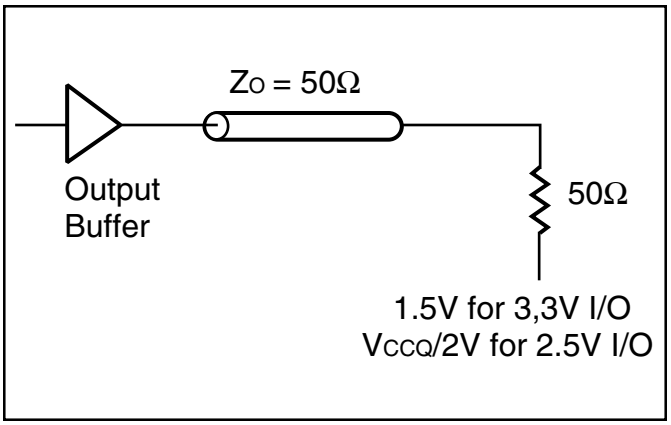


Figure 1

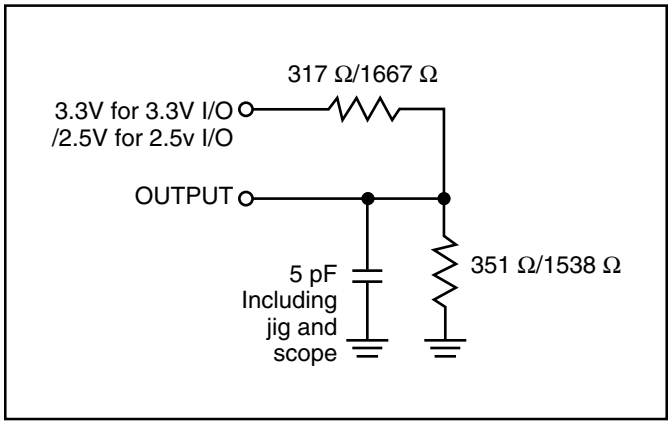


Figure 2

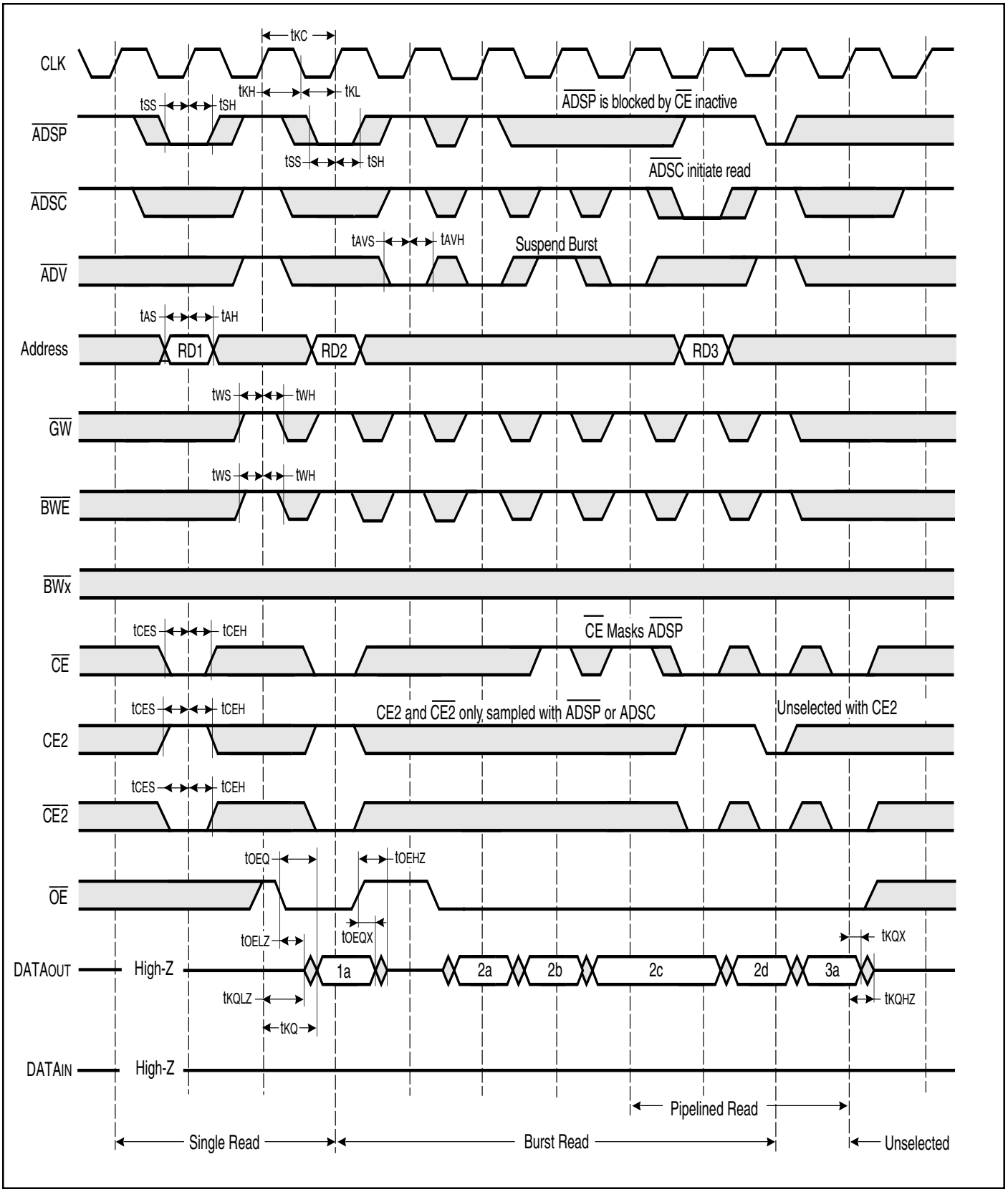
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-166*		-150		-133		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Clock Frequency	—	166	—	150	—	133	—	100	MHz
t_{KC}	Cycle Time	6	—	6.7	—	7.5	—	10	—	ns
t_{KH}	Clock High Pulse Width	2.3	—	2.5	—	2.8	—	3	—	ns
t_{KL}	Clock Low Pulse Width	2.3	—	2.5	—	2.8	—	3	—	ns
t_{KQ}	Clock Access Time	—	3.5	—	3.8	—	4	—	5	ns
t_{KQX}(1)	Clock High to Output Invalid	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{KQLZ}(1,2)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	ns
t_{KQHZ}(1,2)	Clock High to Output High-Z	—	3.5	—	3.8	—	4	—	5	ns
t_{OEQ}	Output Enable to Output Valid	—	3.5	—	3.8	—	4	—	5	ns
t_{OELZ}(1,2)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
t_{OEHZ}(1,2)	Output Enable to Output High-Z	—	3.2	—	3.8	—	4	—	5	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{WS}	Write Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns

*This speed available only in SPD version

Note:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

READ/WRITE CYCLE TIMING

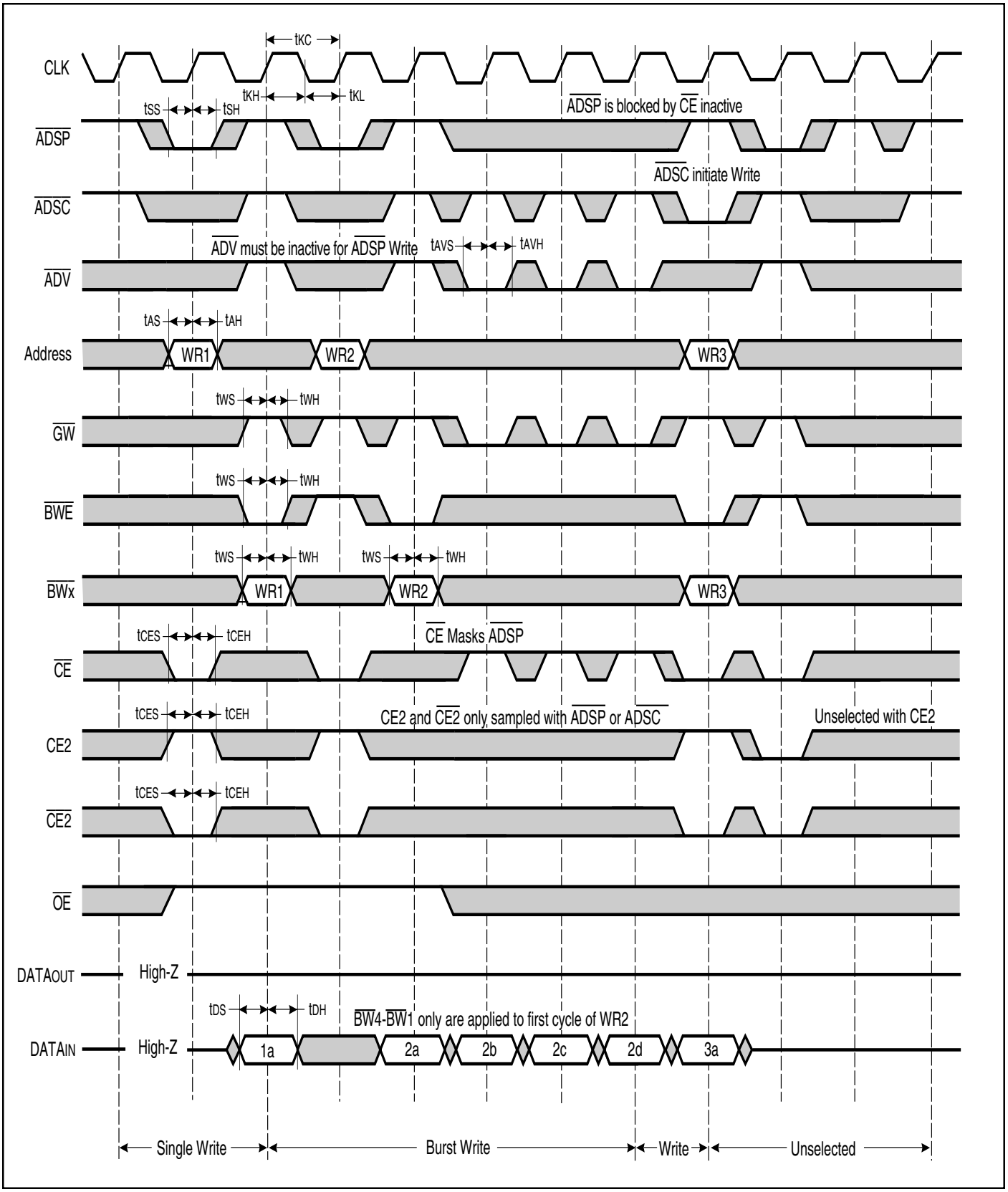


WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-166*		-150		-133		-100		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{KC}	Cycle Time	6	—	6.7	—	7.5	—	10	—	ns
t_{KH}	Clock High Pulse Width	2.3	—	2.5	—	2.8	—	3	—	ns
t_{KL}	Clock Low Pulse Width	2.3	—	2.5	—	2.8	—	3	—	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{WS}	Write Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{DS}	Data In Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	2	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{DH}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns

*This speed available only in SPD version

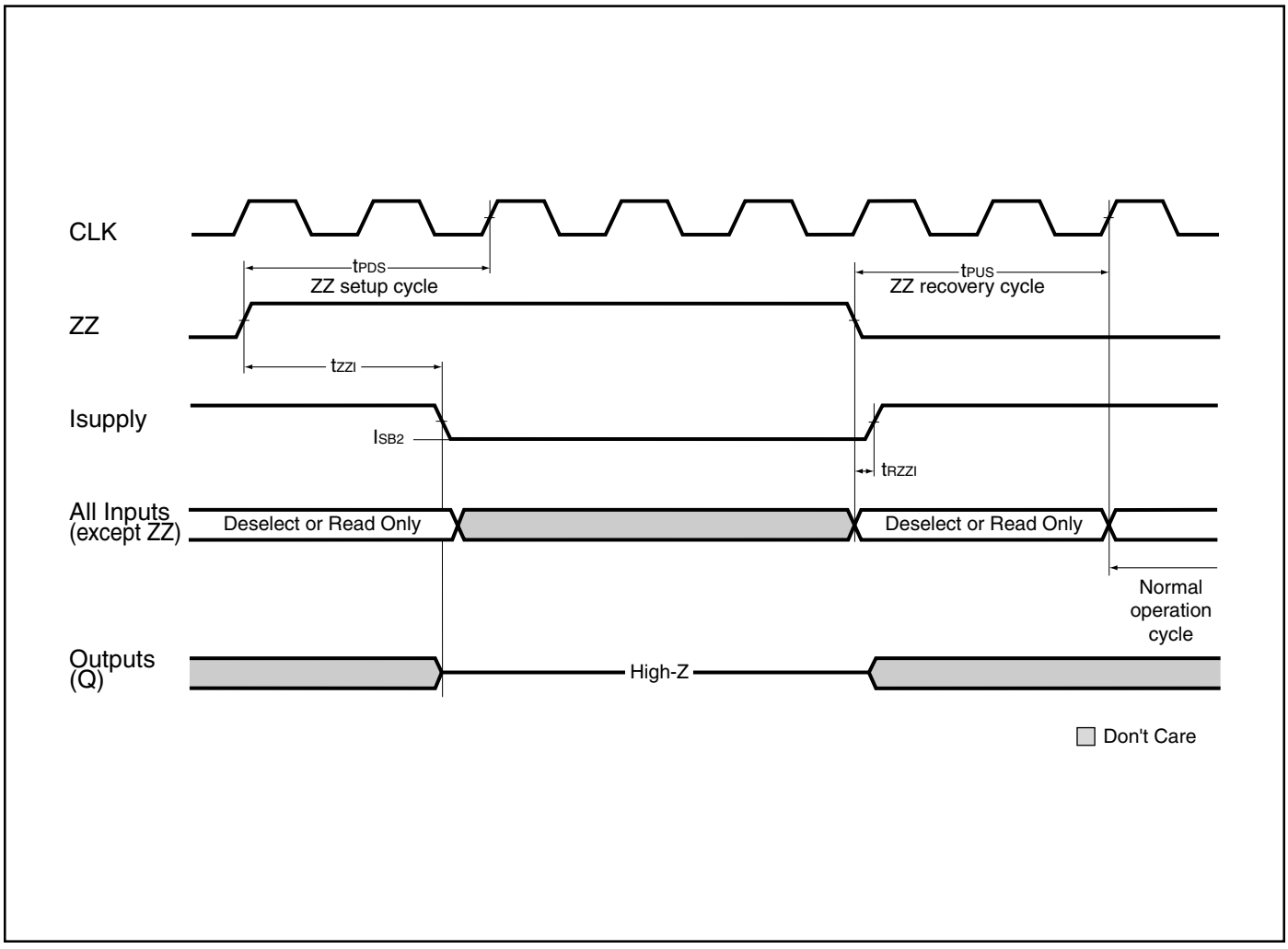
WRITE CYCLE TIMING



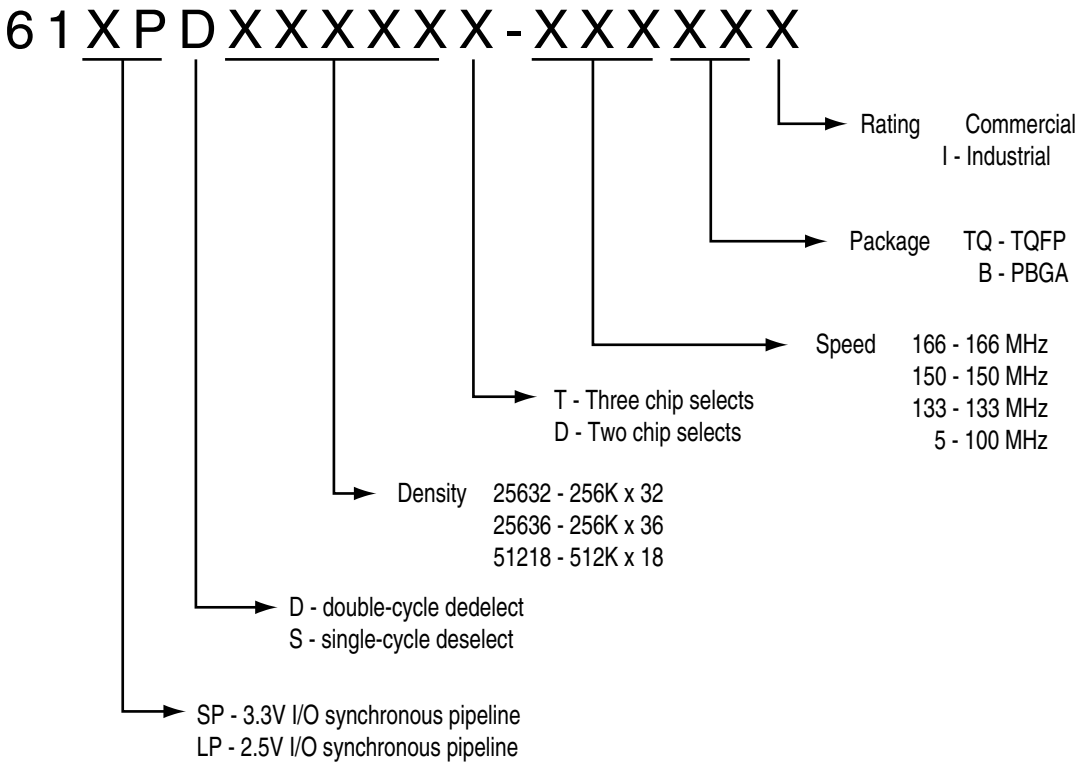
SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SNOOZE MODE	ZZ ≥ Vih	—	30	mA
t_{PDS}	ZZ active to input ignored		—	2	cycle
t_{PUS}	ZZ inactive to input sampled		2	—	cycle
t_{ZZI}	ZZ active to SNOOZE current		—	2	cycle
t_{RZZI}	ZZ inactive to exit SNOOZE current		0	—	ns

SLEEP MODE TIMING



PART IDENTIFICATION



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166 MHz	IS61SPD25632T-166TQ	TQFP
	IS61SPD25632D-166TQ	TQFP
	IS61SPD25632D-166B	PBGA
150 MHz	IS61SPD25632T-150TQ	TQFP
	IS61SPD25632D-150TQ	TQFP
	IS61SPD25632D-150B	PBGA
133 MHz	IS61SPD25632T-133TQ	TQFP
	IS61SPD25632D-133TQ	TQFP
	IS61SPD25632D-133B	PBGA
100 MHz	IS61SPD25632T-5TQ	TQFP
	IS61SPD25632D-5TQ	TQFP
	IS61SPD25632D-5B	PBGA

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166 MHz	IS61SPD25636T-166TQ	TQFP
	IS61SPD25636D-166TQ	TQFP
	IS61SPD25636D-166B	PBGA
150 MHz	IS61SPD25636T-150TQ	TQFP
	IS61SPD25636D-150TQ	TQFP
	IS61SPD25636D-150B	PBGA
133 MHz	IS61SPD25636T-133TQ	TQFP
	IS61SPD25636D-133TQ	TQFP
	IS61SPD25636D-133B	PBGA
100 MHz	IS61SPD25636T-5TQ	TQFP
	IS61SPD25636D-5TQ	TQFP
	IS61SPD25636D-5B	PBGA

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
150 MHz	IS61SPD25632T-150TQI	TQFP
	IS61SPD25632D-150TQI	TQFP
133 MHz	IS61SPD25632T-133TQI	TQFP
	IS61SPD25632D-133TQI	TQFP
100 MHz	IS61SPD25632T-5TQI	TQFP
	IS61SPD25632D-5TQI	TQFP

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
150 MHz	IS61SPD25636T-150TQI	TQFP
	IS61SPD25636D-150TQI	TQFP
133 MHz	IS61SPD25636T-133TQI	TQFP
	IS61SPD25636D-133TQI	TQFP
100 MHz	IS61SPD25636T-5TQI	TQFP
	IS61SPD25636D-5TQI	TQFP

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166 MHz	IS61SPD51218T-166TQ	TQFP
	IS61SPD51218D-166TQ	TQFP
	IS61SPD51218D-166B	PBGA
150 MHz	IS61SPD51218T-150TQ	TQFP
	IS61SPD51218D-150TQ	TQFP
	IS61SPD51218D-150B	PBGA
133 MHz	IS61SPD51218T-133TQ	TQFP
	IS61SPD51218D-133TQ	TQFP
	IS61SPD51218D-133B	PBGA
100 MHz	IS61SPD51218T-5TQ	TQFP
	IS61SPD51218D-5TQ	TQFP
	IS61SPD51218D-5B	PBGA

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
150 MHz	IS61SPD51218T-150TQI	TQFP
	IS61SPD51218D-150TQI	TQFP
133 MHz	IS61SPD51218T-133TQI	TQFP
	IS61SPD51218D-133TQI	TQFP
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	IS61SPD51218D-5TQI	TQFP

ORDERING INFORMATION

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150 MHz	IS61LPD25632T-150TQ	TQFP
	IS61LPD25632D-150TQ	TQFP
	IS61LPD25632D-150B	PBGA
133 MHz	IS61LPD25632T-133TQ	TQFP
	IS61LPD25632D-133TQ	TQFP
	IS61LPD25632D-133B	PBGA
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	IS61LPD25632D-5TQ	TQFP
	IS61LPD25632D-5B	PBGA

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	IS61LPD25636D-150B	PBGA
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	IS61LPD25636D-133B	PBGA
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	IS61LPD51218D-133TQI	TQFP
100 MHz	IS61LPD51218T-5TQI	TQFP
	IS61LPD51218D-5TQI	TQFP

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