Ultrafast 4 ns Single Supply Comparators

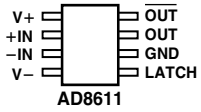
AD8611/AD8612

FEATURES
4 ns Propagation Delay at 5 V
Single Supply Operation: 3 V to 5 V
100 MHz Input
Latch Function

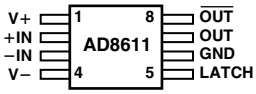
APPLICATIONS
High-Speed Timing
Clock Recovery and Clock Distribution
Line Receivers
Digital Communications
Phase Detectors
High-Speed Sampling
Read Channel Detection
PCMCIA Cards
Zero Crossing Detector
High-Speed A/D Converter
Upgrade for LT1394 and LT1016 Designs

PIN CONFIGURATIONS

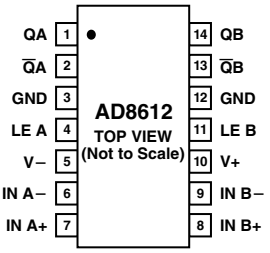
8-Lead Narrow Body SO
(SO-8)



8-Lead MSOP
(RM-8)



14-Lead TSSOP
(RU-14)



GENERAL DESCRIPTION

The AD8611/AD8612 are single and dual 4 ns comparators with latch function and complementary output.

Fast 4 ns propagation delay makes the AD8611/AD8612 a good choice for timing circuits and line receivers. Propagation delays for rising and falling signals are closely matched and track over temperature. This matched delay makes the AD8611/AD8612 a good choice for clock recovery, since the duty cycle of the output will match the duty cycle of the input.

The AD8611 has the same pinout as the LT1016 and LT1394, with lower supply current and a wider common-mode input range, which includes the negative supply rail.

The AD8611/AD8612 is specified over the industrial (–40°C to +85°C) temperature range. The AD8611 is available in both 8-lead MSOP and narrow SO-8 surface mount packages. The AD8612 is available in 14-lead TSSOP surface-mount package.

REV. 0

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AD8611/AD8612–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V+ = 5.0 V, V– = V_{GND} = 0 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	7	mV
		–40°C ≤ T_A ≤ +85°C			8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	V_{CM} = 0 V	–6	–4		µA
	I_B	–40°C ≤ T_A ≤ +85°C	–7	–4.5		µA
Input Offset Current	I_{OS}	V_{CM} = 0 V			±4	µA
Input Common-Mode Voltage Range	V_{CM}		0.0		3.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 3.0 V	55	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		3,000		V/V
Input Capacitance	C_{IN}			3.0		pF
LATCH ENABLE INPUT						
Logic "1" Voltage Threshold	V_{IH}		2.0	1.65		V
Logic "0" Voltage Threshold	V_{IL}			1.60	0.8	V
Logic "1" Current	I_{IH}	V_{LH} = 3.0 V	–1.0	–0.3		µA
Logic "0" Current	I_{IL}	V_{LL} = 0.3 V	–5	–2.7		µA
Latch Enable						
Pulsewidth	$t_{PW(E)}$			3		ns
Setup Time	t_S			0.5		ns
Hold Time	t_H			0.5		ns
DIGITAL OUTPUTS						
Logic "1" Voltage	V_{OH}	I_{OH} = 50 µA, ΔV_{IN} > 250 mV	3.0	3.35		V
Logic "1" Voltage	V_{OH}	I_{OH} = 3.2 mA, ΔV_{IN} > 250 mV	2.4	3.4		V
Logic "0" Voltage	V_{OL}	I_{OL} = 3.2 mA, ΔV_{IN} > 250 mV		0.25	0.4	V
DYNAMIC PERFORMANCE						
Input Frequency	f_{MAX}	400 mV p-p sine wave		100		MHz
Propagation Delay	t_P	200 mV Step with 100 mV Overdrive[1]		4.0	5.5	ns
		–40°C ≤ T_A ≤ +85°C		5		ns
Propagation Delay	t_P	100 mV Step with 5 mV Overdrive		5		ns
Differential Propagation Delay						
(Rising Propagation Delay vs.						
Falling Propagation Delay)	Δt_P	100 mV Step with 100 mV Overdrive[1]		0.5	2.0	ns
Rise Time		20% to 80%		2.5		ns
Fall Time		80% to 20%		1.1		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	4.5 V ≤ V+ ≤ 5.5 V	55	73		dB
V+ Supply Current[2]	I+			5.7	10	mA
		–40°C ≤ T_A ≤ +85°C			10	mA
Ground Supply Current[2]	I_{GND}	V_O = 0 V, R_L = ∞		3.5	7	mA
		–40°C ≤ T_A ≤ +85°C			7	mA
V– Supply Current[2]	I–			2.2	4	mA
		–40°C ≤ T_A ≤ +85°C			5	mA

NOTES
[1]Guaranteed by design.
[2]Per comparator.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V+ = 3.0 V, V– = V_{GND} = 0 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	7	mV
Input Bias Current	I_B	V_{CM} = 0 V	–6	–4.0		µA
	I_B	–40°C ≤ T_A ≤ +85°C	–7	–4.5		µA
Input Common-Mode Voltage Range	V_{CM}		0		1.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.0 V	55			dB
OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	I_{OH} = –3.2 mA, V_{IN} > 250 mV	1.2[1]			V
Output Low Voltage	V_{OL}	I_{OL} = +3.2 mA, V_{IN} > 250 mV			0.3	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	2.7 V ≤ V+ ≤ 6 V		46		dB
Supply Currents		V_O = 0 V, R_L = ∞				
V+ Supply Current[2]	I+			4.5	6.5	mA
		–40°C ≤ T_A ≤ +85°C			10	mA
Ground Supply Current[2]	I_{GND}			2.5	3.5	mA
		–40°C ≤ T_A ≤ +85°C			5.5	mA
V– Supply Current[2]	I–			2	3.5	mA
		–40°C ≤ T_A ≤ +85°C			4.8	mA
DYNAMIC PERFORMANCE						
Propagation Delay	t_P	100 mV Step with 20 mV Overdrive[3]		4.5	6.5	ns

NOTES
[1]Output high voltage without pull-up resistor. It may be useful to have a pull-up resistor to V+ for 3 V operation.
[2]Per comparator.
[3]Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Analog Supply Voltage . . . . . 7.0 V
Digital Supply Voltage . . . . . 7.0 V
Input Voltage[1] . . . . . ±4 V
Differential Input Voltage . . . . . ±5 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
R, RU, RM Packages . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range
R, RU, RM Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . . . 300°C

Package Type	θ_{JA}[2]	θ_{JC}	Unit
8-Lead SO (R)	158	43	°C/W
8-Lead MSOP (RM)	240	43	°C/W
14-Lead TSSOP (RU)	240	43	°C/W

NOTES
[1]The analog input voltage is equal to ±4 V or the analog supply voltage, whichever is less.
[2]θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information
AD8611ARM	–40°C to +85°C	8-Lead Micro SOIC	RM-8	G1A
AD8611AR	–40°C to +85°C	8-Lead Small Outline IC	SO-8	
AD8612ARU	–40°C to +85°C	14-Lead Thin Shrink Small Outline	RU-14	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8611/AD8612 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



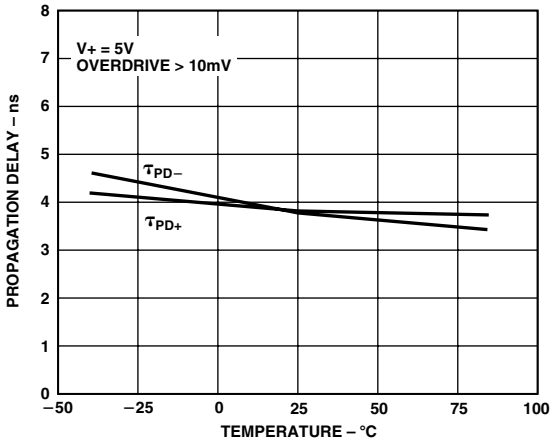


Figure 1. Propagation Delay Over Temperature

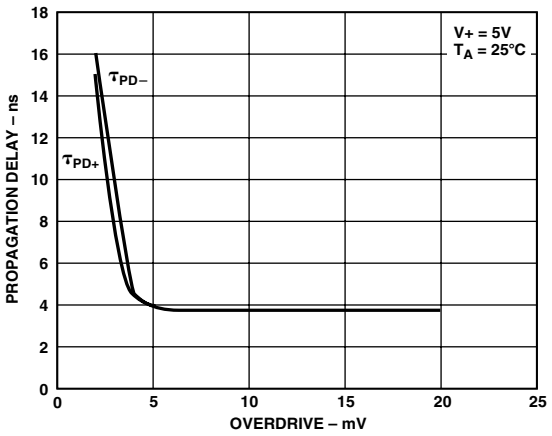


Figure 2. Propagation Delay vs. Overdrive

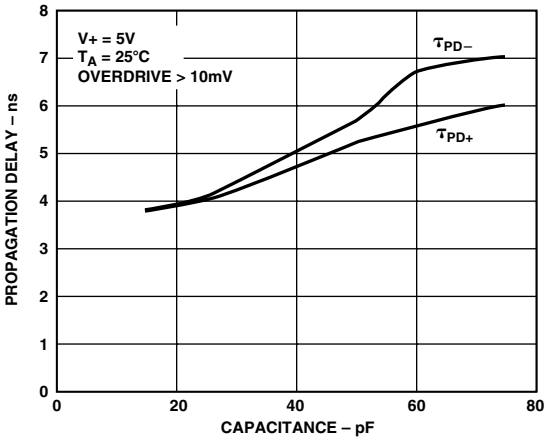


Figure 3. Propagation Delay vs. Load Capacitance

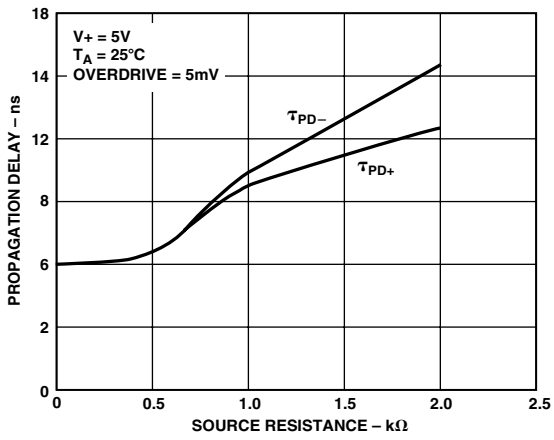


Figure 4. Propagation Delay vs. Source Resistance

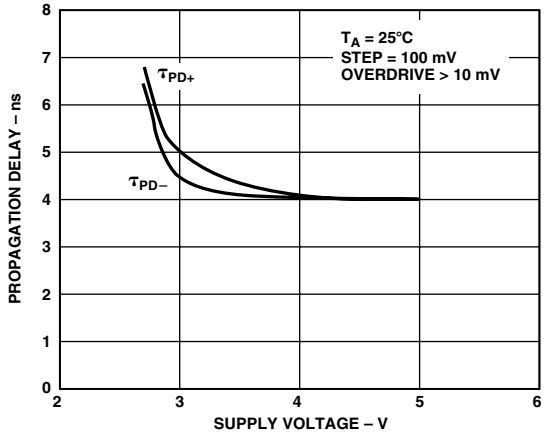


Figure 5. Propagation Delay vs. Supply Voltage

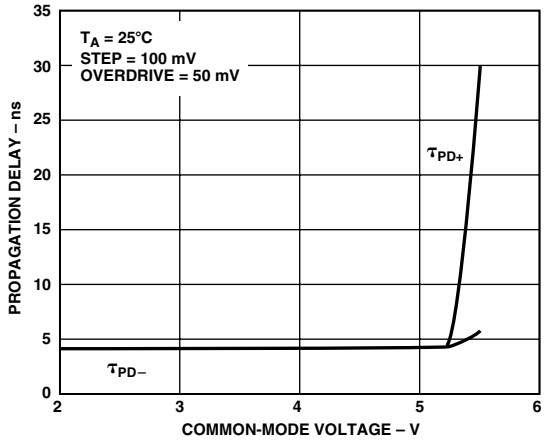


Figure 6. Propagation Delay vs. Common-Mode Voltage

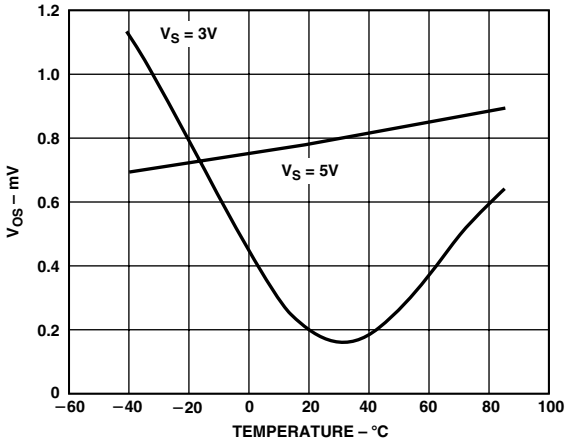


Figure 7. Offset Voltage vs. Temperature

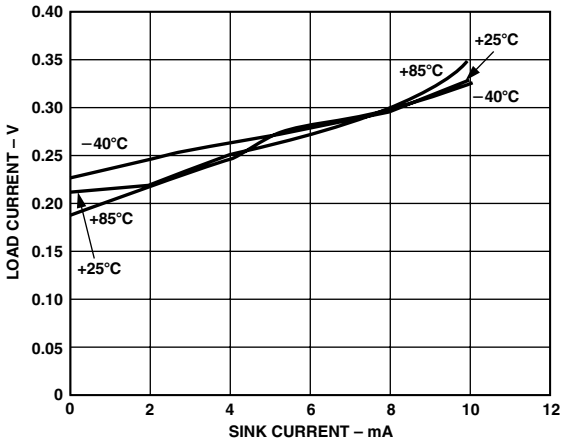


Figure 10. Output Low Voltage vs. Load Current (Sinking) Over Temperature

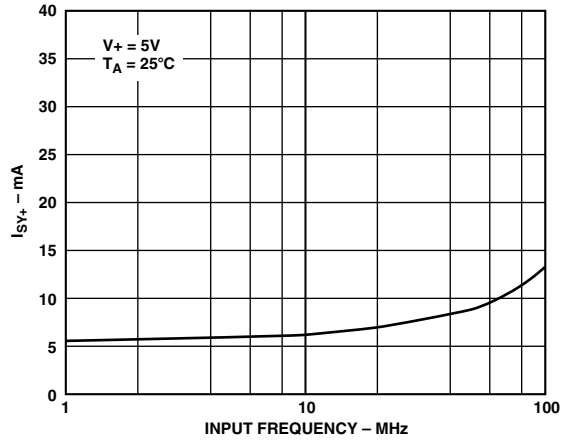


Figure 8. Supply Current vs. Input Frequency

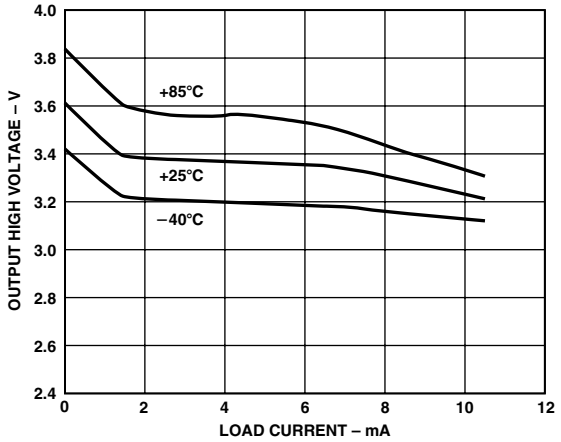


Figure 11. Output High Voltage vs. Load Current (Sourcing) Over Temperature

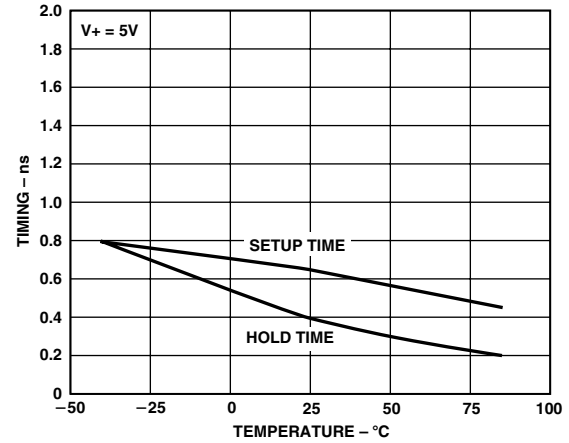


Figure 9. Latch Setup and Hold Time Over Temperature

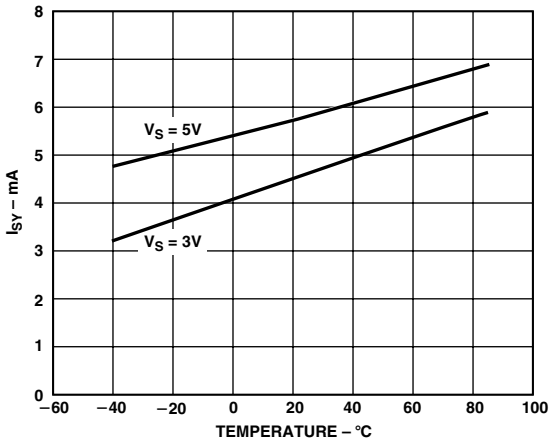


Figure 12. Supply Current vs. Temperature

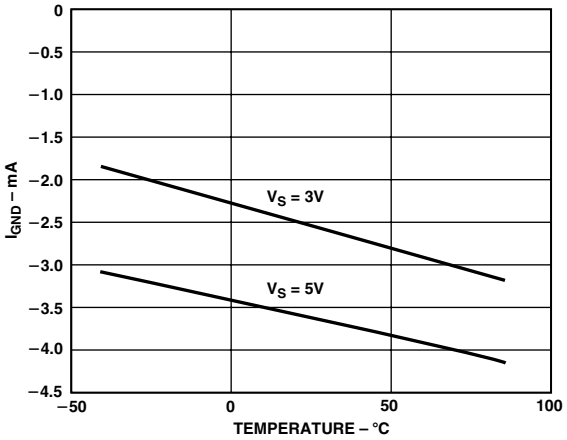


Figure 13. I_{GND} vs. Temperature

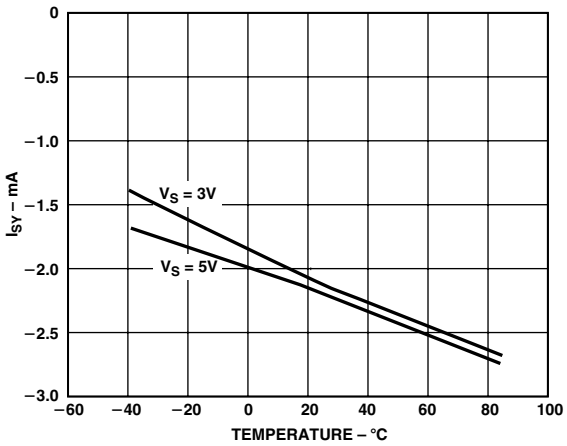


Figure 14. I_{SY}– vs. Temperature

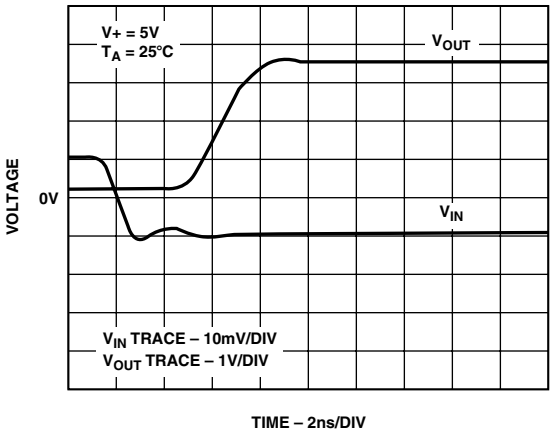


Figure 15. Rising Edge Response

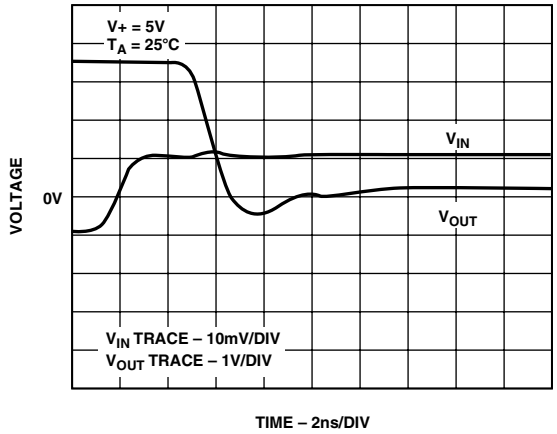


Figure 16. Falling Edge Response

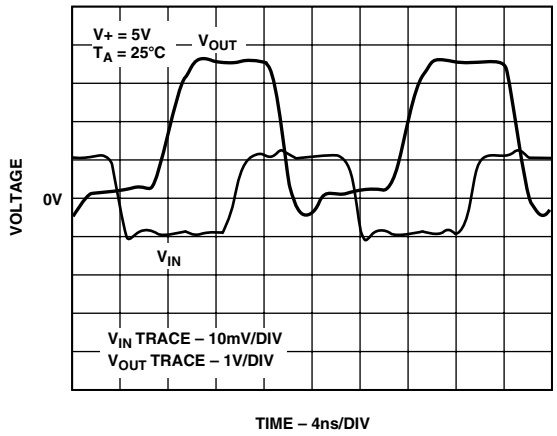


Figure 17. Response to a 50 MHz 100 mV Input Sine Wave

Optimizing High-Speed Performance

As with any high-speed comparator or amplifier, proper design and layout should be used to ensure optimal performance from the AD8611/AD8612. Excess stray capacitance or improper grounding can limit the maximum performance of high-speed circuitry.

Minimizing resistance from the source to the comparator's input is necessary to minimize the propagation delay of the circuit. Source resistance, in combination with the equivalent input capacitance of the AD8611/AD8612 creates an R-C filter that could cause a lagged voltage rise at the input to the comparator. The input capacitance of the AD8611/AD8612 in combination with stray capacitance from an input pin to ground results in several picofarads of equivalent capacitance. Using a surface-mount package and a minimum of input trace length, this capacitance is typically around 3 pF to 5 pF. A combination of 3 kΩ source resistance and 3 pF of input capacitance yields a time constant of 9 ns, which is slower than the 4 ns propagation delay of the AD8611/AD8612. Source impedances should be less than 1 kΩ for best performance.

Another important consideration is the proper use of power supply bypass capacitors around the comparator. A 1 μF bypass capacitor should be placed within 0.5 inches of the device between each power supply pin and ground. Another 10 nF ceramic capacitor should be placed as close as possible to the device in parallel with the 1 μF bypass capacitor. The 1 μF capacitor will reduce any potential voltage ripples from the power supply, and the 10 nF capacitor acts as a charge reservoir for the comparator during high-frequency switching.

A continuous ground plane on the PC board is also recommended to maximize circuit performance. A ground plane can be created by using a continuous conductive plane over the surface of the circuit board, only allowing breaks in the plane for necessary traces and vias. The ground plane provides a low inductive current return path for the power supply, thus eliminating any potential differences at different ground points throughout the circuit board caused from "ground bounce." A proper ground plane will also minimize the effects of stray capacitance on the circuit board.

Upgrading the LT1394 and LT1016

The AD8611 single comparator is pin-for-pin compatible with the LT1394 and LT1016 and offers an improvement in propagation delay over both comparators. These devices can easily be replaced with the higher performance AD8611, but there are differences and it is useful to check that these ensure proper operation.

The five major differences between the AD8611 and the LT1016 include input voltage range, input bias currents, propagation delay, output voltage swing, and power consumption. Input common-mode voltage is found by taking the average of the two voltages at the inputs to the comparator. The LT1016 has an input voltage range from 1.25 V above the negative supply to 1.5 V below the positive supply. The AD8611 input voltage range extends down to the negative supply voltage to within 2 V of V+. If the input common-mode voltage could be exceeded, input signals should be shifted or attenuated to bring them into range, keeping in mind the note about source resistance in Optimizing High-Speed Performance.

Example: An AD8611 power from a 5 V single supply has its noninverting input connected to 1 V peak-to-peak high-frequency signal centered around 2.3 V and its inverting input connected to a fixed 2.5 V reference voltage. The worst-case input common-mode voltage to the AD8611 is 2.65 V. This is well below the 3.0 V input common-mode voltage range to the comparator. Note that signals much greater than 3.0 V will result in increased input currents and may cause the comparator to operate more slowly.

The input bias current to the AD8611 is 7 μA maximum over temperature (–40°C to +85°C). This is identical to the maximum input bias current for the LT1394, and half of the maximum I_B for the LT1016. Input bias currents to the AD8611 and LT1394 flow out from the comparator's inputs, as opposed to the LT1016 whose input bias current flows into its inputs. Using low value resistors around the comparator and low impedance sources will minimize any potential voltage shifts due to bias currents.

The AD8611 is able to swing within 200 mV of ground and within 1.5 V of positive supply voltage. This is slightly more output voltage swing than the LT1016. The AD8611 also uses less current than the LT1016, 5 mA as compared to 25 mA of typical supply current.

The AD8611 has a typical propagation delay of 4 ns, compared to the LT1394 and LT1016, whose propagation delays are typically 7 ns and 10 ns, respectively.

Maximum Input Frequency and Overdrive

The AD8611 can accurately compare input signals up to 100 MHz with less than 10 mV of overdrive. The level of overdrive required increases with ambient temperature, with up to 50 mV of overdrive recommended for a 100 MHz input signal and an ambient temperature of +85°C.

It is not recommend to use an input signals with a fundamental frequency above 100 MHz as the AD8611 could draw up to 20 mA of supply current and the outputs may not settle to a definite state. The device will return to its specified performance once the fundamental input frequency returns to below 100 MHz.

Output Loading Considerations

The AD8611 can deliver up to 10 mA of output current without increasing its propagation delay. The outputs of the device should not be connected to more than 40 TTL input logic gates or drive less than 400 Ω of load resistance.

The AD8611 output has a typical output swing between ground and 1 V below the positive supply voltage. Decreasing the output load resistance to ground will lower the maximum output voltage due to the increase in output current. Table I shows the typical output high voltage versus load resistance to ground.

Table I. Maximum Output Voltage vs. Resistive Load

Output Load to Ground	$V+ - V_{OUT, HI}$ (typ)
300 Ω	1.5 V
500 Ω	1.3 V
1 kΩ	1.2 V
10 kΩ	1.1 V
> 20 kΩ	1.0 V

Connecting a 500 Ω–2 kΩ pull-up resistor to V+ on the output will help increase the output voltage closer to the positive rail; in this configuration, however, the output voltage will not reach its maximum until at least 20 ns to 50 ns after the output voltage switches. This is due to the R-C time constant between the pull-up resistor and the output and load capacitances. The output pull-up resistor will not improve propagation delay.

The AD8611 is stable with all values of capacitive load; however, loading an output with greater than 30 pF will increase the propagation delay of that channel. Capacitive loads greater than 500 pF will also create some ringing on the output wave. Table II shows propagation delay versus several values of load capacitance. The loading on one output of the AD8611 does not affect the propagation delay of the other output.

Table II. Propagation Delay vs. Capacitive Load

C_L	τ_{PD} Rising	τ_{PD} Falling
< 10 pF	3.5 ns	3.5 ns
33 pF	5 ns	5 ns
100 pF	8 ns	7 ns
390 pF	14.5 ns	10 ns
680 pF	26 ns	15 ns

Using the Latch to Maintain a Constant Output

The latch input to the AD8611/AD8612 can be used to retain data at the output of the comparator. When the latch voltage goes high, the output voltage will remain in its previous state, independent of changes in the input voltage.

The setup time for the AD8611/AD8612 is 0.5 ns and the hold time is 0.5 ns. Setup time is defined as the minimum amount of time the input voltage must remain in a valid state before the latch is activated for the latch to function properly. Hold time is defined as the amount of time the input must remain constant after the latch voltage goes high for the output to remain latched its voltage.

The latch input is TTL and CMOS compatible, so a logic high is a minimum of 2.0 V and a logic low is a maximum of 0.8 V. The latch circuitry in the AD8611/AD8612 has no built-in hysteresis.

Input Stage and Bias Currents

The AD8611 and AD8612 use a bipolar PNP differential input stage. This enables the input common-mode voltage range to extend from within 2.0 V of the positive supply voltage to 200 mV below the negative supply voltage. Therefore, using a single 5 V supply, the input common-mode voltage range is –200 mV to +3.0 V. Input common-mode voltage is the average of the voltages at the two inputs. For proper operation, the input common-mode voltage should be kept within the common-mode voltage range.

The input bias current for the AD8611/AD8612 is 4 μA, which is the amount of current that flows from each input of the comparator. This bias current will go to zero on an input that is high and will double on an input that is low, which is a characteristic common to any bipolar comparator. Care should be taken in choosing resistances to be connected around the comparator as large resistors could cause significant voltage drops due to the input bias current.

The input capacitance for the AD8611/AD8612 is typically 3 pF. This is measured by inserting a 5 kΩ source resistance in series with the input and measuring the change in propagation delay.

Using Hysteresis

Hysteresis can easily be added to a comparator through the addition of positive feedback. Adding hysteresis to a comparator offers an advantage in noisy environments where it is not desirable for the output to toggle between states when the input signal is close to the switching threshold. Figure 18 shows a simple method for configuring the AD8611 or AD8612 with hysteresis.

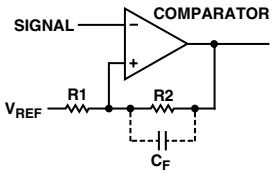


Figure 18. Configuring the AD8611/AD8612 with Hysteresis

Here, the input signal is connected directly to the inverting input of the comparator. The output is fed back to the noninverting input through R1 and R2. The ratio of R1 to R1 + R2 establishes the width of the hysteresis window with V_{REF} setting the center of the window, or the average switching voltage. The Q output will switch low when the input voltage is greater than V_{HI}, and will not switch high again until the input voltage is less than V_{LO} as given in Equation 1:

$$V_{HI} = \left(V_+ - 1.5 - V_{REF} \right) \frac{R1}{R1 + R2} + V_{REF} \qquad (1)$$

$$V_{LO} = V_{REF} \times \frac{R2}{R1 + R2}$$

Where V_+ is the positive supply voltage.

The capacitor C_F is optional and can be added to introduce a pole into the feedback network. This has the effect of increasing the amount of hysteresis at high frequencies, which is useful when comparing relatively slow signals in high-frequency noise environments. At frequencies greater than f_P, the hysteresis window approaches $V_{HI} = V_+ - 1.5$ V and $V_{LO} = 0$ V. For frequencies less than f_P, the threshold voltages remain as in Equation 1.

Clock Timing Recovery

Comparators are often used in digital systems to recover clock timing signals. High-speed square waves transmitted over a distance, even tens of centimeters, can become distorted due to stray capacitance and inductance. Poor layout or improper termination can also cause reflections on the transmission line, further distorting the signal waveform. A high-speed comparator can be used to recover the distorted waveform while maintaining a minimum of delay.

Figure 19 shows the AD8611 used to recover a 65 MHz, 100 mV peak-to-peak distorted clock signal into a 4 V peak-to-peak square wave. The lower trace is the input to the AD8611 and the upper trace is the Q output from the comparator. The AD8611 is powered from a 5 V single supply.

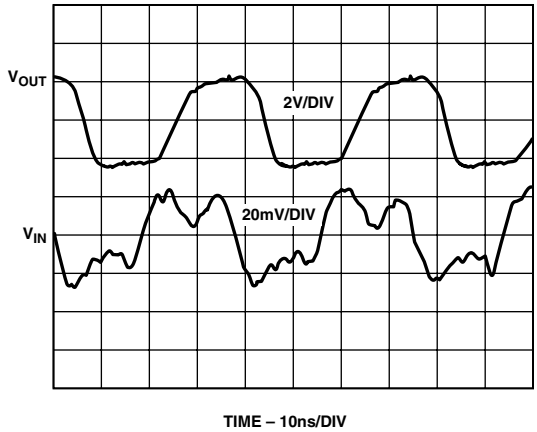


Figure 19. Using the AD8611 to Recover a Noisy Clock Signal

A 5 V High-Speed Window Comparator

A window comparator circuit is used to detect when a signal is between two fixed voltages. The AD8612 can be used to create a high-speed window comparator, as shown in Figure 20. Here, the reference window voltages are set as:

$$V_{HI} = \frac{R2}{R1 + R2} \qquad V_{LO} = \frac{R4}{R3 + R4}$$

The output of the A1 comparator will go high when the input signal exceeds V_{HI}, and the output of A2 will go high only when V_{IN} drops below V_{LO}. When the input voltage is between V_{HI} and V_{LO}, both comparator outputs will be low, turning off both Q1 and Q2, thus driving V_{OUT} to a high state. If the input signal goes outside of the reference voltage window, then V_{OUT} will go low.

To ensure a minimum of switching delay, high-speed transistors are recommended for Q1 and Q2. Using the AD8612 with 2N3960 transistors provides a total propagation delay from V_{IN} to V_{OUT} of less than 10 ns.

Table III. Window Comparator Output States

V_{OUT}	Input Voltage
= 200 mV	$V_{IN} < V_{LO}$
+ 5 V	$V_{LO} < V_{IN} < V_{HI}$
= 200 mV	$V_{IN} > V_{HI}$

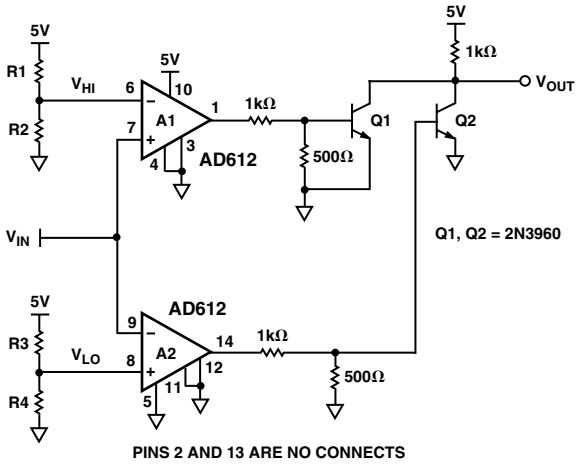


Figure 20. A High-Speed Window Comparator

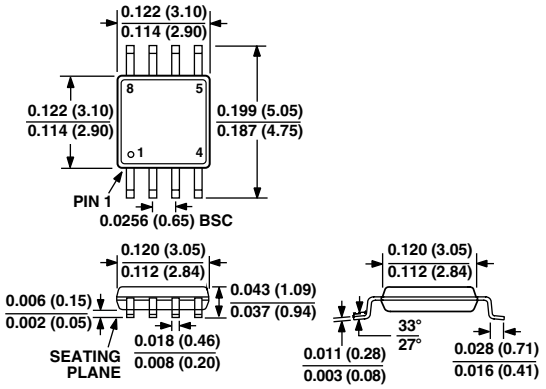
```
SPICE Model
* AD8611 SPICE Macro-Model Typical Values
* 1/2000, Ver. 1.0
* TAM / ADSC
*
* Node assignments
*                     non-inverting input
*                     |      inverting input
*                     |      |      positive supply
*                     |      |      |      negative supply
*                     |      |      |      |      Latch
*                     |      |      |      |      |      DGND
*                     |      |      |      |      |      |      Q
*                     |      |      |      |      |      |      |      QNOT
*                     |      |      |      |      |      |      |      |
.SUBCKT AD8611        1      2      99     50     80     51     45     65
*
* INPUT STAGE
*
*
Q1     4  3 5 PIX
Q2     6  2 5 PIX
IBIAS 99  5 800E-6
RC1    4 50 1E3
RC2    6 50 1E3
CL1    4  6 3E-13
CIN    1  2 3E-12
VCM1  99  7 DC 1.9
D1     5  7 DX
EOS    3  1 POLY(1) (31,98) 1E-3 1
*
* Reference Voltages
*
EREF  98 0 POLY(2) (99,0) (50,0) 0 0.5 0.5
RREF  98 0 100E3
*
* CMRR=66dB, ZERO AT 1kHz
*
ECM1 30 98 POLY(2) (1,98) (2,98) 0 0.5 0.5
RCM1 30 31 10E3
RCM2 31 98 5
CCM1 30 31 15.9E-9
*
* Latch Section
*
```

```
RX 80 51 100E3
E1 10 98 (4,6) 1
S1 10 11 (80,51) SLATCH1
R2 11 12 1
C3 12 98 5.4E-12
E2 13 98 (12,98) 1
R3 12 13 500
*
* Power Supply Section
*
GSY1 99 52 POLY(1) (99,50) 4E-3 -2.6E-4
GSY2 52 50 POLY(1) (99,50) 3.7E-3 -.6E-3
RSY  52 51 10
*
* Gain Stage Av=250 fp=100MHz
*
G2 98 20 (12,98) 0.25
R1 20 98 1000
C1 20 98 10E-13
E3 97  0 (99,0) 1
E4 52  0 (51,0) 1
V1 97 21 DC 0.8
V2 22 52 DC 0.8
D2 20 21 DX
D3 22 20 DX
*
* Q Output
*
Q3  99 41 46 NOX
Q4  47 42 51 NOX
RB1 43 41 2000
RB2 40 42 2000
CB1 99 41 0.5E-12
CB2 42 51 1E-12
RO1 46 44 1
D4  44 45 DX
RO2 47 45 500
EO1 97 43 (20,51) 1
EO2 40 51 (20,51) 1
*
* Q NOT Output
*
Q5  99 61 66 NOX
Q6  67 62 51 NOX
RB3 63 61 2000
RB4 60 62 2000
CB3 99 61 0.5E-12
CB4 62 51 1E-12
RO3 66 64 1
D5  64 65 DX
RO4 67 65 500
EO3 63 51 (20,51) 1
EO4 97 60 (20,51) 1
*
* MODELS
*
.MODEL PIX PNP(BF=100,IS=1E-16)
.MODEL NOX NPN(BF=100,VAF=130,IS=1E-14)
.MODEL DX D(IS=1E-14)
.MODEL SLATCH1 VSWITCH(ROFF=1E6,RON=500,
+VOFF=2.1,VON=1.4)
.ENDS AD8611
```

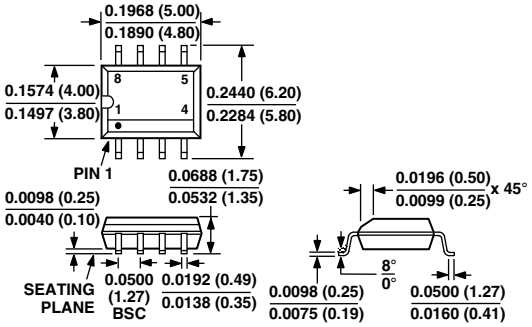
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

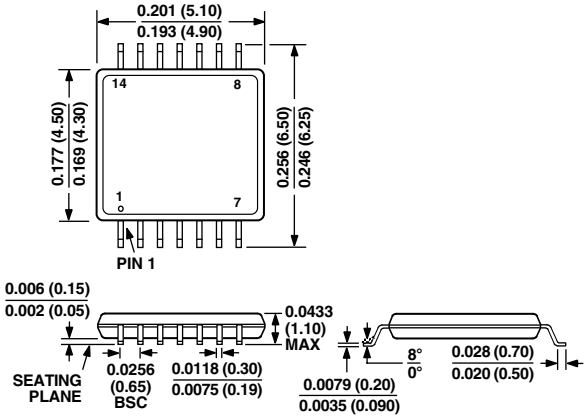
8-Lead micro SO
(RM-8)



8-Lead Small Outline IC
(SO-8)



14-Lead Thin Shrink Small Outline
(RU-14)



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