

128K x 32, 128K x 36 SYNCHRONOUS FLOW-THROUGH STATIC RAM

FEATURES

- Fast access times: 7.5 ns, 8 ns, 8.5 ns, 10 ns, and 12 ns
- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data inputs and control signals
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin LQFP and 119-pin PBGA package
- Single +3.3V +10%, -5% power supply
- Power-down snooze mode

DESCRIPTION

The *ICSI* IS61SF12832 and IS61SF12836 are high-speed synchronous static RAM designed to provide a burstable, high-performance for high speed networking and communication applications. It is organized as 131,072 words by 32 bits or 36 bits, fabricated with *ICSI*'s advanced CMOS technology. The device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQa, $\overline{BW2}$ controls DQb, $\overline{BW3}$ controls DQc, $\overline{BW4}$ controls DQd, conditioned by $\overline{BWE}$ being LOW. A LOW on $\overline{GW}$ input would cause all bytes to be written.

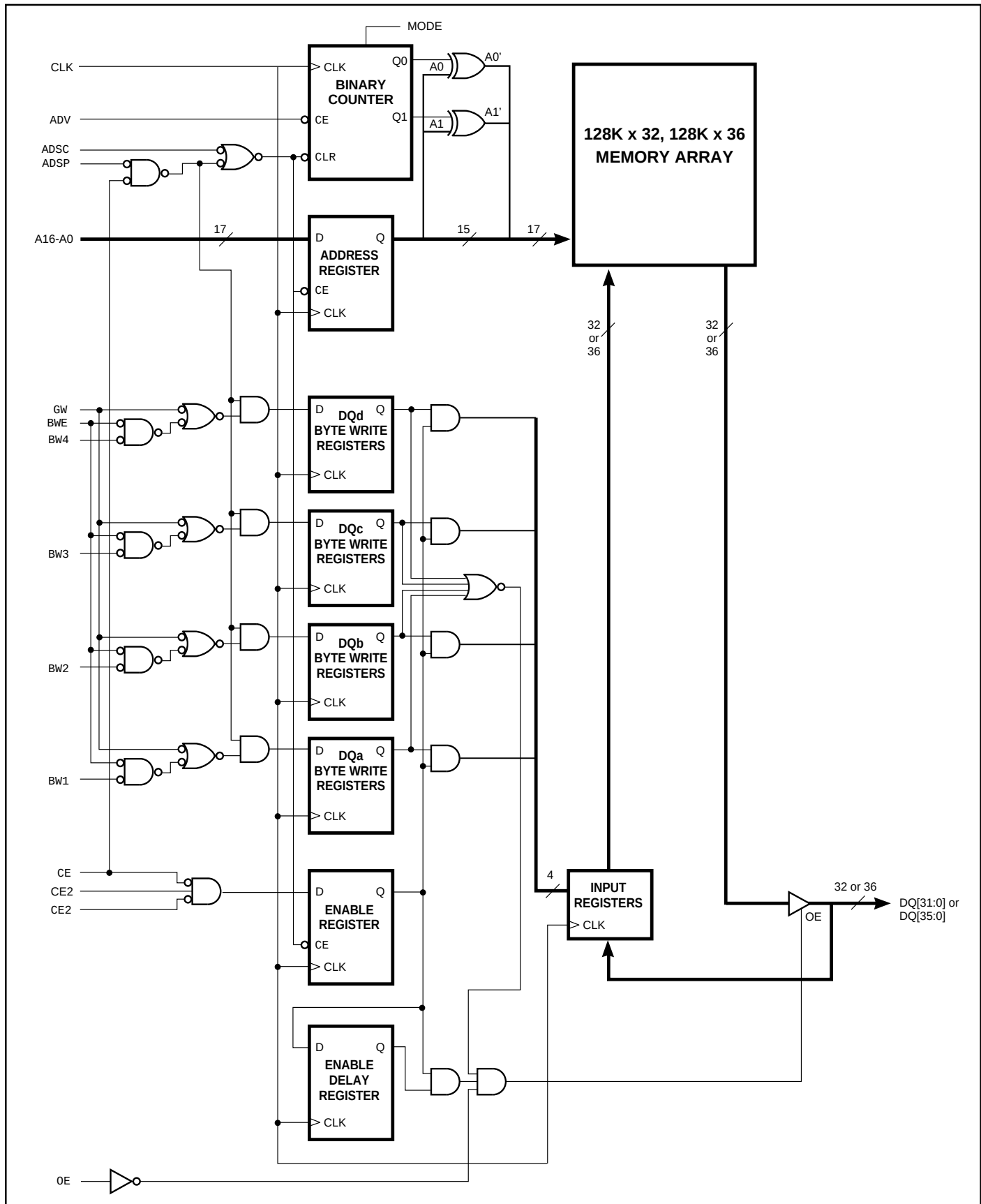
Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally by the IS61SF12832 and controlled by the ADV (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

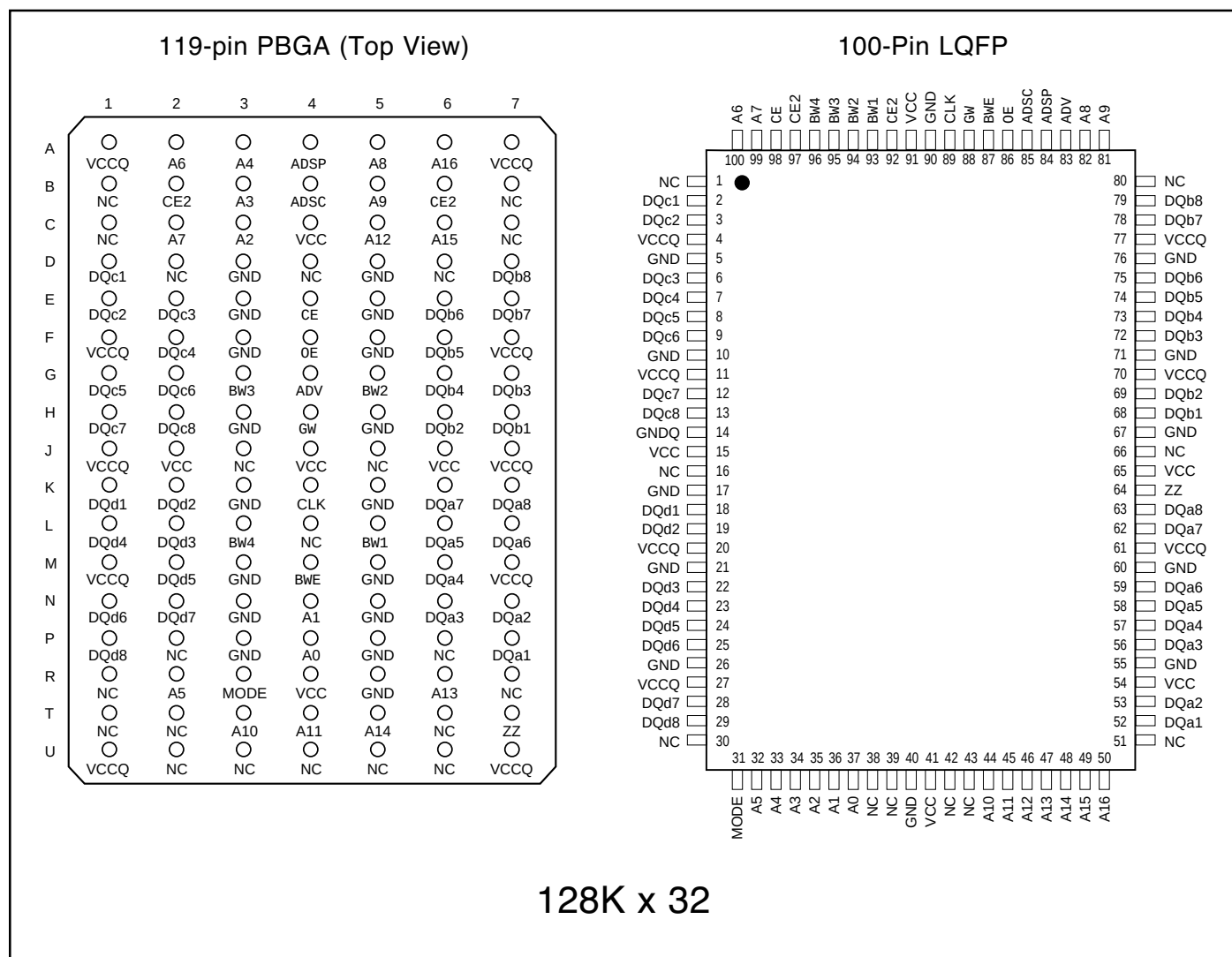
FAST ACCESS TIME

Symbol	Parameter	7.5	8	8.5	10	12	Units
tkQ	Clock Access Time	7.5	8	8.5	10	12	ns
tkC	Cycle Time	8.5	10	11	15	15	ns
	Frenquency	117	100	90	66	66	MHz

BLOCK DIAGRAM



PIN CONFIGURATION

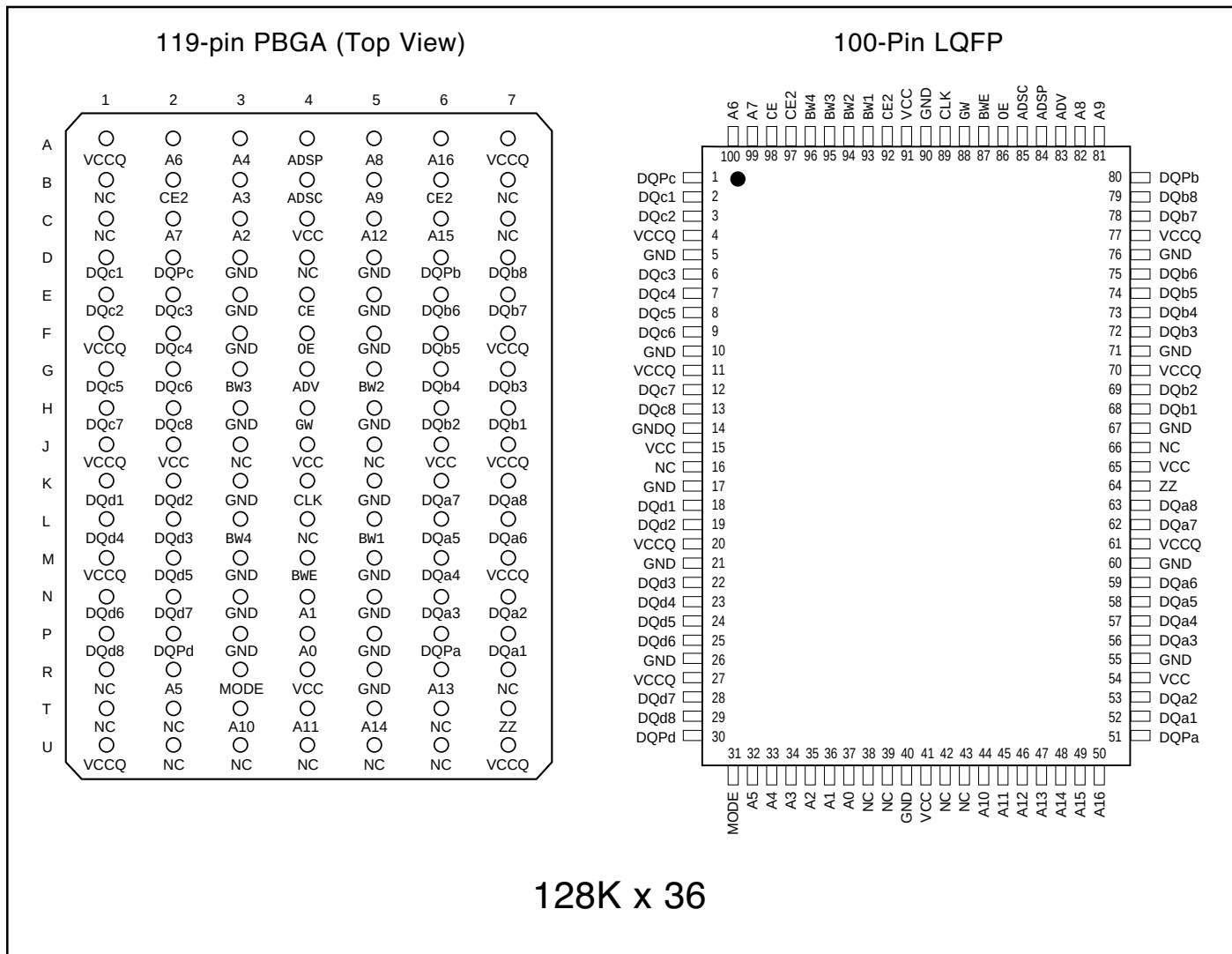


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A16	Synchronous Address Inputs
CLK	Synchronous Clock
ADSP	Synchronous Processor Address Status
ADSC	Synchronous Controller Address Status
ADV	Synchronous Burst Address Advance
BW1-BW4	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable

GW	Synchronous Global Write Enable
CE, CE2, CE2	Synchronous Chip Enable
OE	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply: +3.3V
ZZ	Snooze Enable

PIN CONFIGURATION



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A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A16	Synchronous Address Inputs
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$\overline{\text{ADSP}}$	Synchronous Processor Address Status
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$\overline{\text{BW1-BW4}}$	Synchronous Byte Write Enable
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$\overline{\text{GW}}$	Synchronous Global Write Enable
$\overline{\text{CE}}, \overline{\text{CE2}}, \text{CE2}$	Synchronous Chip Enable
$\overline{\text{OE}}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply: +3.3V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

TRUTH TABLE

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	WRITE	$\overline{OE}$	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	X	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	X	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	High-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	High-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	High-Z
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	High-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	High-Z
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	High-Z

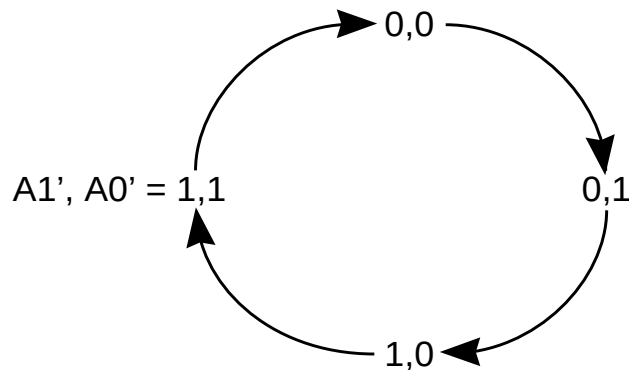
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = VccQ or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
T _{BIAS}	Temperature Under Bias	-40 to +85	°C
T _{STG}	Storage Temperature	-55 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for I/O Pins	-0.5 to V _{CCQ} + 0.3	V
V _{IN}	Voltage Relative to GND for for Address and Control Inputs	-0.5 to V _{CC} + 0.5	V
V _{CC}	Voltage on Vcc Supply Relative to GND	-0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V +10%, -5%
Industrial	-40°C to +85°C	3.3V +10%, -5%

DC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -4.0 mA	2.4	–	V
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA	–	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CCQ} ⁽²⁾	Com. Ind.	-2 5	μA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CCQ} , $\overline{OE} = V_{IH}$	Com. Ind.	-2 5	μA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		7.5 Max.	8 Max.	8.5 Max.	10 Max.	12 Max.	Unit
I _{CC}	AC Operating Supply Current	Device Selected, All Inputs = V _{IL} or V _{IH} $\overline{OE} = V_{IH}$, V _{CC} = Max. Cycle Time ≥ t _{kc} min.	Com. Ind.	270 –	250 260	230 240	190 200	170 180	mA
I _{SB}	Standby Current	Device Deselected, V _{CC} = Max., All Inputs = V _{IH} or V _{IL} CLK Cycle Time ≥ t _{kc} min.	Com. Ind.	50 –	50 60	50 60	50 60	50 60	mA
I _{ZZ}	Power-down Mode Current	ZZ = V _{CCQ} Clock Running All Inputs ≤ GND + 0.2V or ≥ V _{CC} - 0.2V	Com. Ind.	10 –	10 15	10 15	10 15	10 15	mA

Notes:

1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to V_{CCQ}.
2. The MODE pin should be tied to V_{CC} or GND. It exhibits ±10 μA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{CC} - 0.2V.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

- Notes:
- 1. Tested initially and after any design or process changes that may affect these parameters.
 - 2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

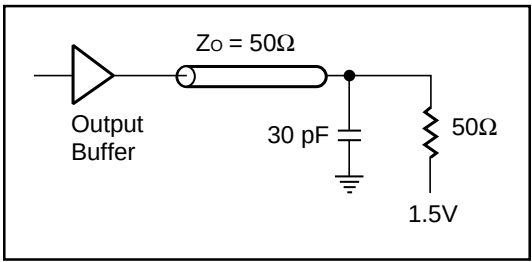


Figure 1

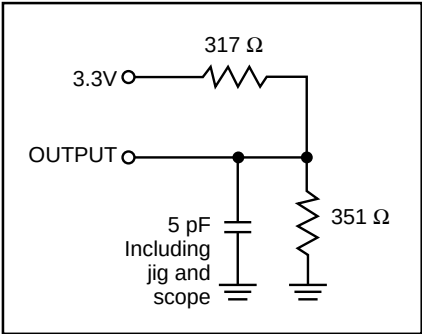


Figure 2

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	7.5		8		8.5		10		12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}	Clock Frequency	–	117	–	100	–	90	–	66	–	66	MHz
t _{KC}	Cycle Time	8.5	–	10	–	11	–	15	–	15	–	ns
t _{KH}	Clock High Time	3	–	4	–	4.5	–	4.5	–	4.5	–	ns
t _{KL}	Clock Low Time	3	–	4	–	4.5	–	4.5	–	4.5	–	ns
t _{KQ}	Clock Access Time	–	7.5	–	8	–	8.5	–	10	–	12	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	2	–	2	–	2	–	2	–	2	–	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	–	0	–	0	–	0	–	0	–	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	2	3.5	2	3.5	2	3.5	2	3.5	2	3.5	ns
t _{OEQ}	Output Enable to Output Valid	–	3.5	–	3.5	–	3.5	–	3.5	–	5	ns
t _{OELZ} ^(1,2)	Output Enable to Output Low-Z	0	–	0	–	0	–	0	–	0	–	ns
t _{OEHZ} ^(1,2)	Output Disable to Output High-Z	–	3.5	–	3.5	–	3.5	–	3.5	–	3.5	ns
t _{AS}	Address Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{SS}	Address Status Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{WS}	Write Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{CES}	Chip Enable Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{AVS}	Address Advance Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{AH}	Address Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{SH}	Address Status Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{WH}	Write Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{CEH}	Chip Enable Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{AVH}	Address Advance Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns

Notes:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Tested with load in Figure 1.

The timing diagram for the AD9080 shows the following signals and their timing characteristics:

- CLK**: Clock signal with period t_{KH} and duty cycle t_{KL} .
- ADSP**: Address Strobe (Pulse) signal. $\overline{ADSP}$ is blocked by $\overline{CE}$ inactive. Timing parameters: t_{SS} (setup), t_{SH} (hold).
- ADSC**: Address Strobe (Clock) signal. Timing parameters: t_{SS} (setup), t_{SH} (hold).
- ADV**: Address Valid signal. Timing parameters: t_{AS} (setup), t_{AH} (hold).
- A16-A0**: Address bus. Operations: RD1, WR1, RD2, RD3.
- GW**: Global Write signal. Timing parameters: t_{WS} (setup), t_{WH} (hold).
- BWE**: Burst Write Enable signal. Timing parameters: t_{WS} (setup), t_{WH} (hold).
- BW4-BW1**: Burst Write Enable signal. Operation: WR1. Timing parameters: t_{WS} (setup), t_{WH} (hold).
- CE**: Chip Enable signal. $\overline{CE}$ Masks $\overline{ADSP}$. Timing parameters: t_{CES} (setup), t_{CEH} (hold).
- CE2**: Chip Enable 2 signal. CE2 and $\overline{CE2}$ only, sampled with $\overline{ADSP}$ or $\overline{ADSC}$. Timing parameters: t_{CES} (setup), t_{CEH} (hold).
- CE2**: Chip Enable 2 signal. Unselected with $\overline{CE2}$. Timing parameters: t_{CES} (setup), t_{CEH} (hold).
- OE**: Output Enable signal. Timing parameters: t_{OEQ} (setup), t_{OEZ} (hold).
- DATAOUT**: Data Output signal. Operations: 1a, 2a, 2b, 2c, 2d. Timing parameters: t_{OELZ} (setup), t_{KQLZ} (hold), t_{KQ} (hold), t_{KQX} (hold), t_{KQHZ} (hold).
- DATAIN**: Data Input signal. Operation: 1a. Timing parameters: t_{DS} (setup), t_{DH} (hold).

The diagram is divided into four main sections: Single Read, Single Write, Burst Read, and Unselected.

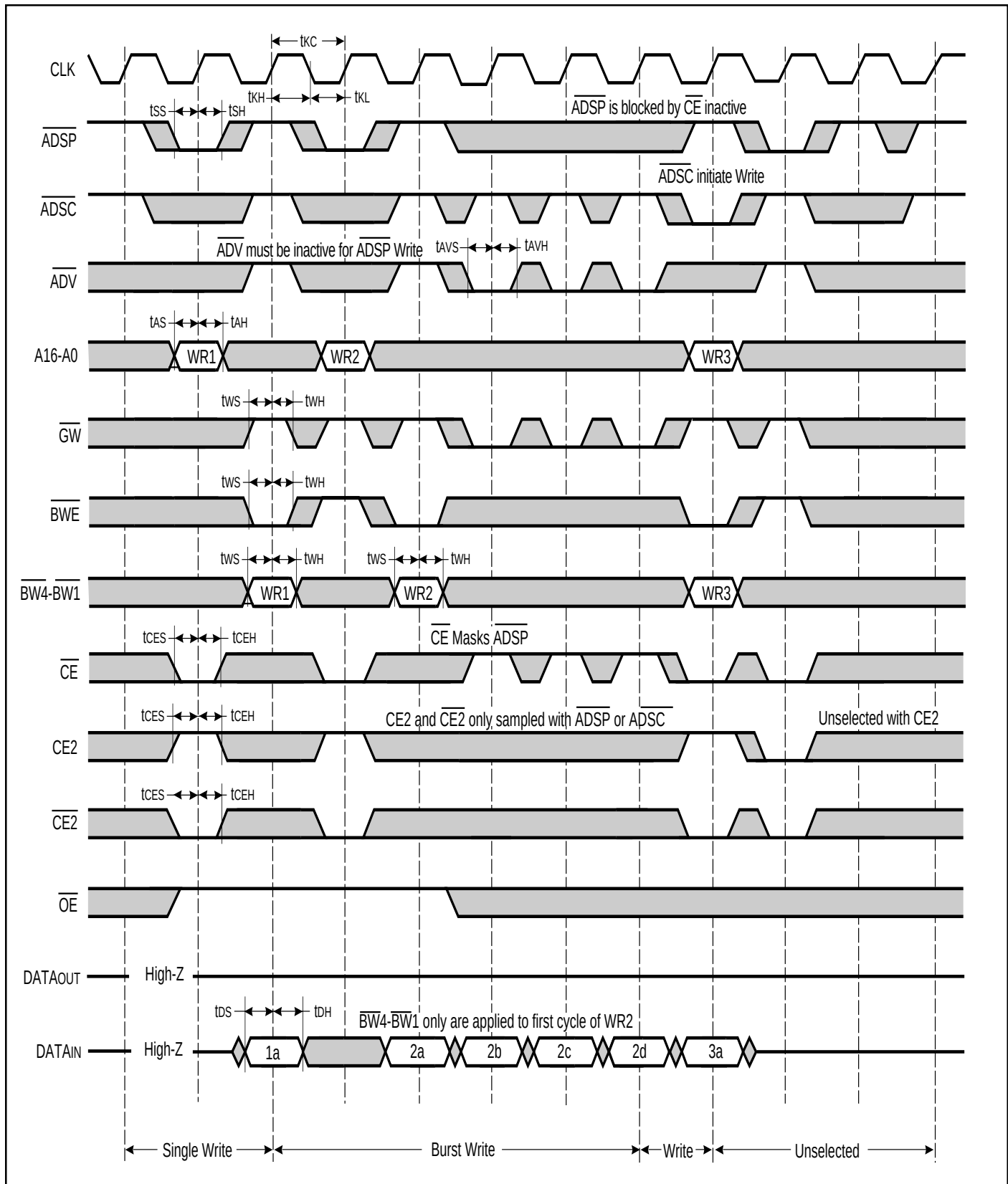
WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	7.5		8		8.5		10		12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{kc}	Cycle Time	8.5	–	10	–	11	–	15	–	15	–	ns
t _{kH}	Clock High Time	3	–	4	–	4.5	–	4.5	–	4.5	–	ns
t _{kL}	Clock Low Time	3	–	4	–	4.5	–	4.5	–	4.5	–	ns
t _{as}	Address Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{ss}	Address Status Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{ws}	Write Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{ds}	Data In Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{ces}	Chip Enable Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{avs}	Address Advance Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{aH}	Address Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{sH}	Address Status Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{dH}	Data In Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{wH}	Write Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{ceH}	Chip Enable Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{avH}	Address Advance Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns

Note:

1. Tested with load in Figure 1.

WRITE CYCLE TIMING



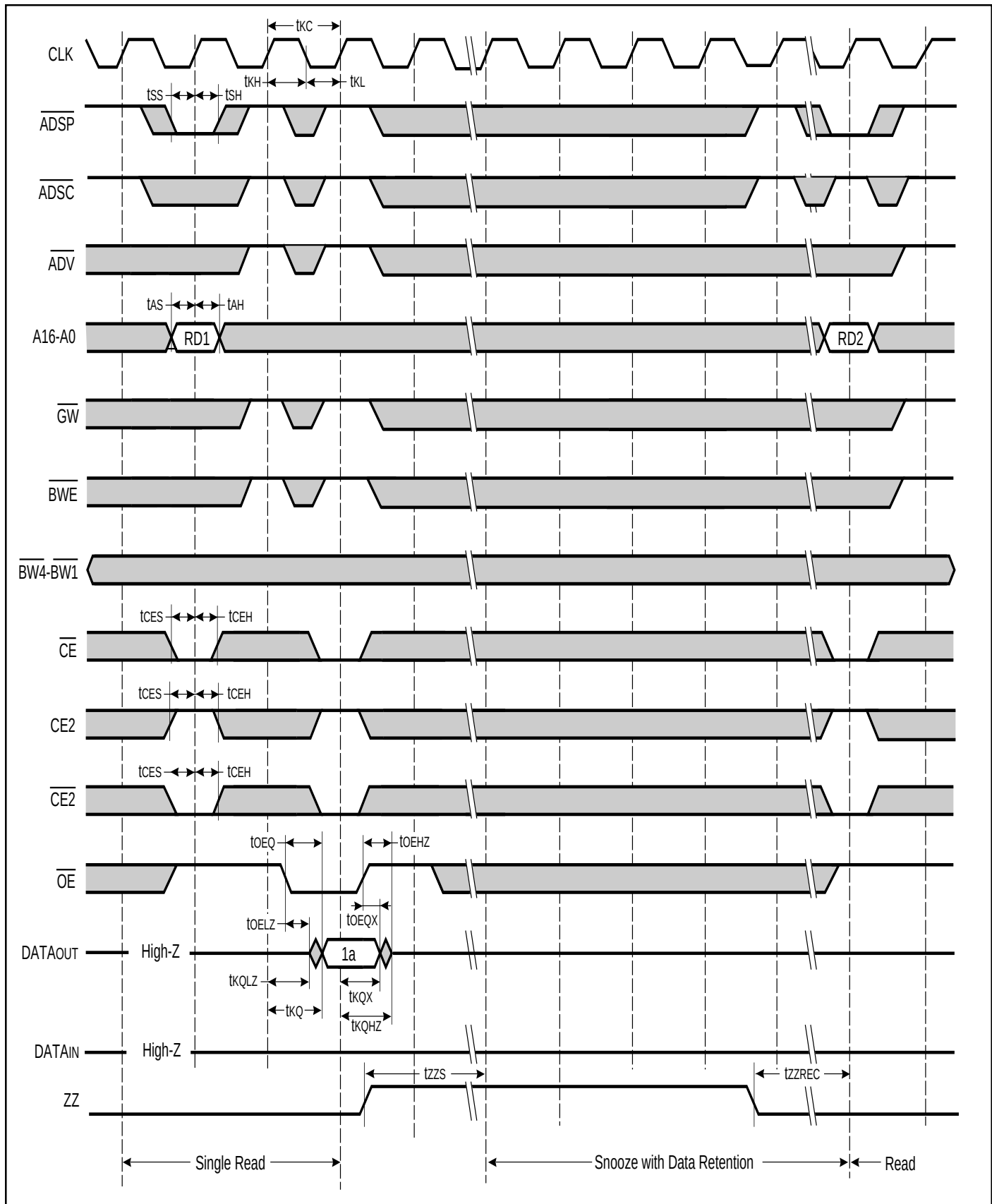
SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	7.5		8		8.5		10		12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{kc}	Cycle Time	8.5	–	10	–	11	–	15	–	15	–	ns
t _{kH}	Clock High Time	3	–	4	–	4.5	–	4.5	–	4.5	–	ns
t _{kL}	Clock Low Time	3	–	4	–	4.5	–	4.5	–	4.5	–	ns
t _{kQ}	Clock Access Time	–	7.5	–	8	–	8.5	–	10	–	12	ns
t _{kQX} ⁽¹⁾	Clock High to Output Invalid	2	–	2	–	2	–	2	–	2	–	ns
t _{kQLZ} ^(1,2)	Clock High to Output Low-Z	0	–	0	–	0	–	0	–	0	–	ns
t _{kQHZ} ^(1,2)	Clock High to Output High-Z	2	3.5	2	3.5	2	3.5	2	3.5	2	3.5	ns
t _{oEQ}	Output Enable to Output Valid	–	3.5	–	3.5	–	3.5	–	3.5	–	5	ns
t _{oELZ} ^(1,2)	Output Enable to Output Low-Z	0	–	0	–	0	–	0	–	0	–	ns
t _{oEHZ} ^(1,2)	Output Disable to Output High-Z	–	3.5	–	3.5	–	3.5	–	3.5	–	3.5	ns
t _{as}	Address Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{ss}	Address Status Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{ces}	Chip Enable Setup Time	2	–	2	–	2	–	2	–	4	–	ns
t _{aH}	Address Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{sH}	Address Status Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{ceH}	Chip Enable Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	1.5	–	ns
t _{zZS}	ZZ Standby	2	–	2	–	2	–	2	–	2	–	cyc
t _{zZREC}	ZZ Recovery	2	–	2	–	2	–	2	–	2	–	cyc

Notes:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Tested with load in Figure 1.

SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Order Part Number	Package
7.5	IS61SF12832-7.5TQ	14*20*1.4mm LQFP
	IS61SF12832-7.5B	14*22mm PBGA
8	IS61SF12832-8TQ	14*20*1.4mm LQFP
	IS61SF12832-8B	14*22mm PBGA
8.5	IS61SF12832-8.5TQ	14*20*1.4mm LQFP
	IS61SF12832-8.5B	14*22mm PBGA
10	IS61SF12832-10TQ	14*20*1.4mm LQFP
	IS61SF12832-10B	14*22mm PBGA
12	IS61SF12832-12TQ	14*20*1.4mm LQFP
	IS61SF12832-12B	14*22mm PBGA

Industrial Range: -40°C to +85°C

Frequency	Order Part Number	Package
8	IS61SF12832-8TQI	14*20*1.4mm LQFP
8.5	IS61SF12832-8.5TQI	14*20*1.4mm LQFP
10	IS61SF12832-10TQI	14*20*1.4mm LQFP
12	IS61SF12832-12TQI	14*20*1.4mm LQFP

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Order Part Number	Package
7.5	IS61SF12836-7.5TQ	14*20*1.4mm LQFP
	IS61SF12836-7.5B	14*22mm PBGA
8	IS61SF12836-8TQ	14*20*1.4mm LQFP
	IS61SF12836-8B	14*22mm PBGA
8.5	IS61SF12836-8.5TQ	14*20*1.4mm LQFP
	IS61SF12836-8.5B	14*22mm PBGA
10	IS61SF12836-10TQ	14*20*1.4mm LQFP
	IS61SF12836-10B	14*22mm PBGA
12	IS61SF12836-12TQ	14*20*1.4mm LQFP
	IS61SF12836-12B	14*22mm PBGA

Industrial Range: -40°C to +85°C

Frequency	Order Part Number	Package
8	IS61SF12836-8TQI	14*20*1.4mm LQFP
8.5	IS61SF12836-8.5TQI	14*20*1.4mm LQFP
10	IS61SF12836-10TQI	14*20*1.4mm LQFP
12	IS61SF12836-12TQI	14*20*1.4mm LQFP



Integrated Circuit Solution Inc.

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