
2SB1002

Silicon PNP Epitaxial

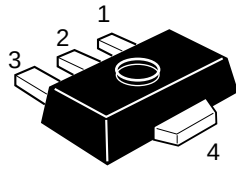
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Application

- Low frequency power amplifier
- Complementary pair with 2SD1368

Outline

UPAK



1. Base
2. Collector
3. Emitter
4. Collector (Flange)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Collector to base voltage	V_{CBO}	-70	V
Collector to emitter voltage	V_{CEO}	-50	V
Emitter to base voltage	V_{EBO}	-6	V
Collector current	I_C	-1	A
Collector peak current	$i_{C(peak)}^{*1}$	-1.5	A
Collector power dissipation	P_C^{*2}	1	W
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

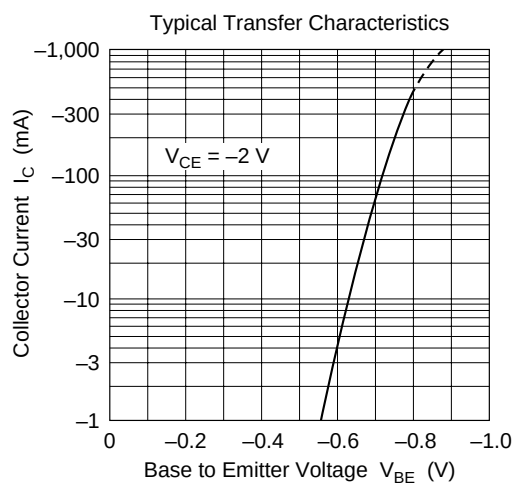
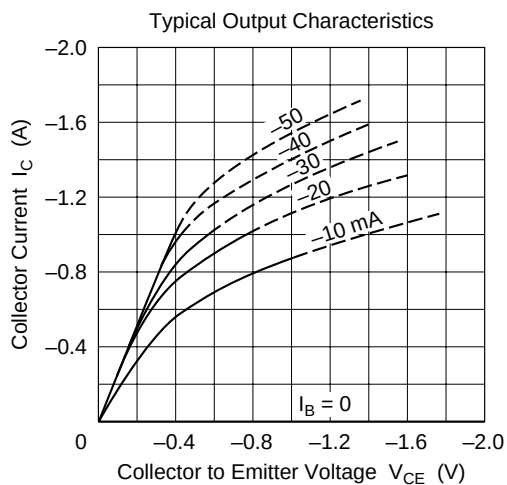
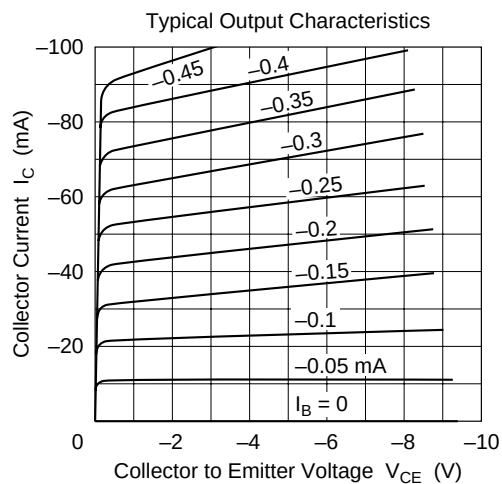
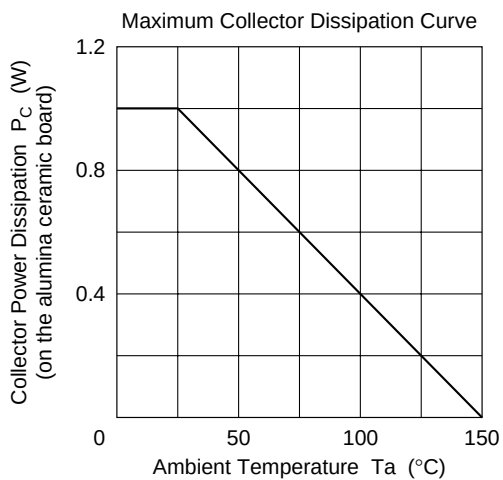
Notes: 1. $PW \leq 10$ ms, Duty cycle $\leq 20\%$
2. Value on the alumina ceramic board ($12.5 \times 20 \times 0.7$ mm)

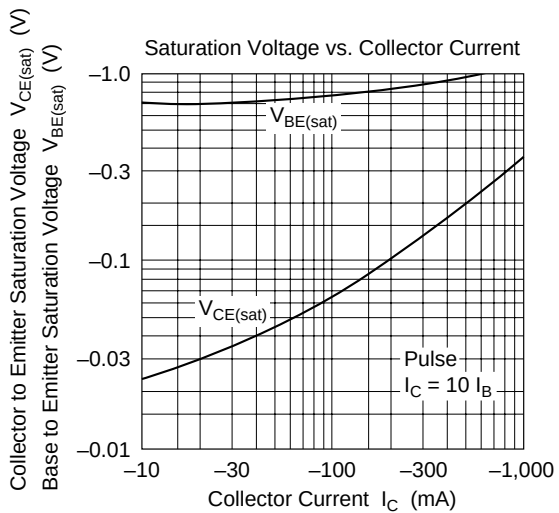
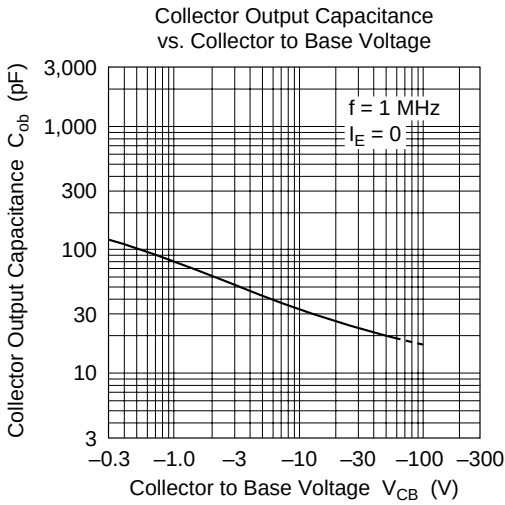
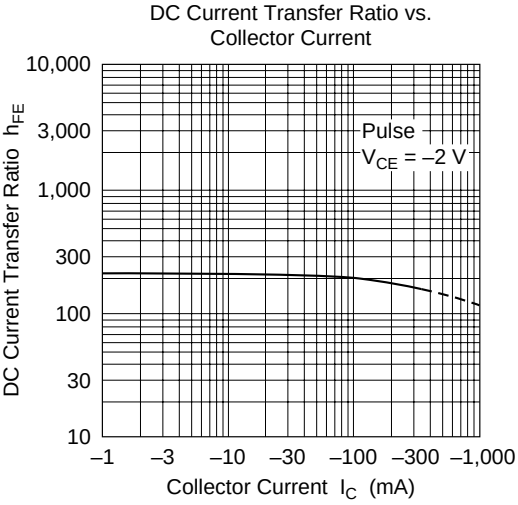
Electrical Characteristics (Ta = 25°C)

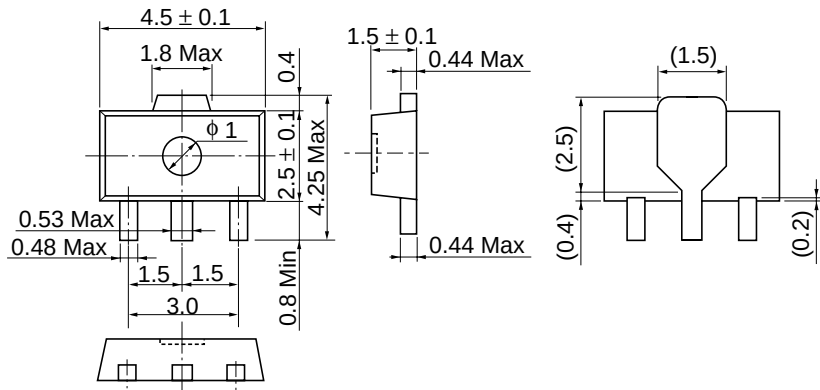
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Collector to base breakdown voltage	$V_{(BR)CBO}$	-70	—	—	V	$I_C = -10 \mu A, I_E = 0$
Collector to emitter breakdown voltage	$V_{(BR)CEO}$	-50	—	—	V	$I_C = -1$ mA, $R_{BE} = \infty$
Emitter to base breakdown voltage	$V_{(BR)EBO}$	-6	—	—	V	$I_E = -10 \mu A, I_C = 0$
Collector cutoff current	I_{CBO}	—	—	-0.1	μA	$V_{CB} = -50$ V, $I_E = 0$
Emitter cutoff current	I_{EBO}	—	—	-0.1	μA	$V_{EB} = -4$ V, $I_C = 0$
DC current transfer ratio	h_{FE}^{*1}	100	—	320		$V_{CE} = -2$ V, $I_C = -0.1$ A
Collector to emitter saturation voltage	$V_{CE(sat)}$	—	—	-0.6	V	$I_C = -1$ A, $I_B = -0.1$ A (Pulse test)
Base to emitter saturation voltage	$V_{BE(sat)}$	—	—	-1.2	V	$I_C = -1$ A, $I_B = -0.1$ A (Pulse test)
Gain bandwidth product	f_T	—	150	—	MHz	$V_{CE} = -2$ V, $I_C = -10$ mA (Pulse test)
Collector output capacitance	C_{ob}	—	35	—	pF	$V_{CB} = -10$ V, $I_E = 0$, $f = 1$ MHz

Note: 1. The 2SB1002 is grouped by h_{FE} as follows.

Mark	CH	CJ
h_{FE}	100 to 200	160 to 320







Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.050 g

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