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# 2SK1773

Silicon N-Channel MOS FET

# HITACHI

ADE-208-1319 (Z)  
1st. Edition  
Mar. 2001

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## Application

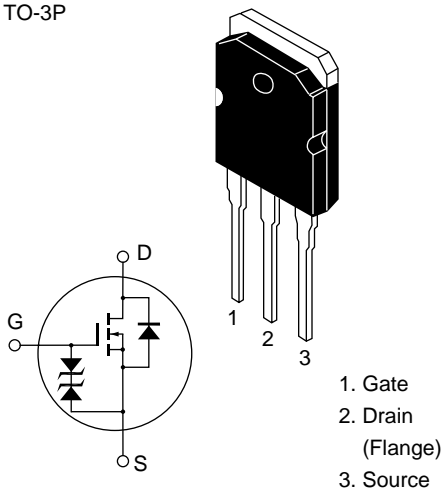
High speed power switching

## Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter

## Outline

TO-3P



**Absolute Maximum Ratings** ( $T_a = 25^\circ\text{C}$ )

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	$V_{\text{DSS}}$	1000	V
Gate to source voltage	$V_{\text{GSS}}$	$\pm 30$	V
Drain current	$I_{\text{D}}$	5	A
Drain peak current	$I_{\text{D(pulse)}}^{*1}$	15	A
Body to drain diode reverse drain current	$I_{\text{DR}}$	5	A
Channel dissipation	$P_{\text{ch}}^{*2}$	100	W
Channel temperature	$T_{\text{ch}}$	150	$^\circ\text{C}$
Storage temperature	$T_{\text{stg}}$	-55 to +150	$^\circ\text{C}$

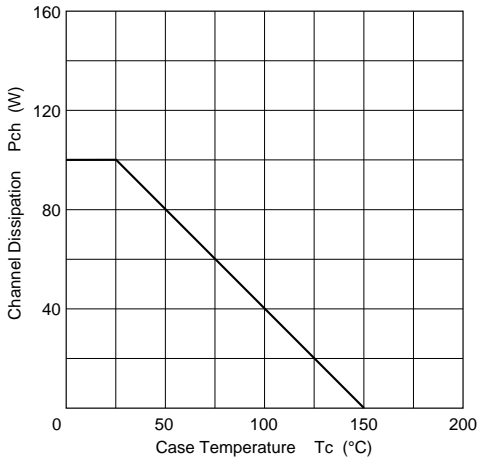
- Notes
1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$
  2. Value at  $T_c = 25^\circ\text{C}$

## Electrical Characteristics (Ta = 25°C)

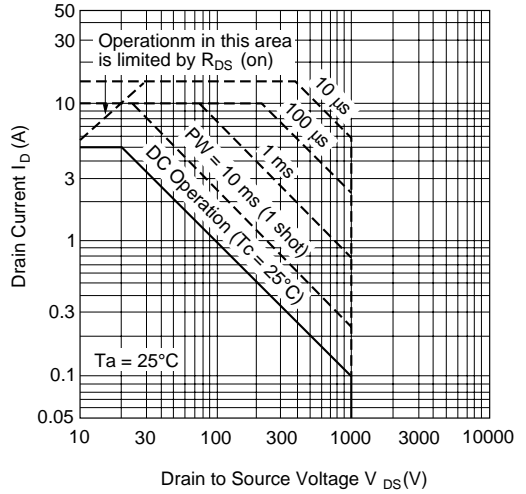
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	1000	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	$I_G = \pm 100 \text{ } \mu\text{A}, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	250	μA	$V_{DS} = 800 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.5	2.0	Ω	$I_D = 3 \text{ A}$ $V_{GS} = 10 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	3.2	5.0	—	S	$I_D = 3 \text{ A}$ $V_{DS} = 20 \text{ V}^{*1}$
Input capacitance	$C_{iss}$	—	1700	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	700	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	315	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	$I_D = 3 \text{ A}$
Rise time	$t_r$	—	110	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	210	—	ns	$R_L = 10 \text{ } \Omega$
Fall time	$t_f$	—	135	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	0.85	—	V	$I_F = 5 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	1050	—	ns	$I_F = 5 \text{ A}, V_{GS} = 0,$ $di_F / dt = 100 \text{ A} / \mu\text{s}$

Note 1. Pulse Test

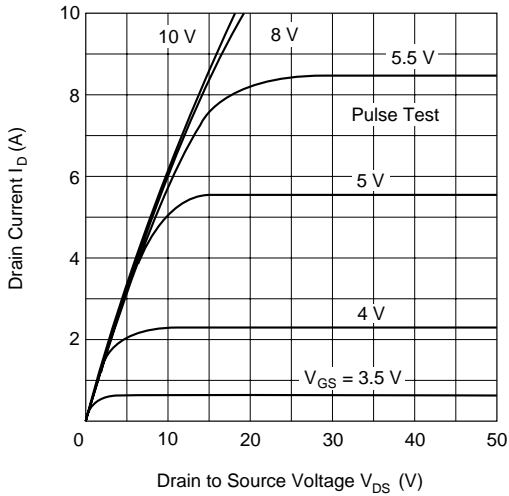
Power vs. Temperature Derating



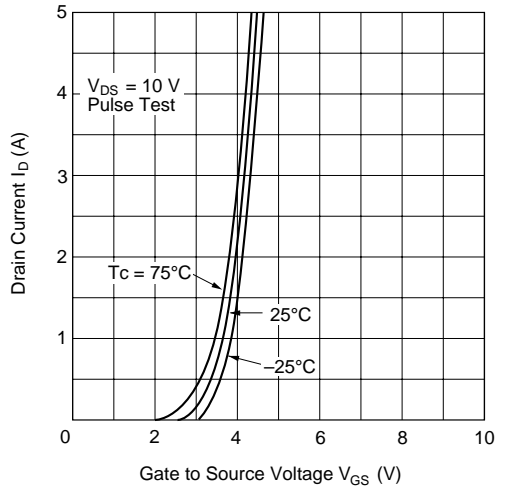
Maximum Safe Operation Area



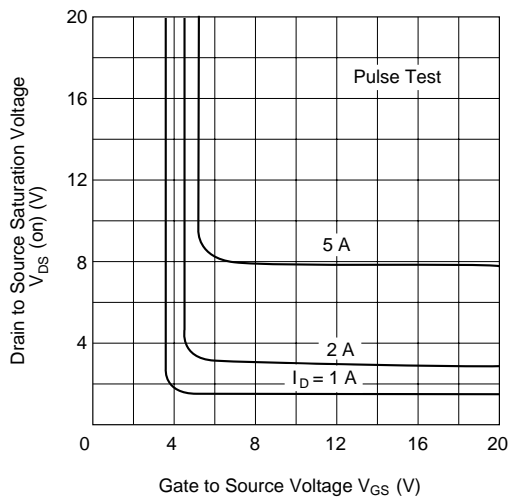
Typical Output Characteristics



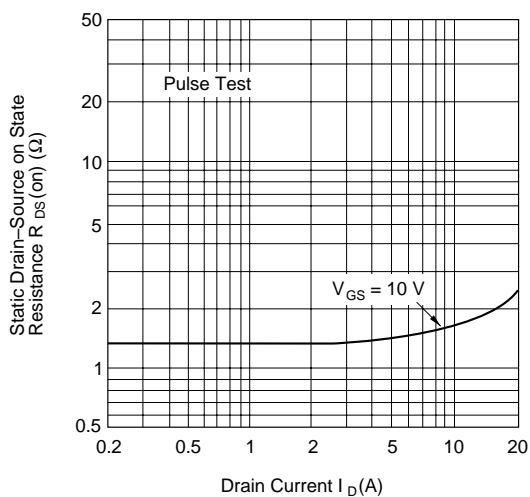
Typical Transfer Characteristics



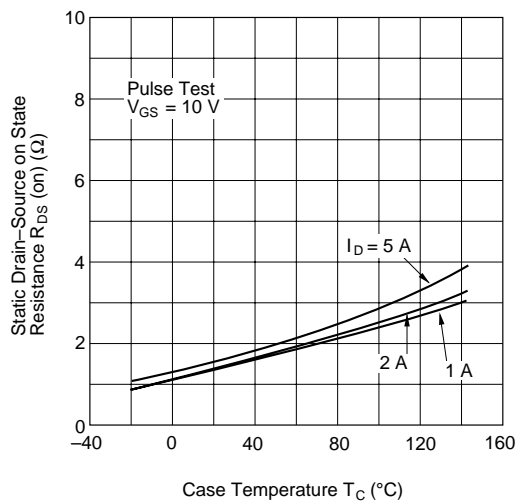
Drain to Source Saturation Voltage vs. Gate to Source Voltage



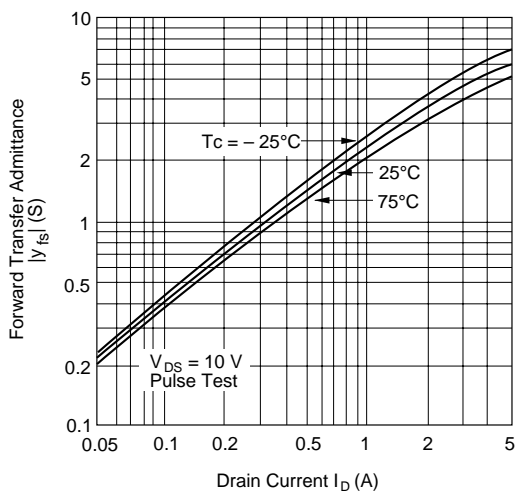
Static Drain to Source on State Resistance vs. Drain Current



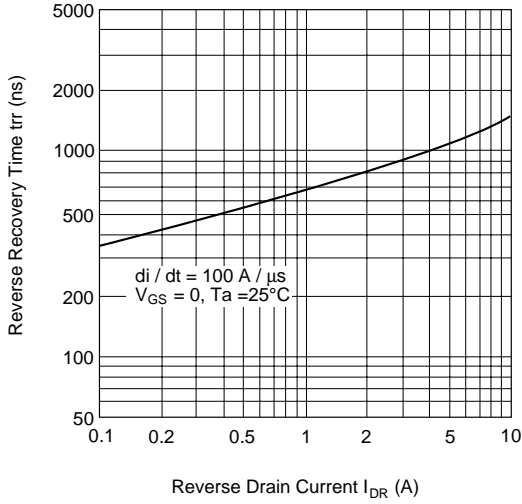
Static Drain to Source on State Resistance vs. Temperature



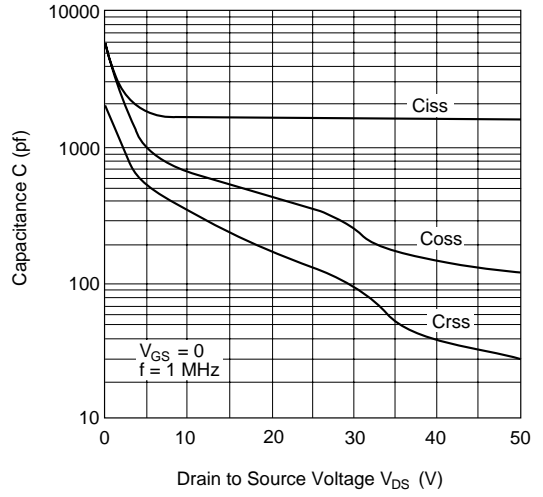
Forward Transfer Admittance vs. Drain Current



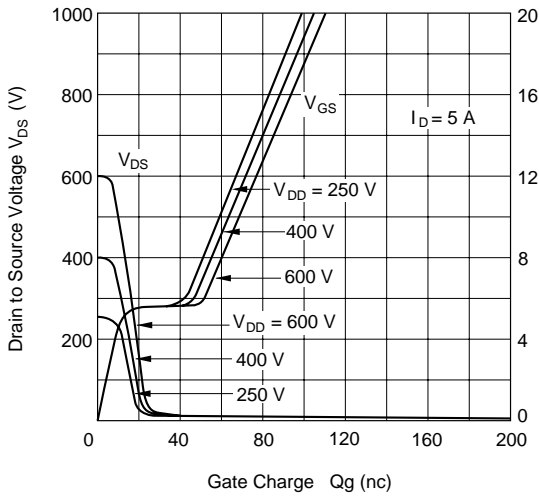
Body to Drain Diode Reverse Recovery Time



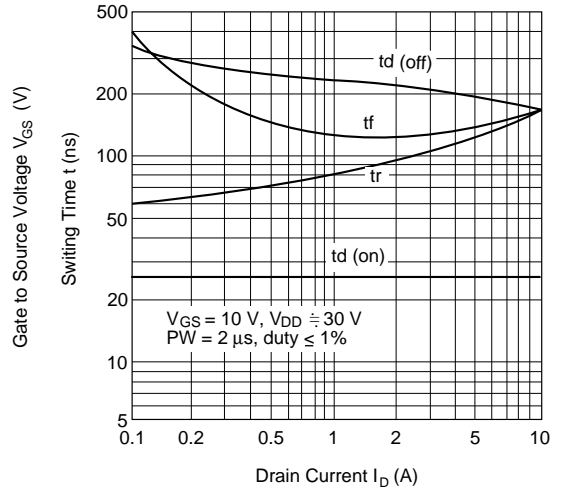
Typical Capacitance vs. Drain to Source Voltage



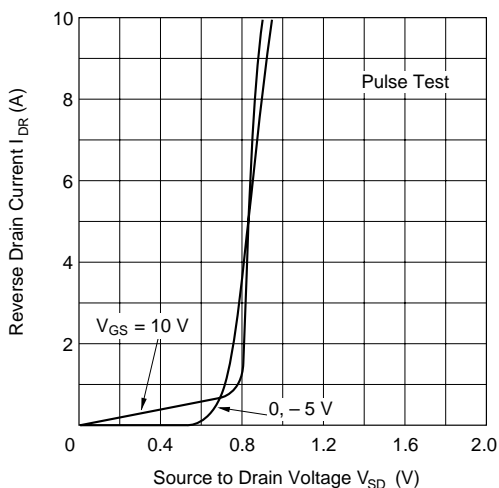
Dynamic Input Characteristics



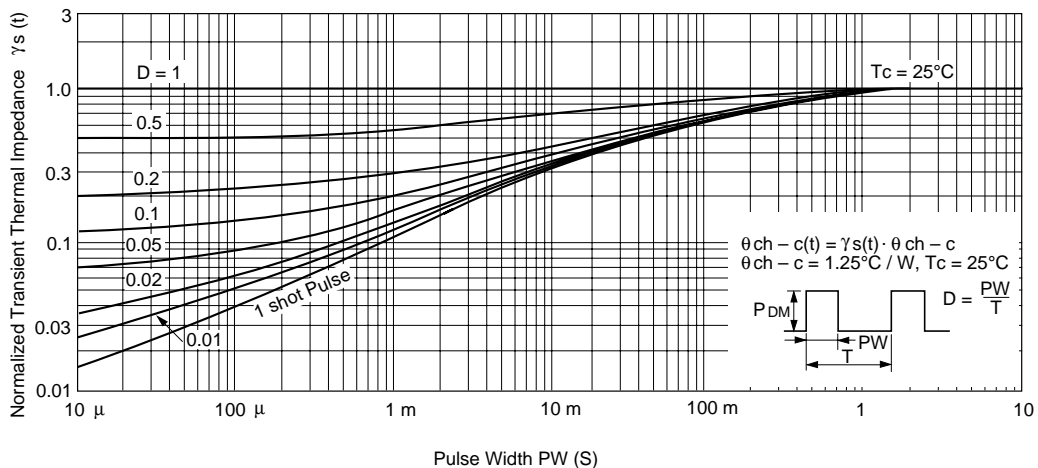
Switching Characteristics



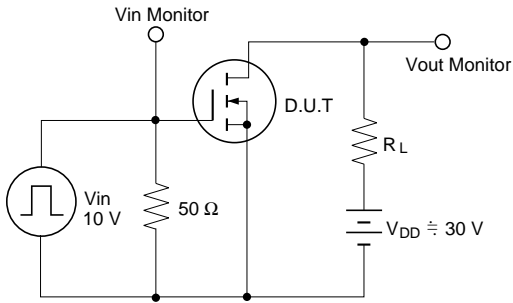
Reverse Drain Current vs. Source to Drain Voltage



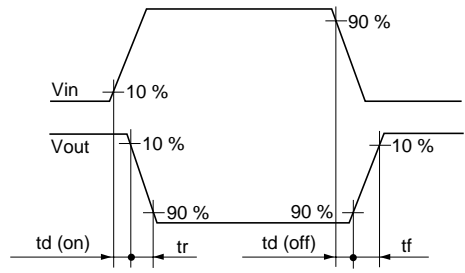
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



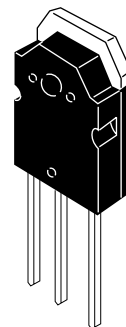
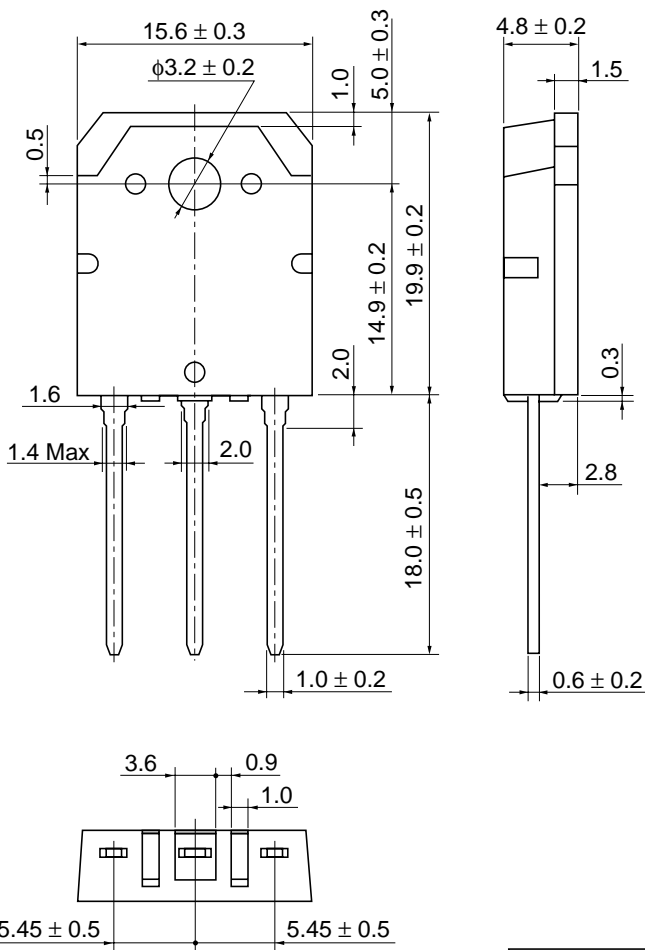
Waveforms



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.0 g

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