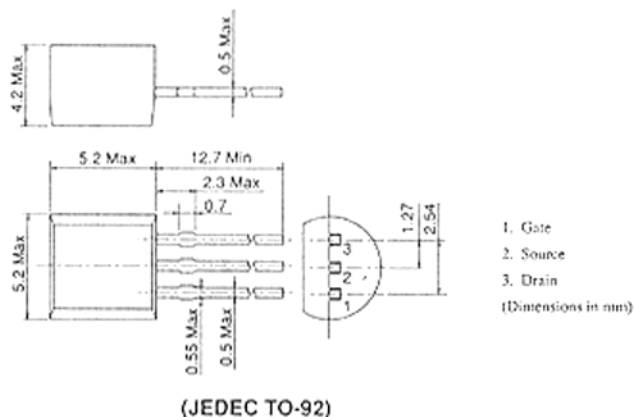


2SK55

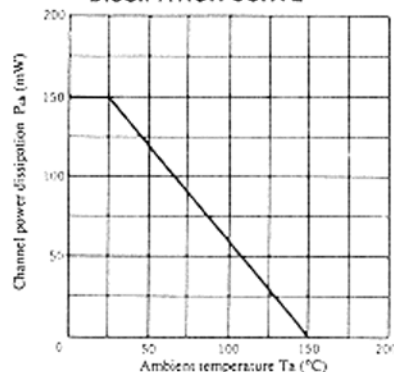
SILICON N-CHANNEL JUNCTION FET
VHF AMPLIFIER, MIXER



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	2SK55	Unit
Gate to drain voltage	V_{GDO}	-18	V
Gate current	I_G	10	mA
Channel power dissipation	P_{ch}	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

MAXIMUM CHANNEL POWER DISSIPATION CURVE



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

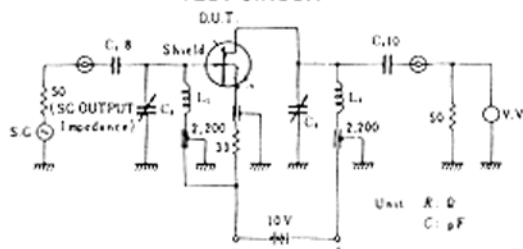
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Gate to drain breakdown voltage	$V_{(BR)GDO}$	$I_G = -100\mu A, I_S = 0$	-18	—	—	V
Gate cutoff current	I_{GSS}	$V_{GS} = -0.5V, V_{DS} = 0$	—	—	-10	nA
Drain current	I_{DSS}^*	$V_{DS} = 10V, V_{GS} = 0$	3	—	14	mA
Gate to source breakdown voltage	$V_{GS(off)}$	$V_{DS} = 10V, I_D = 10\mu A$	-0.3	—	-5.5	V
Forward transfer admittance	$ y_{fs} $	$V_{DS} = 10V, V_{GS} = 0, f = 1kHz$	3	8	—	mS
Input capacitance	C_{is}	$V_{DS} = 10V, V_{GS} = 0, f = 1MHz$	—	3	—	pF
Reverse transfer capacitance	C_{rs}	$V_{DS} = 10V, V_{GS} = 0, f = 1MHz$	—	0.4	0.6	pF
Power gain	PG	$V_{DD} = 10V, R_S = 33\Omega, f = 100MHz$	—	18	—	dB
Noise figure	NF		—	2.0	3.5	dB

* The 2SK55 is grouped by I_{DSS} as follows.

D	E
3 to 2mA	6 to 14mA

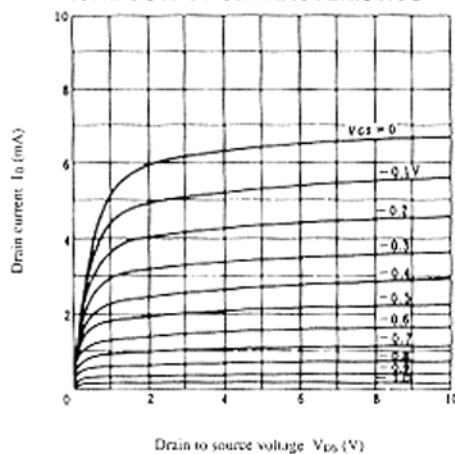
2SK55

POWER GAIN AND NOISE FIGURE TEST CIRCUIT

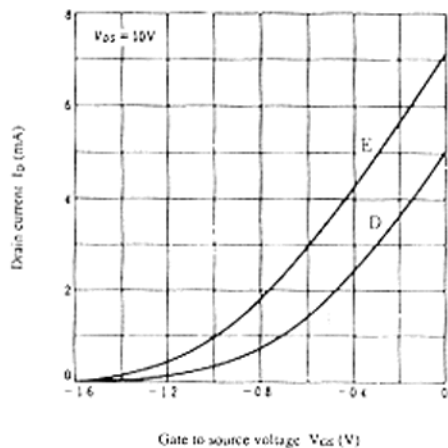


- C_1, C_2 : 30pF max. Variable Air
- L_1 : 3T 1.0mm Copper Ribbon, Tin plated 10mm inside dia. 5.0mm pitch.
- L_2 : 3.5T 1.0mm Copper Ribbon, Tin plated 10mm inside dia. 5.0mm pitch.

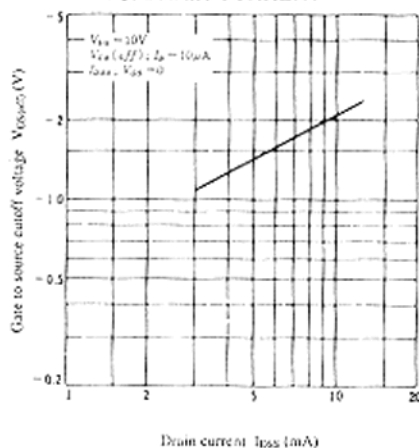
TYPICAL OUTPUT CHARACTERISTICS



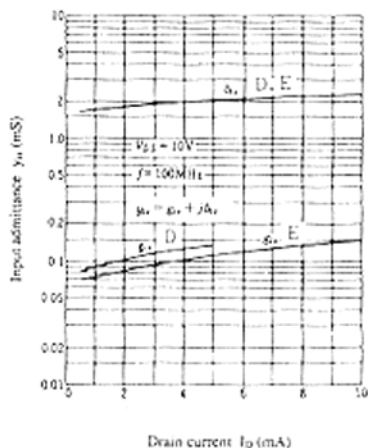
TYPICAL TRANSFER CHARACTERISTICS



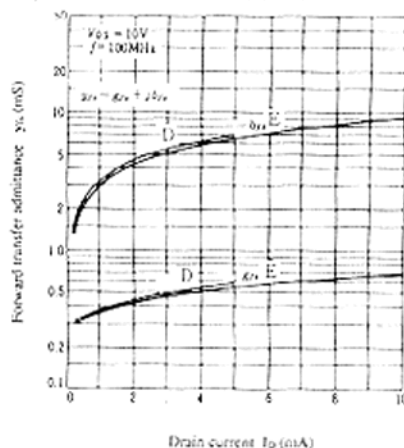
GATE TO SOURCE CUTOFF VOLTAGE VS. DRAIN CURRENT



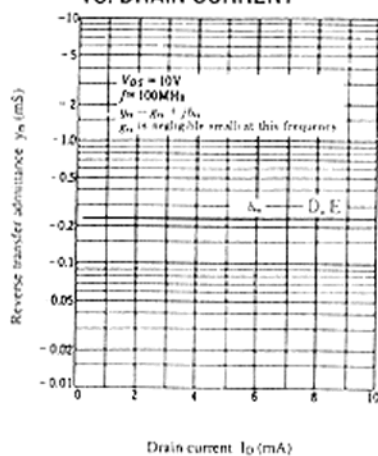
INPUT ADMITTANCE VS. DRAIN CURRENT



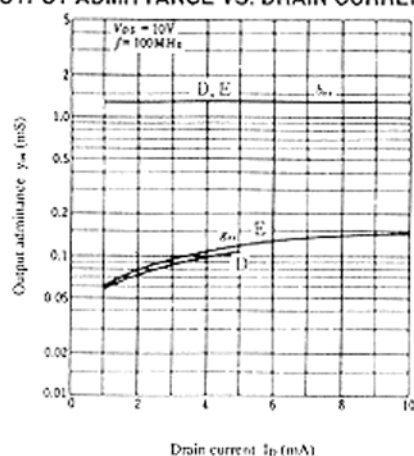
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



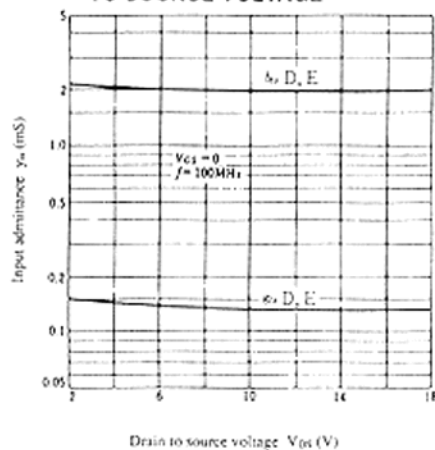
REVERSE TRANSFER ADMITTANCE VS. DRAIN CURRENT



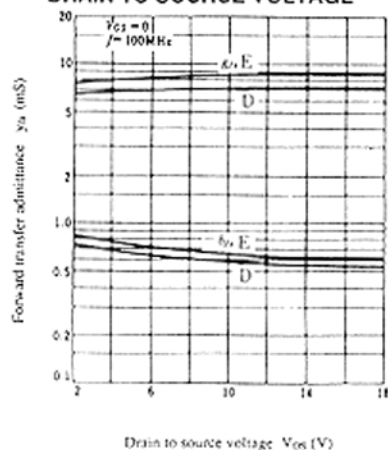
OUTPUT ADMITTANCE VS. DRAIN CURRENT



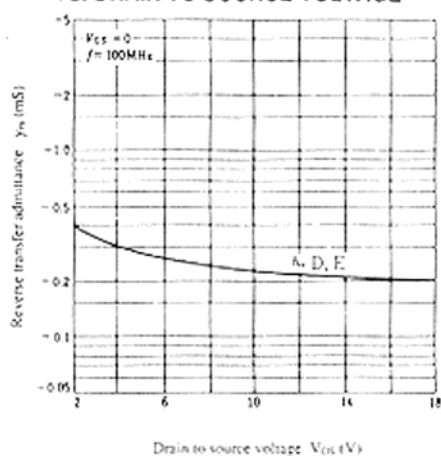
INPUT ADMITTANCE VS. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER ADMITTANCE VS. DRAIN TO SOURCE VOLTAGE



REVERSE TRANSFER ADMITTANCE VS. DRAIN TO SOURCE VOLTAGE



OUTPUT ADMITTANCE VS. DRAIN TO SOURCE VOLTAGE

