

HD74HC155

Dual 2-to-4-line Decoders/Demultiplexers

HITACHI

Description

This circuit features dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address input. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

Features

- High Speed Operation: t_{pd} (A or B to Y) = 15 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

2-line-to-4-line Decoder/1-line-to-4-line Demultiplexer

Inputs

Select		Strobe	Data	Outputs			
B	A	1G	1C	1Y ₀	1Y ₁	1Y ₂	1Y ₃
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

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Inputs

Select		Strobe	Data	Outputs			
B	A	2G	2C	2Y ₀	2Y ₁	2Y ₂	2Y ₃
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-line-to-8-line Decoder/1-line-to-8-line Demultiplexer

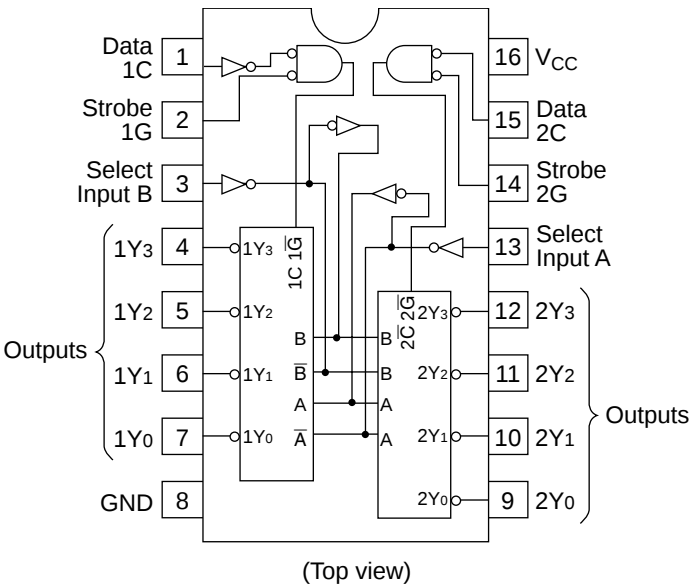
Inputs

Outputs

Select				Strobe Data	0	1	2	3	4	5	6	7
C	B	A	G		2Y ₀	2Y ₁	2Y ₂	2Y ₃	1Y ₀	1Y ₁	1Y ₂	1Y ₃
X	X	X	H		H	H	H	H	H	H	H	H
L	L	L	L		L	H	H	H	H	H	H	H
L	L	H	L		H	L	H	H	H	H	H	H
L	H	L	L		H	H	L	H	H	H	H	H
L	H	H	L		H	H	H	L	H	H	H	H
H	L	L	L		H	H	H	H	L	H	H	H
H	L	H	L		H	H	H	H	H	L	H	H
H	H	L	L		H	H	H	H	H	H	L	H
H	H	H	L		H	H	H	H	H	H	H	L

- Notes: 1. C: inputs 1C and 2C connected together
2. G: inputs 1G and 2G connected together
3. X: irrelevant

Pin Arrangement

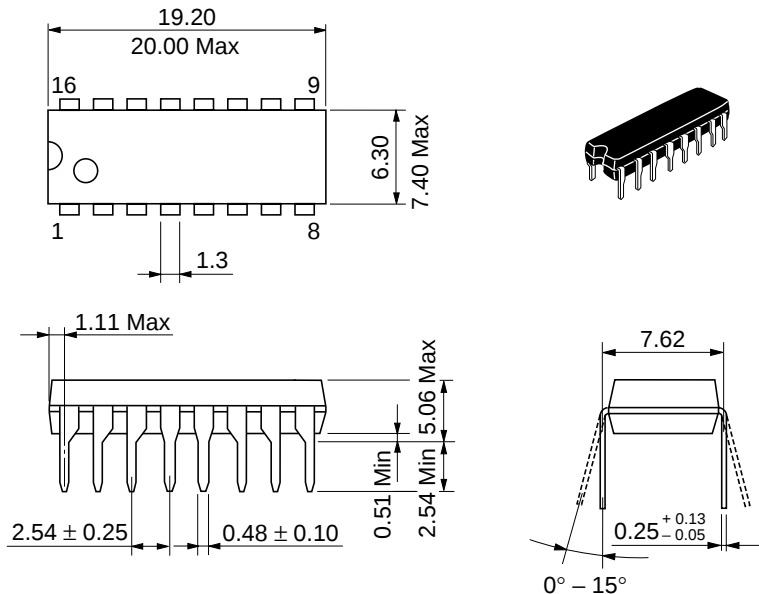


DC Characteristics

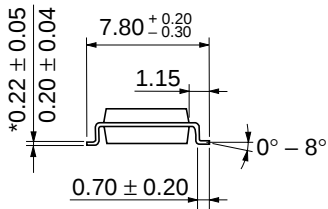
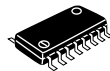
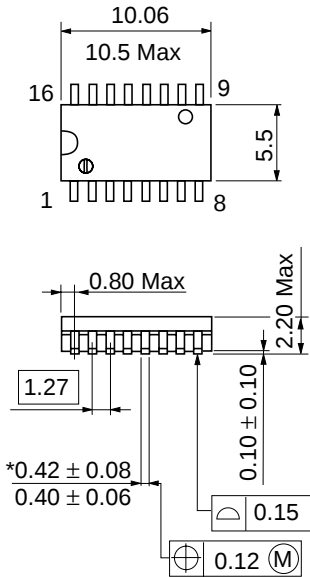
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	t _{PLH}	2.0	—	—	160	—	200	ns	A, B, 2C, 1G or 2G to Y
	t _{PHL}	4.5	—	13	32	—	40		
		6.0	—	—	27	—	34		
		2.0	—	—	160	—	200	A or B to Y	
		4.5	—	15	32	—	40		
		6.0	—	—	27	—	34		
		2.0	—	—	145	—	180	1C to Y	
		4.5	—	14	29	—	36		
		6.0	—	—	25	—	31		
Output rise/fall time	t _{TLH}	2.0	—	—	75	—	95	ns	
	t _{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C _{in}	—	—	5	10	—	10	pF	

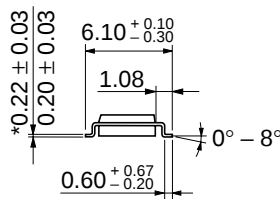
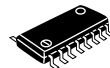
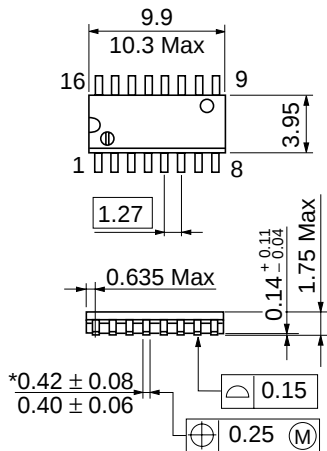


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

$$\frac{\text{*Dimension including the plating thickness}}{\text{Base material dimension}}$$



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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