HA13703A

IPIC* High Side Solenoid Driver

Description

(IPIC: Intelligent Power IC)

HA13703A is high side power driver IC with protectors and diagnostic function. The device is especially designed to switch inductive loads.

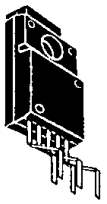
Functions

- Power MOS source follower output (4 A)
- With over voltage shut down circuit (OVSD)
- With over current protector circuit (OCSD)
- With over temperature shut down circuit (OTSD)
- With diagnostic circuit and status output
- With fail safe function under input open circuit condition
- With low voltage inhibit circuit (LVI)

Features

- Protected against 60 V load dump condition
- Low R_{ON} (0.1 Ω typ)
- Wide operating supply voltage range (V_{DD} = 7 V to 25 V)
- High sustaining voltage (–15 V)
- Protected against reverse supply voltage (–13 V)
- Protected against short circuit condition
- Suitable switching speed to have high speed operation and low EMI
- Input compatible with TTL, LS-TTL, or 5 V CMOS
- Protected against electrostatic discharge (2 kV min at 100 pF/1.5 kΩ)

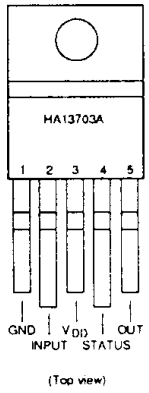
HA13703A



SP-5TA

Pin Arrangement

SP-5TA



Ordering Information

Type No.	Package
HA13703A	SP-5TA

Figure 1
Pin Arrangement

Block Diagram

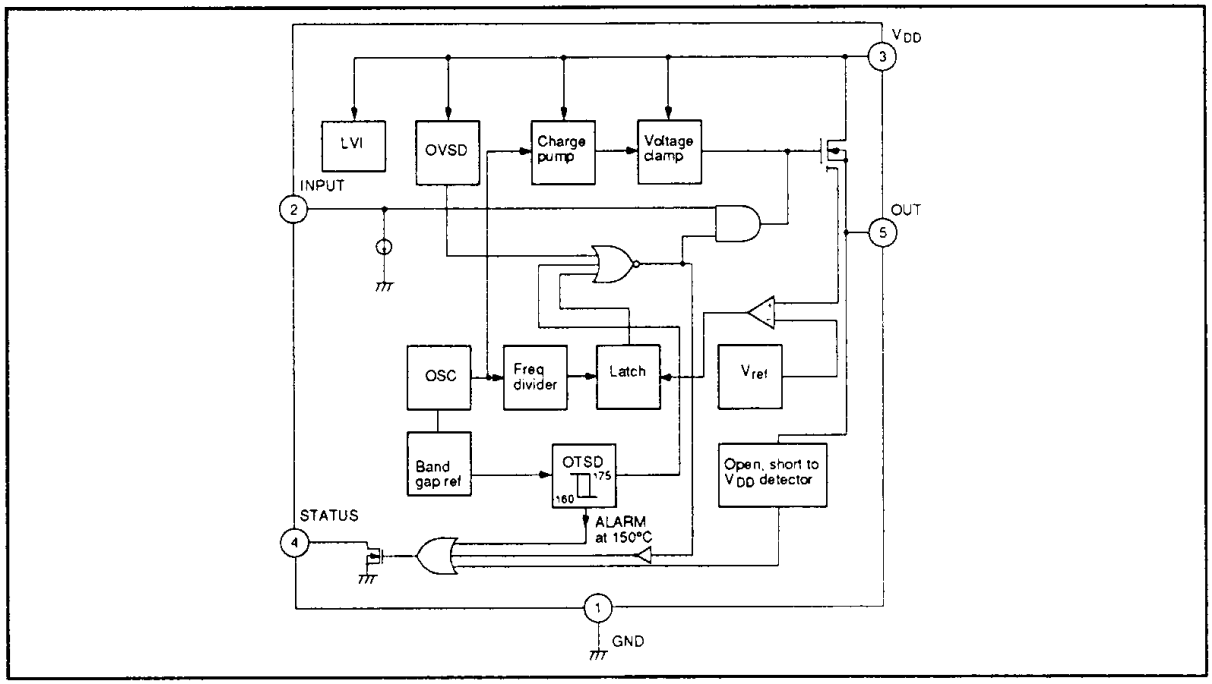


Figure 2 Block Diagram

Function Description

Peak Current and Turn-off Time

Figure 3 shows waveforms of load current (Iout) and output voltage (Vout) at driving inductive load.
The peak output current (Ip) and sustaining time (t_{sus}) can be described as

$$Ip = \frac{V_{DD}}{R}(1 - e^{-\frac{R}{L}t_{ON}}) \quad (1)$$

$$t_{sus} = \frac{L}{R} \ln\left(1 + \frac{Ip \cdot R}{V_B}\right) \quad (2)$$

Where
R : Equivalent resistance of the load
L : Equivalent inductance of the load

HA13703A has the internal protector to prevent turn on during t_{sus} period.

Table 1 Truth Table

Mode		In	Out	Status
Normal		L	L	H
		H	H	H
Load short		L	L	H
		H	L	L
Load open		L	L	H
		H	H	L
Short to V_{DD}		L	H	L
		H	H	L
OTSD	*1	L	L	L
		H	L	L
OVSD	*2	L	L	L
		H	L	L
LVI	*3	L	L	H
		H	L	H

Note: L: Low level (0.8 V)
H: High level (2.0 V)
*1) OTSD: Over temperature shut down
*2) OVSD: Over voltage shut down
*3) LVI: Low voltage inhibit

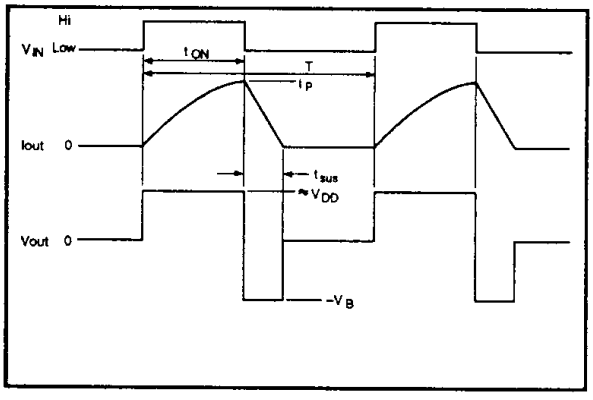


Figure 3 Peak Current and Turn-off Time

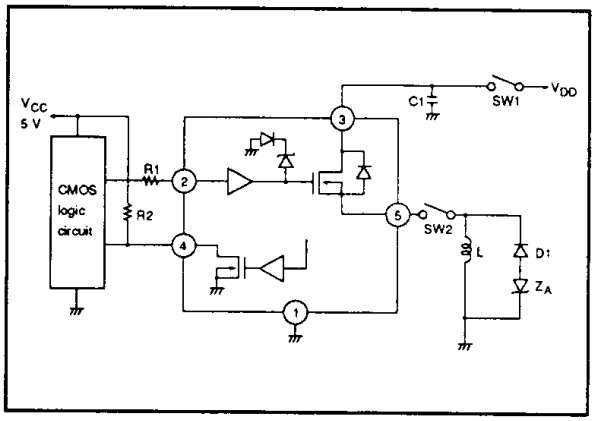


Figure 4 Solenoid Drive with Switched Power Supply

D1 & Z_A: The external voltage clamp circuit using D1 & Z_A are necessary to protect the HA13703A when SW2 switches under normal operating conditions. D1 & Z_A must be in parallel with the load.

The zener voltage (V_{ZB}) and forward diode voltage (V_{D1}) must satisfy the following:

$$V_{D1} + V_{ZB} < 15\ V\ (= V_{(sus)\ MIN}) \quad (3)$$

R1: When SW1 opens with output ON, the Input (Pin 2) may be shorted to GND. In this case, R1 will limit the current from logic circuits at pin 2.

R2: Pull up resistor at Status output.

C1: When SW1 opens with Output ON, the energy stored in the load L can not be dissipated through V_{DD}. Therefore, C1 must be able to absorb this energy, and can be selected from

$$C1 > L \cdot \left(\frac{I_P}{V_{DD}}\right)^2 \quad (4)$$

Note that when using D1 & Z_A clamp, it may not be necessary to use as large a capacitor as described above. In this case, C1 must have the value to compensate the inductance at V_{DD} line (refer equation 4) and should be located near the device.

Reverse Battery

Under reverse battery condition, the HA13703A will dissipate power (P_D^*) because of current through the intrinsic diode on power MOS. P_D^* can be calculated as follows and must not exceed the absolute maximum rating on power dissipation.

$$P_D^* = \frac{-V_{DD}^* - V_{F(B)}}{R} \cdot V_{F(B)} \quad (5)$$

Where
V_{DD}^* = reverse battery voltage
$V_{F(B)}$ = forward intrinsic diode voltage
R = equivalent resistance of the load

The input and status voltage must not exceed the absolute maximum rating (–0.3 V) in reverse battery condition.

Table 2 Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	HA13703A	Unit	Note
Continuous supply voltage		V_{DD}	−13 to 35	V	1
Transient supply voltage		V_{DD}	60	V	2
Input voltage		V_{IN}	−0.3 to 15	V	
Output voltage		Vout	−15 to V_{DD}	V	
Status voltage		V_S	−0.3 to 15	V	
Output current		Iout	—	A	3
Status current		I_S	5	mA	
Power dissipation		P_T	—	W	4
Package thermal rsistance	Junction to case	θjc	5	°C/W	
	Junction to air	θja	70	°C/W	
Junction temperature range		Tj	−40 to OTSD	°C	5
Storage temperature range		Tstg	−55 to 150	°C	

Notes: 1. Recommended operating voltage:
V_{DD} = 7 to 16 V (Normal)
16 to 25 V (Jump start)

2. Load dump condition (Refer to figure 5)

3. Refer to ASO data (figure 6)
Internally limited at
Short circuit condition ; ID ≥ 10A
Over voltage condition ; VDD ≥ 26V

4. Maximum power dissipation (PT(Max)) can be defined as:
$P_T(MAX) = (T_{jopr}(MAX) - T_{ambient})/(\theta jc + \theta ca)$
θca: Thermal resistance between case and air (Depend on heat sink size)

5. Junction temperature operating range Tjopr = −40 to +125 °C

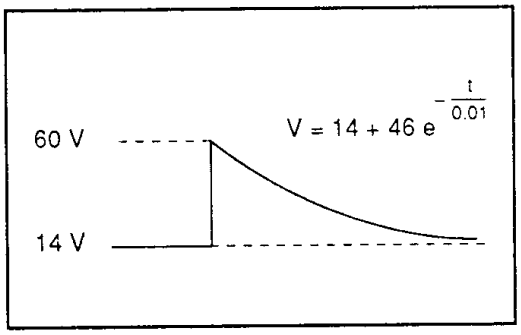


Figure 5 Load Dump Condition

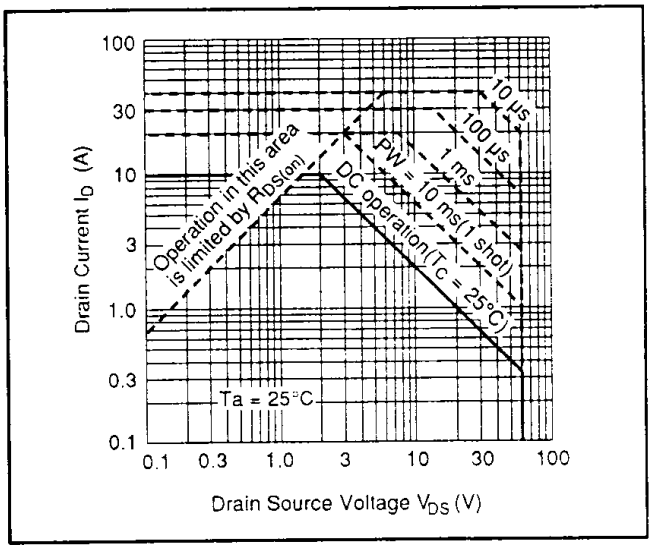


Figure 6 Output Transistor Area of Safe Operation (Reference Data)

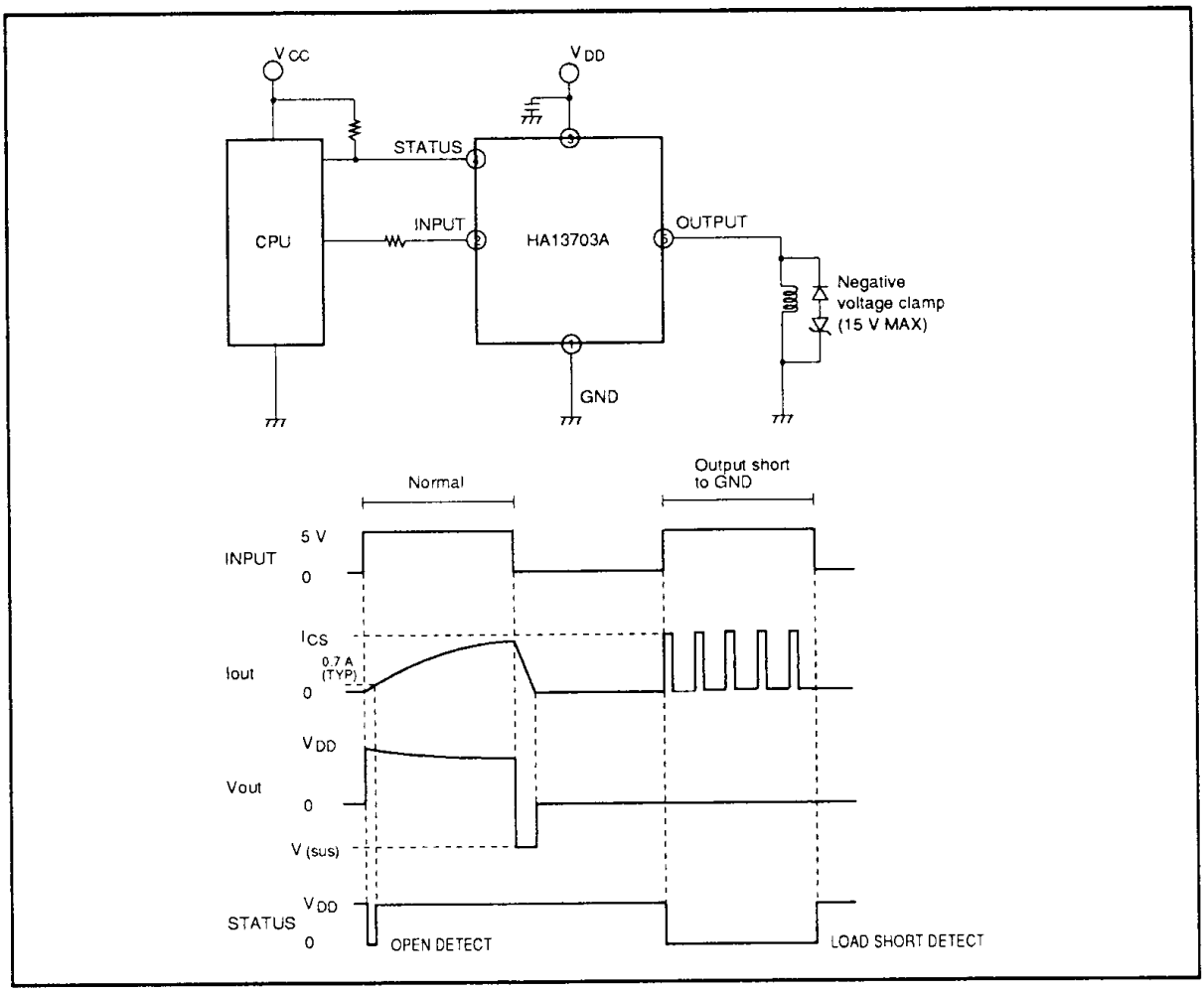


Figure 7 Solenoid Drive Application and Output Waveform

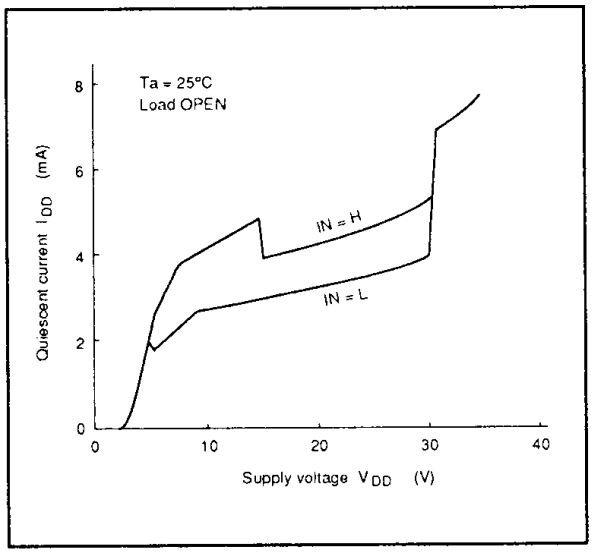


Figure 8 I_{DD} vs. V_{DD}

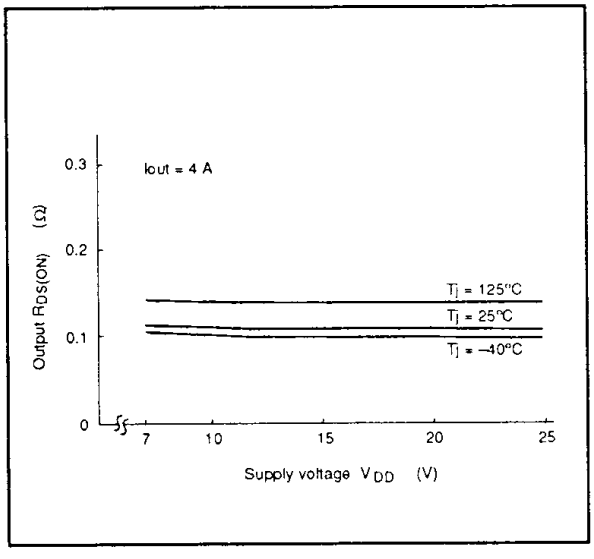


Figure 9 $R_{DS(ON)}$ vs. V_{DD}

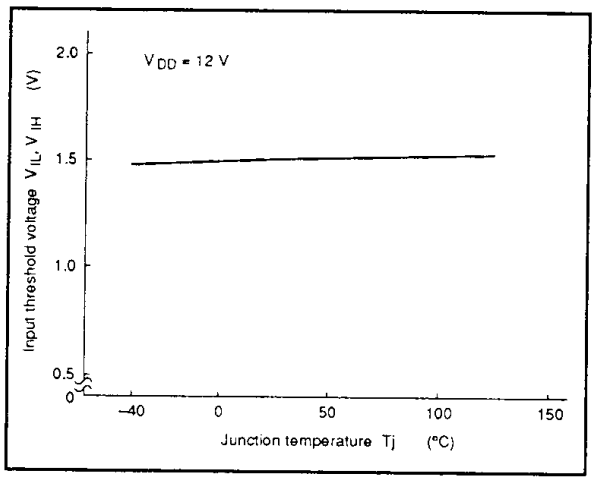


Figure 10 V_{IL}, V_{IH} vs. Tj

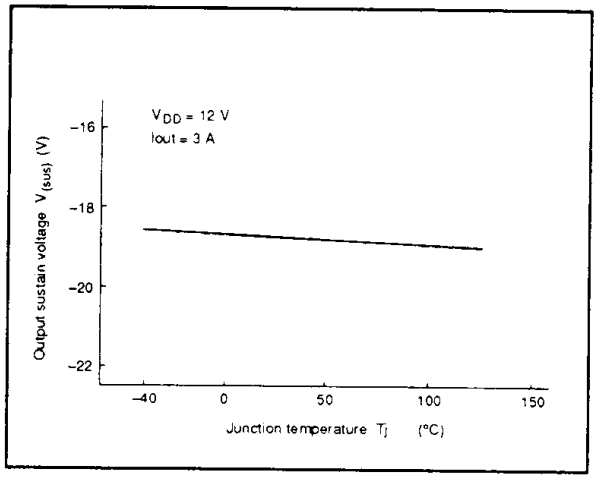


Figure 11 $V_{(sus)}$, V_{IH} vs. Tj

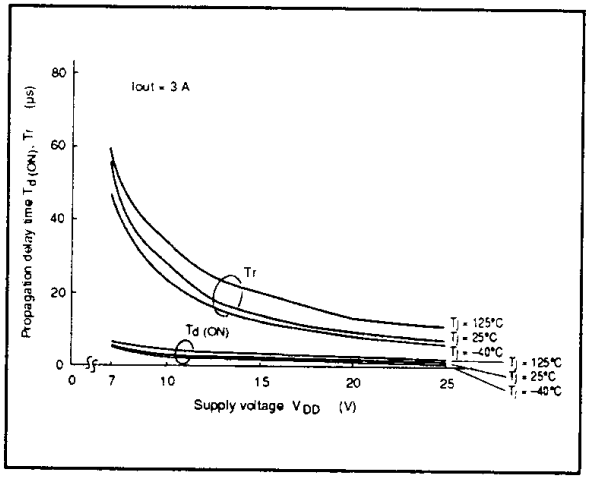


Figure 12 $Td_{(ON)}$, Tr vs. V_{DD}

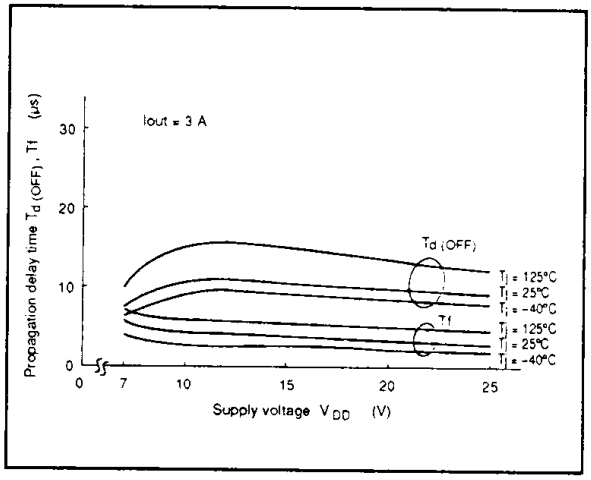


Figure 13 $Td_{(OFF)}$, Tf vs. V_{DD}

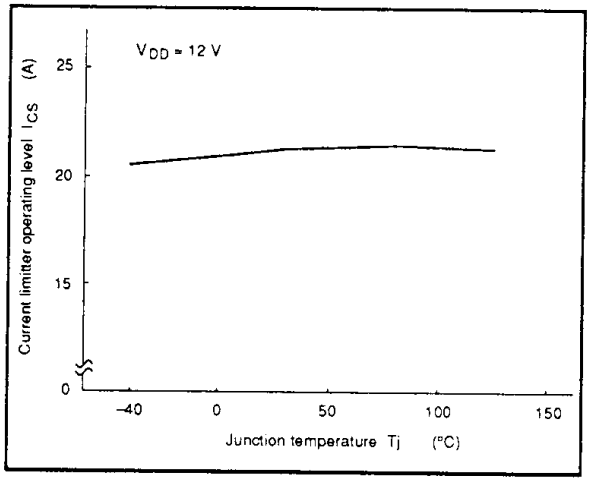


Figure 14 I_{CS}, vs. T_j

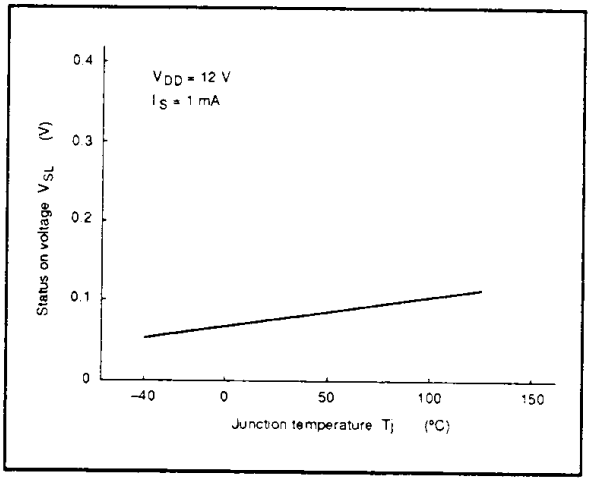


Figure 15 V_{SL}, vs. T_j

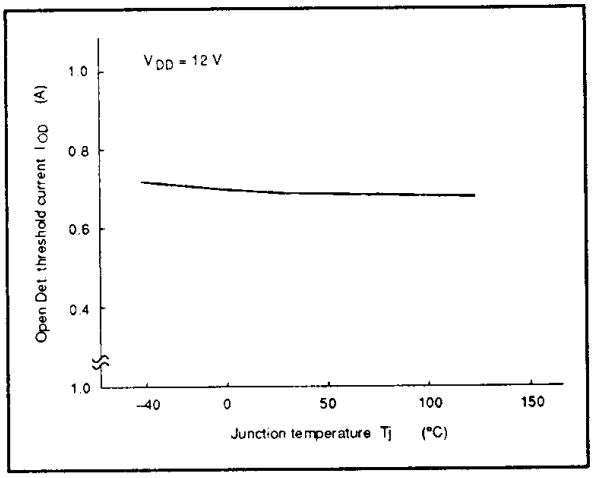


Figure 16 I_{OD} vs. Tj

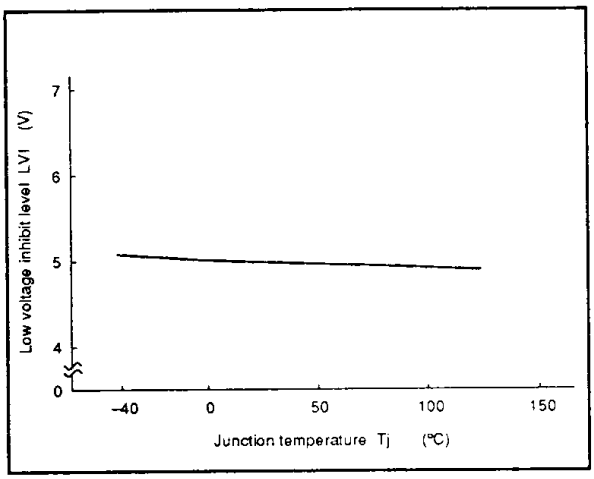


Figure 17 LVI vs. Tj

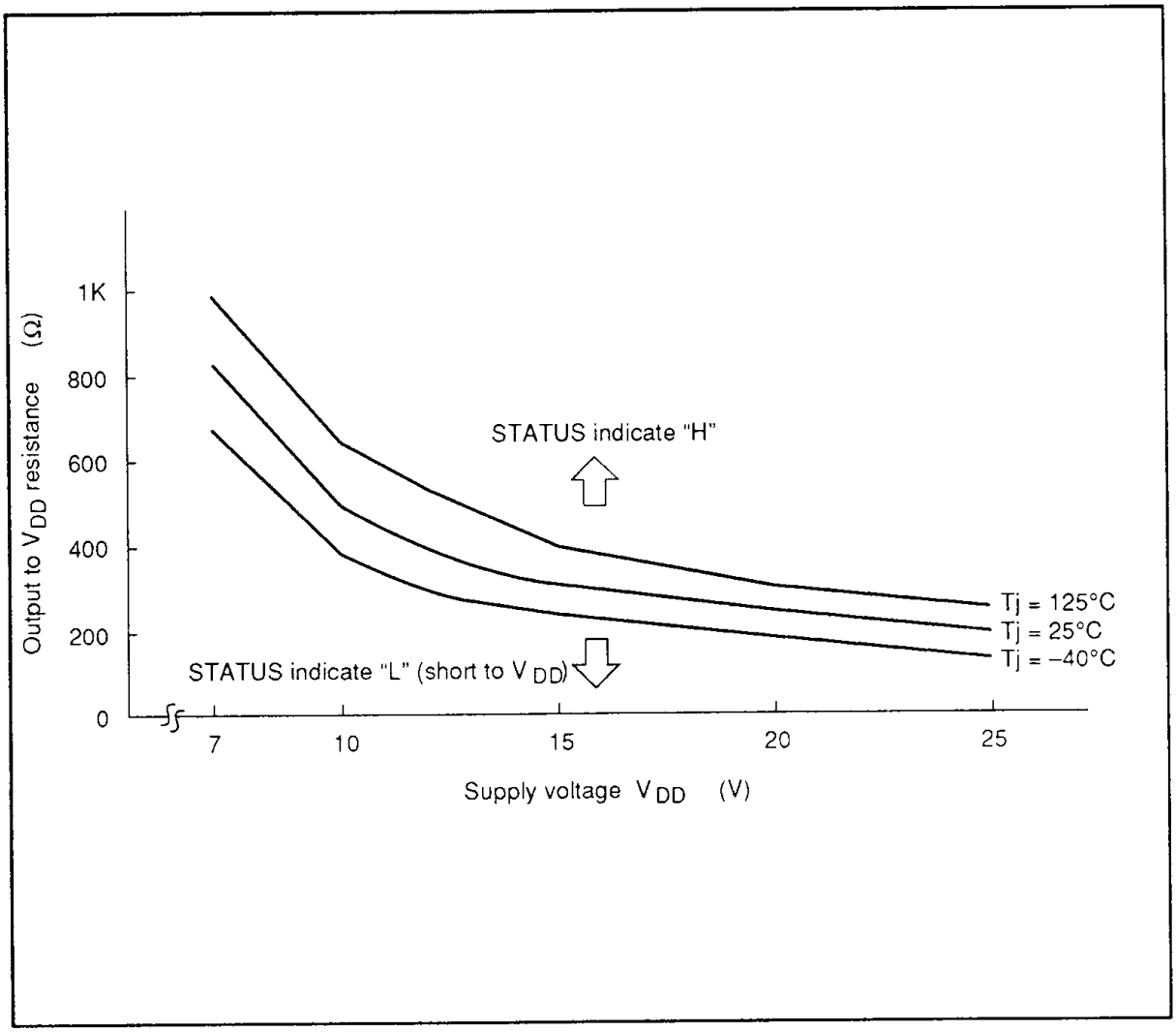


Figure 18 Output to V_{DD} Resistance vs. Supply Voltage

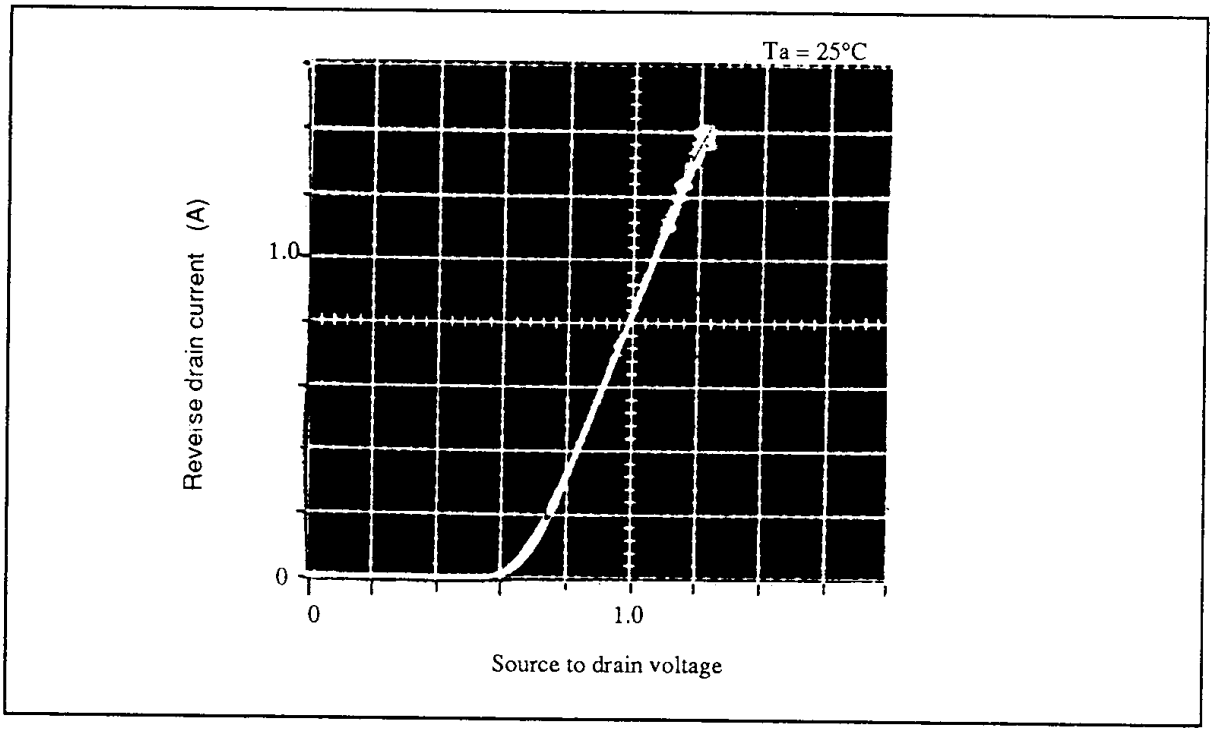


Figure 19 Reverse Drain Current vs. Source to Drain Voltage on Power MOS