

# HAT2037T

Silicon N Channel Power MOS FET  
High Speed Power Switching

# HITACHI

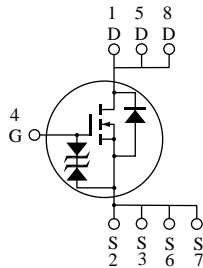
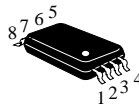
ADE-208-530 D (Z)  
5th. Edition  
February 1999

## Features

- Low on-resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

## Outline

TSSOP-8



1, 5, 8 Drain  
2, 3, 6, 7 Source  
4 Gate

**Absolute Maximum Ratings** ( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	28	V
Gate to source voltage	$V_{GSS}$	$\pm 12$	V
Drain current	$I_D$	5.5	A
Drain peak current	$I_{D(\text{pulse})}$ <sup>Note1</sup>	44	A
Body-drain diode reverse drain current	$I_{DR}$	5.5	A
Channel dissipation	Pch <sup>Note2</sup>	1.3	W
Channel temperature	Tch	150	$^\circ\text{C}$
Storage temperature	Tstg	-55 to +150	$^\circ\text{C}$

Note: 1.  $PW \leq 10\mu\text{s}$ , duty cycle  $\leq 1\%$

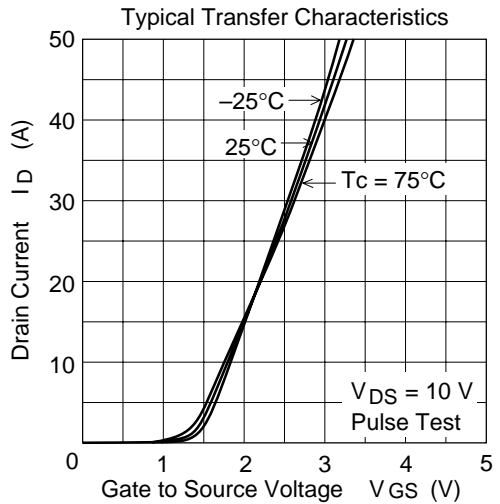
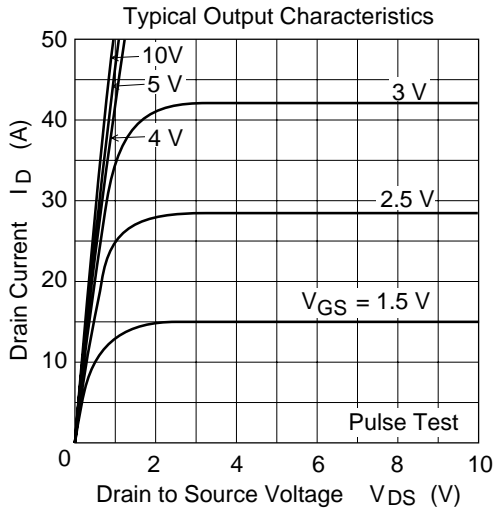
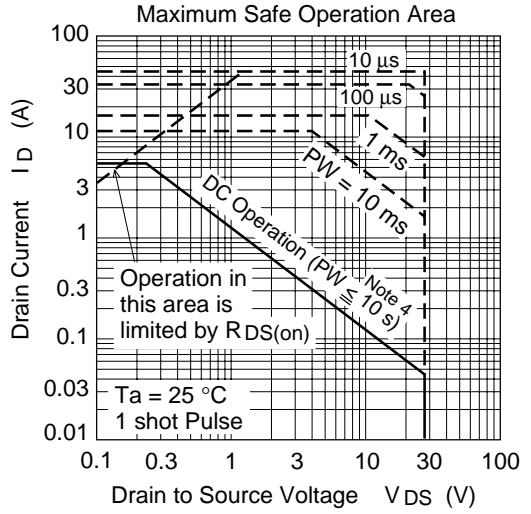
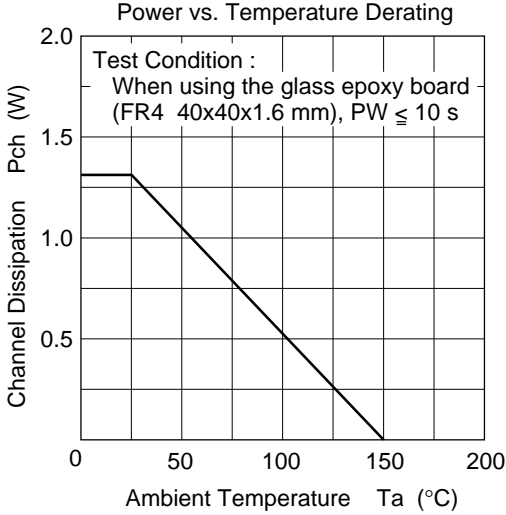
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10\text{s}$

**Electrical Characteristics** ( $T_a = 25^\circ\text{C}$ )

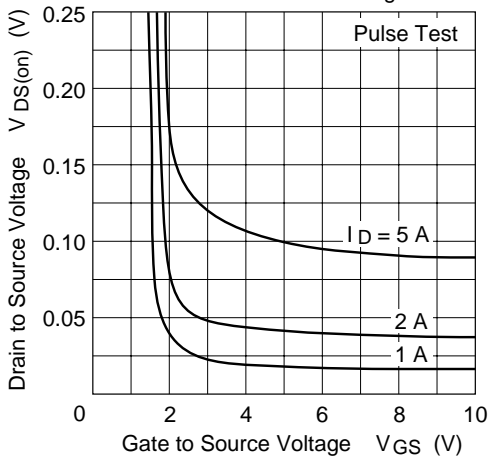
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	28	—	—	V	$I_D = 10\text{mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 12$	—	—	V	$I_G = \pm 100\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 10\text{V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 28\text{V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(\text{off})}$	0.4	—	1.4	V	$V_{DS} = 10\text{V}$ , $I_D = 1\text{mA}$
Static drain to source on state resistance	$R_{DS(\text{on})}$	—	0.021	0.028	$\Omega$	$I_D = 3\text{A}$ , $V_{GS} = 4\text{V}$ <sup>Note3</sup>
	$R_{DS(\text{on})}$	—	0.027	0.038	$\Omega$	$I_D = 3\text{A}$ , $V_{GS} = 2.5\text{V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	9	14	—	S	$I_D = 3\text{A}$ , $V_{DS} = 10\text{V}$ <sup>Note3</sup>
Input capacitance	Ciss	—	780	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	Coss	—	470	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	190	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(\text{on})}$	—	20	—	ns	$V_{GS} = 4\text{V}$ , $I_D = 3\text{A}$
Rise time	$t_r$	—	130	—	ns	$V_{DD} \approx 10\text{V}$
Turn-off delay time	$t_{d(\text{off})}$	—	155	—	ns	
Fall time	$t_f$	—	160	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.81	1.06	V	$IF = 5.5\text{A}$ , $V_{GS} = 0$ <sup>Note3</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	55	—	ns	$IF = 5.5\text{A}$ , $V_{GS} = 0$ $diF/dt = 20\text{A}/\mu\text{s}$

Note: 3. Pulse test

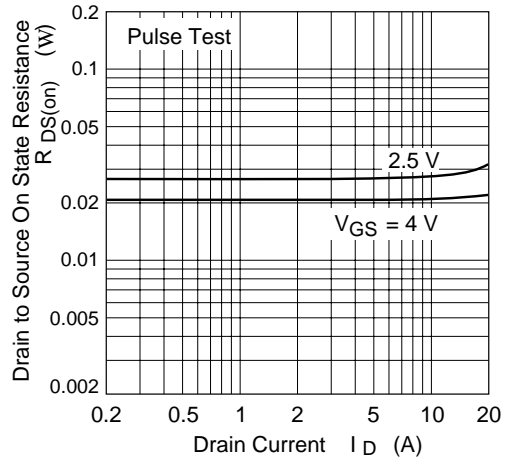
Main Characteristics



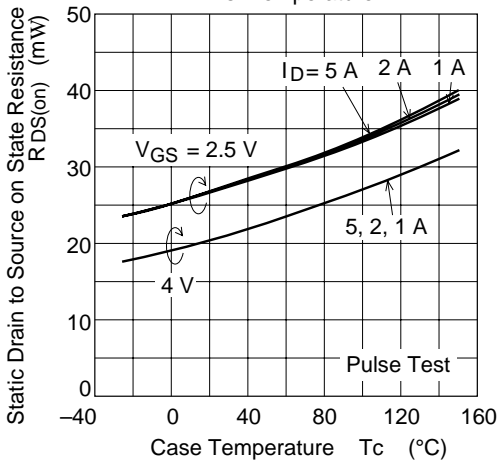
Drain to Source Saturation Voltage vs. Gate to Source Voltage



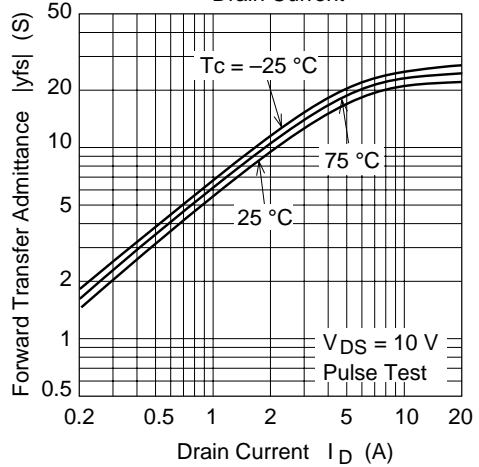
Static Drain to Source on State Resistance vs. Drain Current



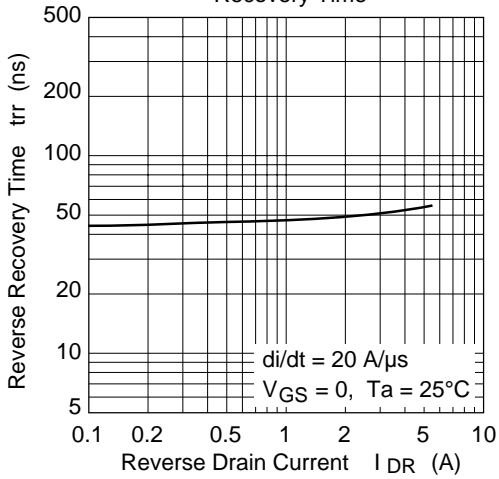
Static Drain to Source on State Resistance vs. Temperature



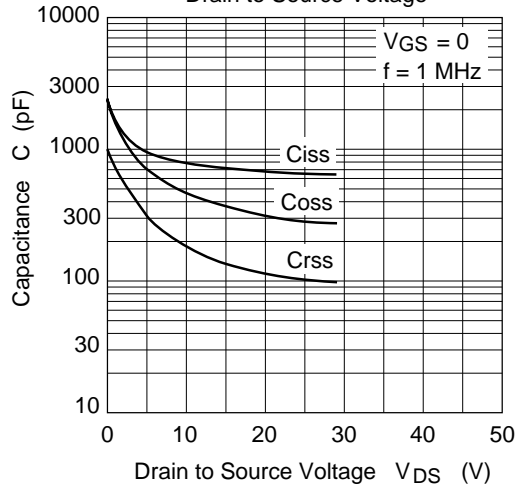
Forward Transfer Admittance vs. Drain Current



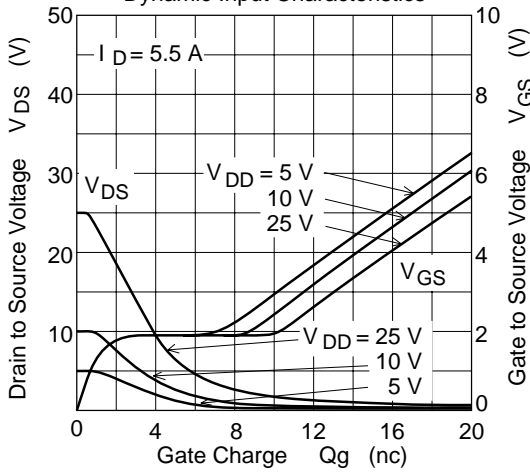
Body-Drain Diode Reverse Recovery Time



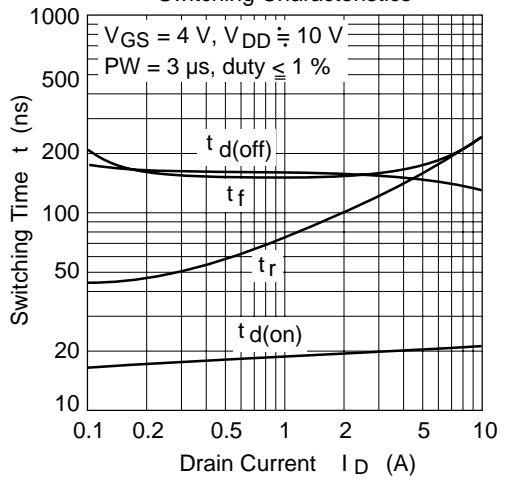
Typical Capacitance vs. Drain to Source Voltage

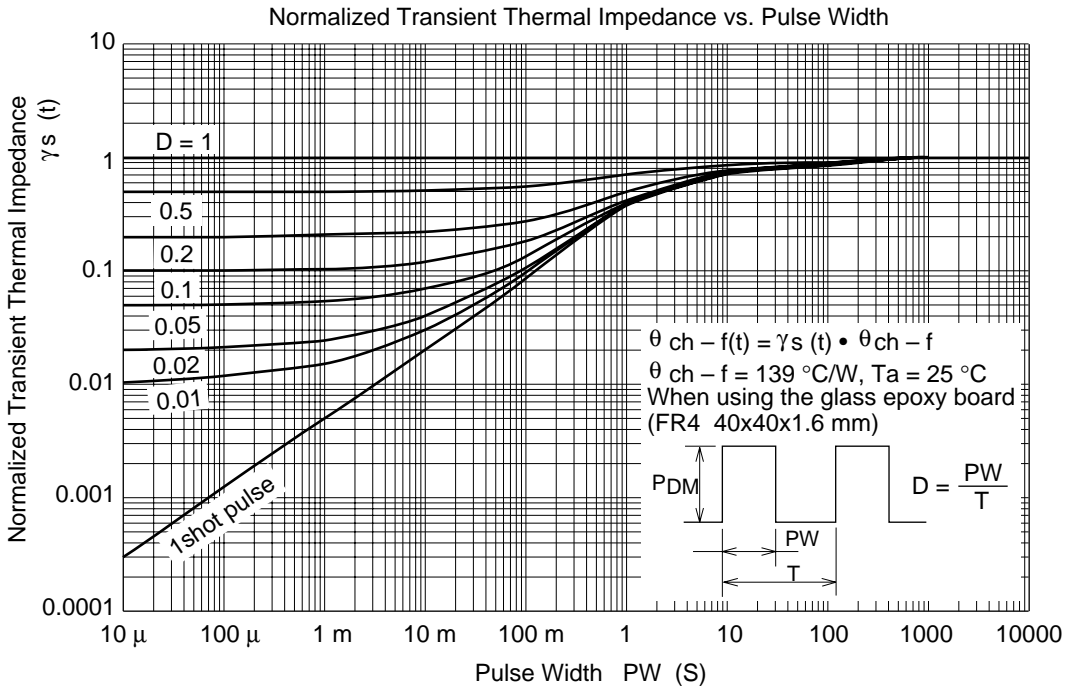
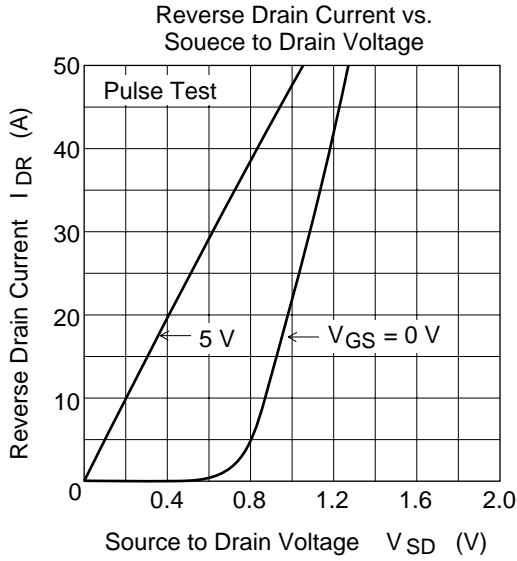


Dynamic Input Characteristics

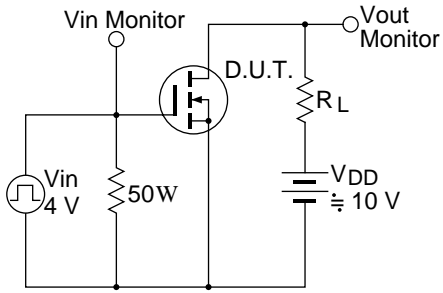


Switching Characteristics

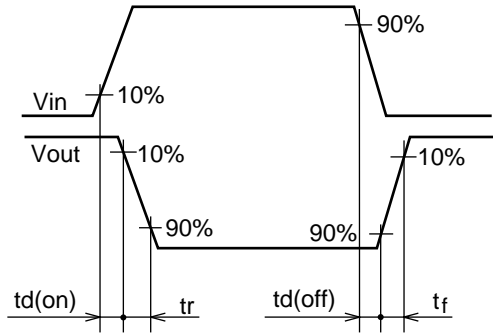




Switching Time Test Circuit

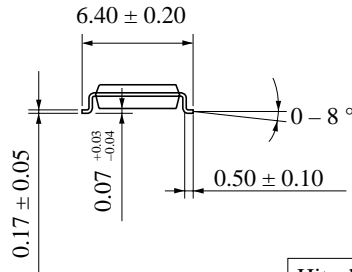
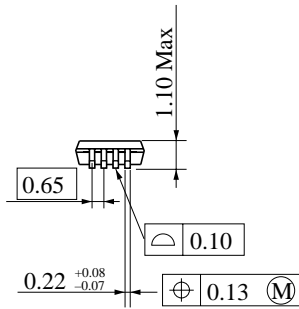
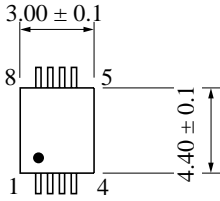


Switching Time Waveform



## Package Dimensions

Unit: mm



Hitachi code	TTP-8D
EIAJ	—
JEDEC	—

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