ZL10320/1

Digital Television PVR-on-a-Chip Processor

Data Sheet

May 2003

Features

- Single Chip solution for Digital Terrestrial Personal Video Recorder (PVR) Products
- Supports Simultaneous 'Pause & Resume' and 2nd-channel recording
- PVR controller providing bitstream multiplexing, PID filtering and record/playback control.
- Dual on-chip DVB-T COFDM demodulators with Forward Error Correction.
- IDE interface
- MPEG-2 Audio & Video decoder
- PowerPC 405^{TM} CPU Core with 16k/16k cache, Memory manager and Virtual memory system
- Dual SDRAM controller
- 6 Video DACs on-chip, for Composite (CVBS) or Component (RGB, YPrPb) Analog Video
- Twin PAL/NTSC DENCs
- I^2S Digital Audio Input
- I^2S and S/PDIF Digital Audio outputs
- DVB-CI Common Interface (CI) control and bitstream interfaces
- Conditional Access (CA) DVB-descrambler
- Smart Card Interface
- Inputs for external MPEG-2 Transport Streams, allowing support for external demodulators (e.g. Cable TV, Satellite TV)
- External Modem support interface

Ordering Information

ZL10320/GAC	388 ball EPBGA
ZL10321/GAC	388 ball EPBGA

0°C to +70°C

- Infrared & UART interface
- Linux-based Software Development Kit (SDK)
- Low Power (<1.4W Typical, in full operation)
- Low Application Component Count
- Small Footprint applications
- Supports Macrovision^{TM} Copy Protection - (*ZL10321 only; Macrovision license holders only)*
- Dolby® Digital Decoding - *(ZL10321 only; Dolby® Digital* license holders only - *awaiting certification)*
- Ideal solution for UK Freeview services

Applications

- DVB-T based PVR products
- DVB-T/PVR combo products
- Dual Channel decoder products
- iDTV/PVR combo products

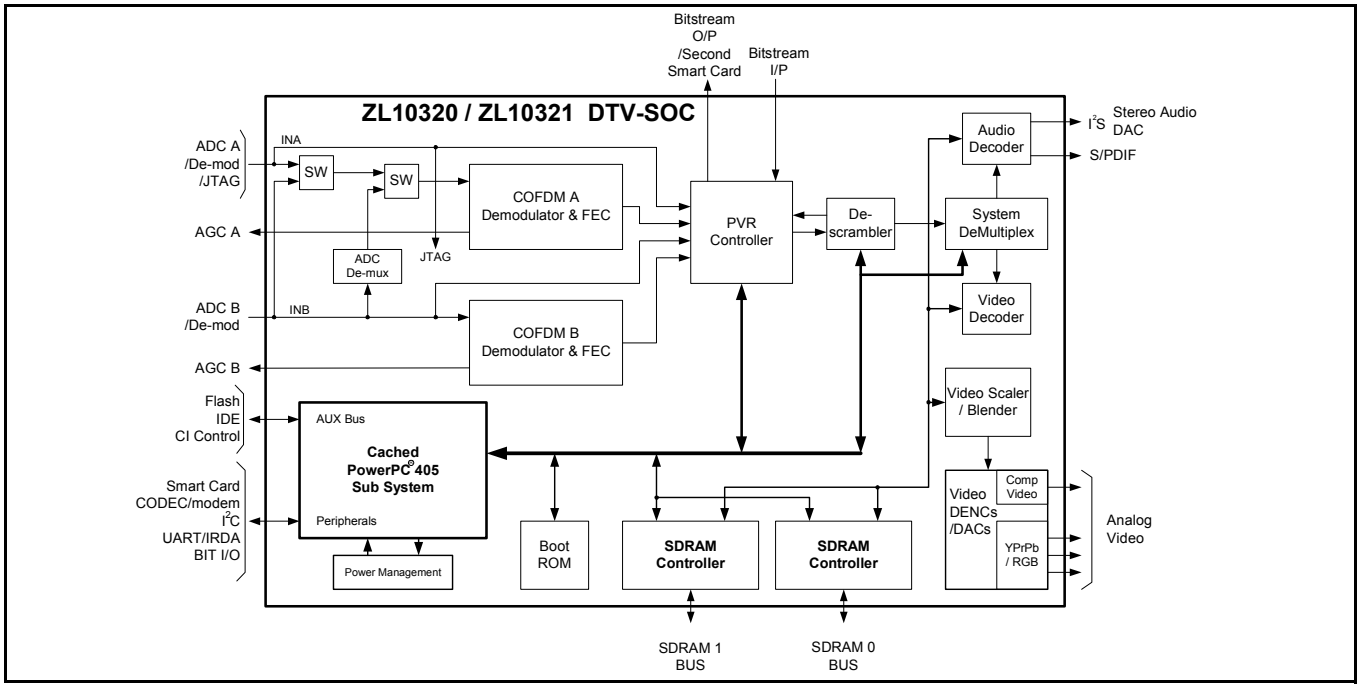


Figure 1 - ZL10320 and ZL10321 Block Diagram

Description

The ZL10320 is a DVB-T PVR-on-a-Chip solution which enables the rapid development of cost effective and feature-rich DVB-T based Personal Video Recorders (PVR). To achieve this, Zarlink has integrated two DVB-T compliant COFDM demodulators, an MPEG-2 audio/video decoder, a PVR controller and a full suite of set-top box/iDTV interfaces together with a high performance CPU into a single System-on-a-Chip (SoC) solution.

The ZL10320's PVR Controller can sustain the simultaneous transfer of three MPEG-2 Transport Streams with a hard disk drive, permitting, for example, simultaneous recording of two TV Channels and playing-back a third; essentially three VCRs in a box. The key capability of PVR technology is the ability to live-pause and time-shift live broadcast television, where a recorded stream can be played back before its recording has completed. The ZL10320 supports this function, and in addition allows the simultaneous recording of a second digital channel. This is made possible by high-performance on-chip DMA controllers, which transfer bitstreams between the PVR Controller, SDRAM and IDE Hard Disk(s) efficiently, with minimum CPU overhead.

PVR functionality places considerable demand on the software environment, which necessitates that such systems are based on robust multitasking operating systems, supporting virtual memory and memory management. Linux, with its wide range of capabilities is ideally suited for such applications. Consequently the ZL10320 uses the high-performance PowerPC 405 RISC processor, which fully supports the requirements of the Linux Operating System.

The ZL10320 is able to share a common Linux Code base at the device driver, middleware and application layers with the entry-level ZL10310/ZL10311 solutions, which are also available from Zarlink Semiconductor.

Also available is the ZL10321 DVB-T PVR-on-a-Chip, which additionally offers Dolby® Digital[1] multi-channel audio decoding, and Macrovision™ Copy Protection for applications requiring Dolby® Audio and Pay TV services.

Device Interfaces

The following peripheral interfaces are available to the user. Apart from possible level translation and connector buffering, no external devices are required to support any of the interfaces.

- Dual 10-bit inputs that may be configured for separate ADC inputs or a single multiplexed ADC input
- Inputs from external video ADCs also act as external MPEG-2 transport stream inputs
- Dual AGC (PWM) outputs for two terrestrial tuners
- Serial control ports for two digital terrestrial tuners
- Serial control ports for external demodulator devices (e.g Satellite Demodulator)
- Common interface control and bitstream interfaces for an external descrambler
- Normal PC (PCMCIA) memory module interface for local software updates
- Shared 64 Mbit SDRAM interface for all decoders and PowerPC 405™
- Dual SDRAM interface to support advanced multi-channel recording functions
- Static memory interface for Flash and external peripherals
- IDE/ATAPI interface supporting up to 2 IDE/ATAPI devices
- External DMA channel and interrupts
- Six analog video outputs give full flexibility on RGB, Y PrPb, and Composite (CVBS) signals (with and without OSD)
- I^2S input port from external Digital Stereo source
- Three I^2S ports to external audio DACs for main, surround, and centre channels
- Dolby® surround sound control signals
- Sony/Philips Digital InterFace (S/PDIF)
- Full RS232 interface to an external modem or a 4 wire interface to a Codec
- IRDA interface or an additional asynchronous serial interface
- Synchronous serial interface for EEPROM, etc.
- Two Smart card Interfaces (one instead of a Common Interface)

1. The ZL10321 device is awaiting Dolby Certification

- General purpose I^2C interface
- General purpose timer for Infrared (IR) decoding
- General purpose individual bit I/Os

If not required in a particular system, any of the peripheral interfaces can be replaced by individual I/O bits from internal general purpose registers. These can then be used for additional purpose, such as interfacing to switches and displays.

Typical Applications

Free-to-Air Terrestrial PVR Receiver

Figure 2 on page 3 shows a typical Free-to-Air DVB-T compatible Terrestrial DTV PVR receiver block diagram employing a ZL10320 device. In its minimal configuration, the ZL10320 requires two 64Mbit SDRAM devices, an audio DAC, a Flash ROM, two Terrestrial Tuner Blocks (Zarlink can provide reference designs for modular tuners and 'tuner-on-motherboard' solutions), a dual multiplexed 10-bit analog to digital converter and an IDE Hard Disk Drive.

The compelling capability of PVR technology is the ability to live-pause and time-shift live broadcast television, where a recorded stream can be played back before its recording has completed. The ZL10320 extends this capability by additionally offering the ability to simultaneously 'Pause-Resume' on one TV channel whilst recording a second TV channel.

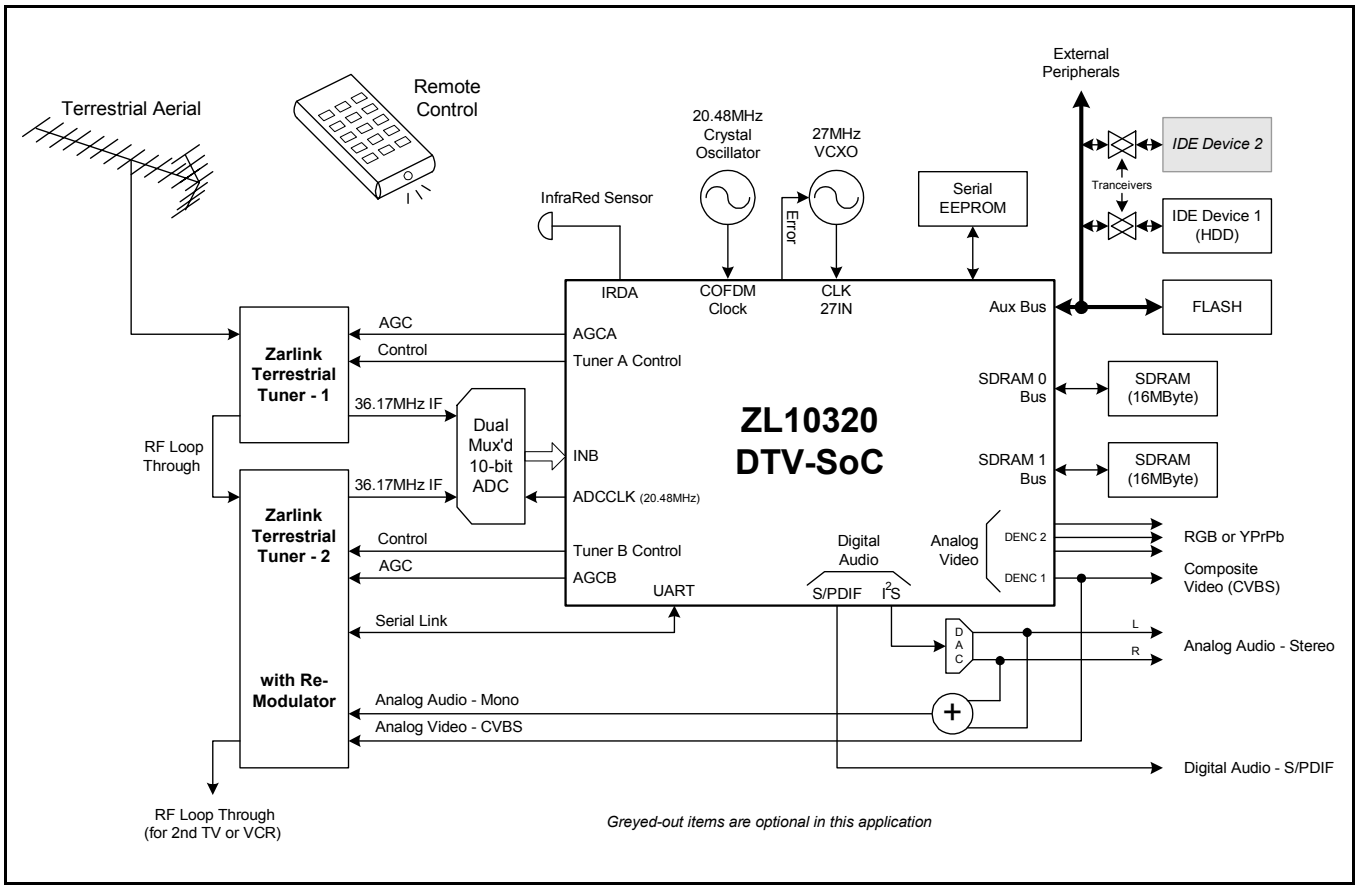


Figure 2 - Block diagram of a typical ZL10320 based Free-to-Air DVB-T PVR receiver

The Terrestrial Tuner sections perform an independent down conversion of the received DVB-T signal from the Antenna, to an IF frequency in the range of 30MHz to 57MHz, dependent on television system (typically 36.17MHz Center Frequency, with ±4MHz span). The analogue IF is then converted to the digital domain, with a 10-bit ADC, clocked at 20.48MHz and the resulting Digital output is centered on 15.69MHz. This Digital signal is applied to the ZL10320 via the ADC_IN[9:0] input pins, in the form of a 10-bit parallel signal.

The ZL10320 converts the digitized IF from a Terrestrial TV Tuner into an MPEG-2 Transport Stream, which can be optionally de-scrambled (if CA scrambling is used by the broadcaster), and de-multiplexed into separate Packetised Elementary Streams (PES), which are routed to the MPEG Audio and Video decoders, and SI data to the PowerPC 405^{TM} subsystem. The PVR controller block contains an additional 64 level PID filter for the efficient selection of the desired programme for recording.

Decoded Video can then be mixed and optionally scaled with On-Screen Display (OSD) Graphics generated by the DTV application software. The resultant combination of video and graphics are then routed to the PAL/NTSC Digital ENCoders (DENCs) for display on the TV via the on-chip 10-bit video DACs. The Video DACs can then produce Analog Video in either Composite Video (CVBS), or Component Video (RGB or YPrPb).

Decoded Audio is output directly from the audio decoder sub-system to the I^2S (Inter IC Sound) and S/PDIF (Sony/Philips Digital InterFace) outputs.

The Decoded Audio and Video from the ZL10320 can either be provided via standard Analogue Video and Audio connections to a Television Monitor, or can be used to provide the inputs to a UHF re modulator to provide a UHF Analogue Television signal to connect to a standard analogue TV.

Free-to-Air Dual-Standard Terrestrial and Satellite PVR Receiver

The ZL10320 can be used to implement multi-standard DVB receiver with the addition of external demodulator devices. Figure 3 on page 5 shows the block diagram of an example application of a dual-standard dual-channel selectable Satellite and Terrestrial PVR receiver. Zarlink Semiconductor's Satellite Tuner technology allows for the DVB-S and DSS Satellite television standards to be received. With the advent of Free-to-view satellite services in some countries, this concept has potential applications in regions where some TV services are available only on one or other standard (Terrestrial or Satellite) but not both.

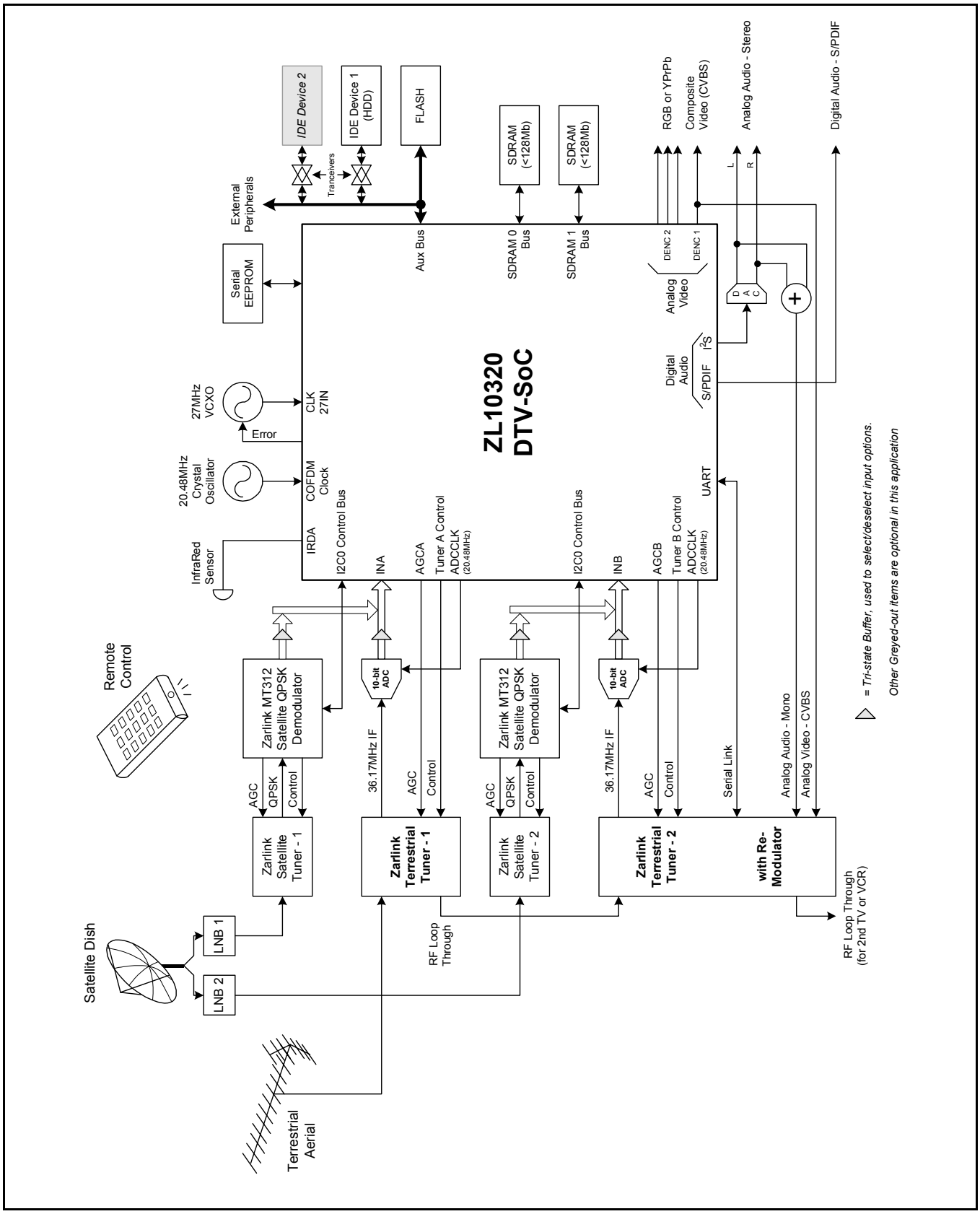


Figure 3 - Block Diagram of a Dual-Standard ZL10320 based Free-to-Air Terrestrial and Satellite PVR receiver

Standards Compliant

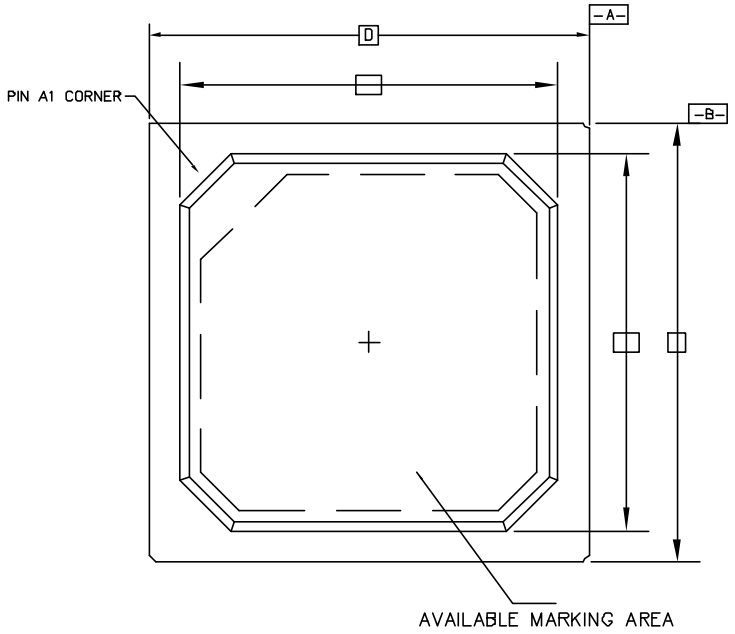
- ETSI EN300-744 (DVB-T)
- MPEG-2 Video & Audio
- Dolby® Digital for Multi-channel audio (ZL10321[1])
- Macrovision™ for copy protection support (ZL10321)

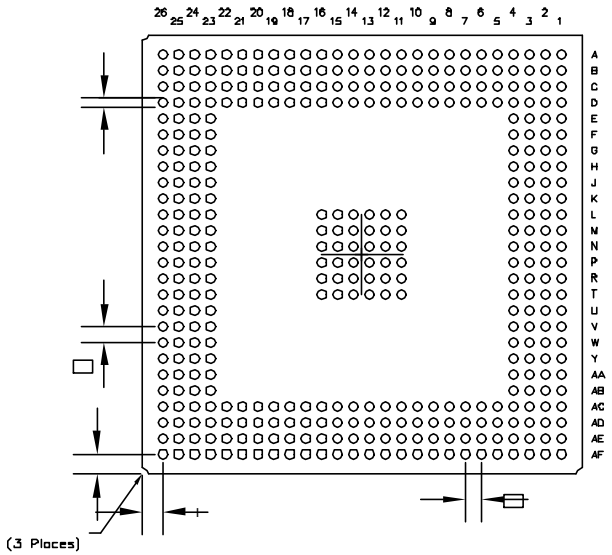
Complementary Products

- SL2610 single conversion tuner
- SL2001 up-down converter
- SL2009 IF AGC amp
- SL2150 antenna amplifier and power splitter
- SL1935 zero IF L-band tuner
- MT312 DVB-S QPSK demodulator

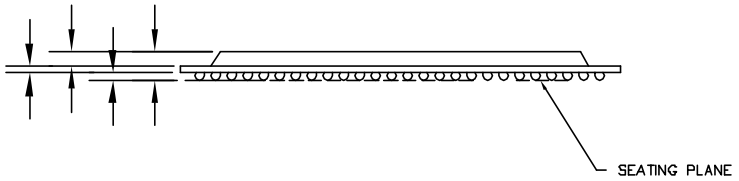
Customer Support

The ZL10320/321 devices are supported by Zarlink's network of in-house applications engineers and software design partners.





SYMBOL	CONTROL DIMENSIONS (mm)			NOTE
	MIN.	NOM.	MAX.	
A	-	-	2.65	
A_1	0.30	-	-	
A_2	-	-	-	
D	26.80	27.00	27.20	
D_1		25.00 BSC		
E	26.80	27.00	27.20	
E_1		25.00 BSC		
I		-		
J		-		
b	0.50	0.60	0.70	
c		-		
d		-		
e		1.00		
f		-		



NOTES: –

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. THIS DWG CONFORMS TO JEDEC MS–034A

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APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code

Package Outline for
388EPBGA 27 x 27

GPD00807

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE