

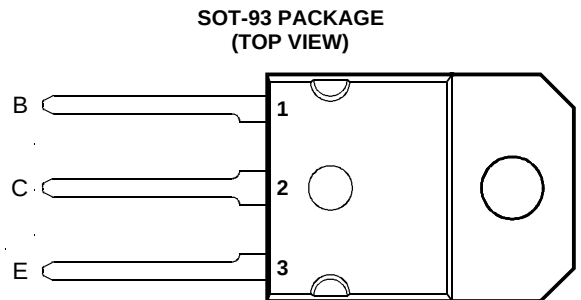
BU426, BU426A

NPN SILICON POWER TRANSISTORS

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AUGUST 1978 - REVISED MARCH 1997

- Rugged Triple-Diffused Planar Construction
- 900 Volt Blocking Capability



Pin 2 is in electrical contact with the mounting base.

MDTRAA

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Collector-base voltage ($I_E = 0$)	BU426	V_{CBO}	800	V
	BU426A		900	
Collector-emitter voltage ($V_{BE} = 0$)	BU426	V_{CES}	800	V
	BU426A		900	
Collector-emitter voltage ($I_B = 0$)	BU426	V_{CEO}	375	V
	BU426A		400	
Continuous collector current		I_C	6	A
Peak collector current (see Note 1)		I_{CM}	10	A
Continuous base current		I_B	+2, -0.1	A
Peak base current (see Note 1)		I_{BM}	±3	A
Continuous device dissipation at (or below) 50°C case temperature		P_{tot}	70	W
Operating junction temperature range		T_j	-65 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTE 1: This value applies for $t_p \leq 2$ ms, duty cycle $\leq 2\%$.

PRODUCT INFORMATION

Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.



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electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP	MAX	UNIT
$V_{CE(sus)}$ Collector-emitter sustaining voltage	$I_C = 100 \text{ mA}$	$L = 25 \text{ mH}$	(see Note 2)	BU426 BU426A	375 400			V
I_{CES} Collector-emitter cut-off current	$V_{CE} = 800 \text{ V}$ $V_{CE} = 900 \text{ V}$ $V_{CE} = 800 \text{ V}$ $V_{CE} = 900 \text{ V}$	$V_{BE} = 0$ $V_{BE} = 0$ $V_{BE} = 0$ $V_{BE} = 0$	$T_C = 125^\circ\text{C}$ $T_C = 125^\circ\text{C}$	BU426 BU426A BU426 BU426A			1 1 2 2	mA
I_{EBO} Emitter cut-off current	$V_{EB} = 10 \text{ V}$	$I_C = 0$					10	mA
h_{FE} Forward current transfer ratio	$V_{CE} = 5 \text{ V}$	$I_C = 0.6 \text{ A}$	(see Notes 3 and 4)			30	60	
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_B = 0.5 \text{ A}$ $I_B = 1.25 \text{ A}$	$I_C = 2.5 \text{ A}$ $I_C = 4 \text{ A}$	(see Notes 3 and 4)				1.5 3	V
$V_{BE(sat)}$ Base-emitter saturation voltage	$I_B = 0.5 \text{ A}$ $I_B = 1.25 \text{ A}$	$I_C = 2.5 \text{ A}$ $I_C = 4 \text{ A}$	(see Notes 3 and 4)				1.4 1.6	V

NOTES: 2. Inductive loop switching measurement.

3. These parameters must be measured using pulse techniques, $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

4. These parameters must be measured using voltage-sensing contacts, separate from the current carrying contacts.

thermal characteristics

PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JC}$ Junction to case thermal resistance			1.1	$^\circ\text{C/W}$

resistive-load-switching characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			MIN	TYP	MAX	UNIT
t_{on} Turn on time	$I_C = 2.5 \text{ A}$ $V_{CC} = 250 \text{ V}$	$I_{B(on)} = 0.5 \text{ A}$ (see Figures 1 and 2)	$I_{B(off)} = -1 \text{ A}$		0.3	0.6	μs
t_s Storage time					2	3.5	μs
t_f Fall time					0.15		μs
t_f Fall time	$I_C = 2.5 \text{ A}$ $V_{CC} = 250 \text{ V}$	$I_{B(on)} = 0.5 \text{ A}$ $T_C = 95^\circ\text{C}$	$I_{B(off)} = -1 \text{ A}$		0.2	0.75	μs

[†] Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

$t_p = 20 \mu s$
 Duty cycle = 1%
 $V_1 = 15 V$, Source Impedance = 50Ω

Timing diagram for a CMOS inverter. The top trace is the input signal I_C , which is a trapezoidal pulse. The bottom trace is the output signal I_B , which is an inverted trapezoidal pulse. The input pulse has a 10% rise time (B to C) and a 90% plateau (C to E). The output pulse has a 10% fall time (D to A) and a 90% plateau (D to B). The output is labeled $I_{B(on)}$ for the high state and $I_{B(off)}$ for the low state. A note indicates that the output transition time is less than or equal to $2 A / \mu s$.

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TYPICAL CHARACTERISTICS

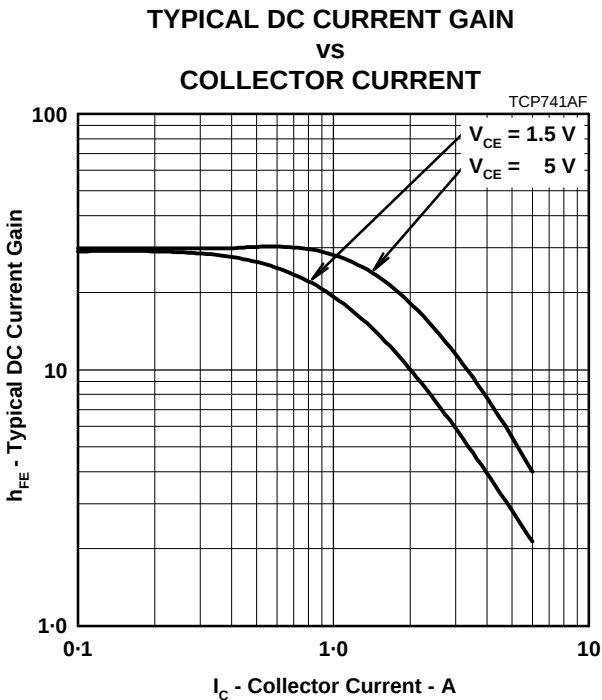


Figure 3.

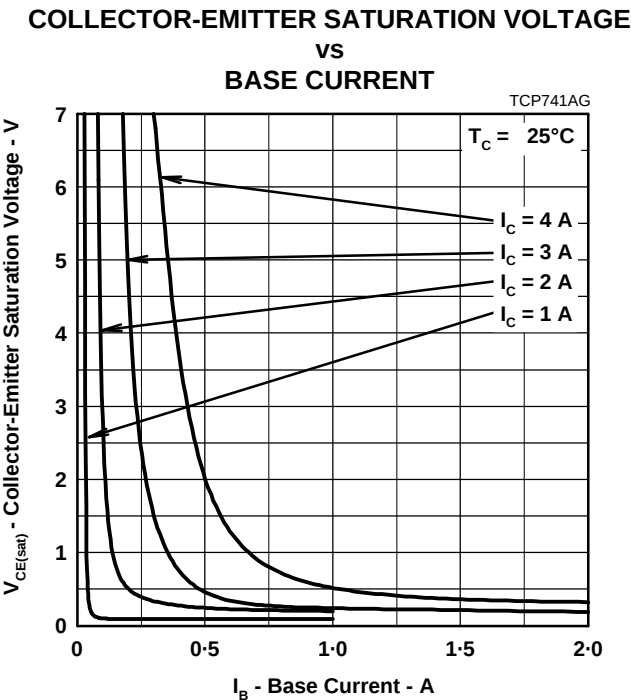


Figure 4.

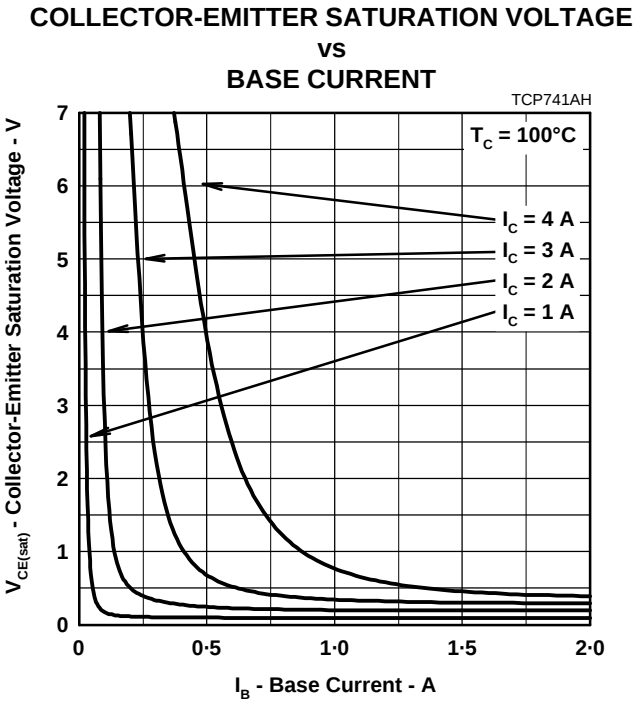


Figure 5.

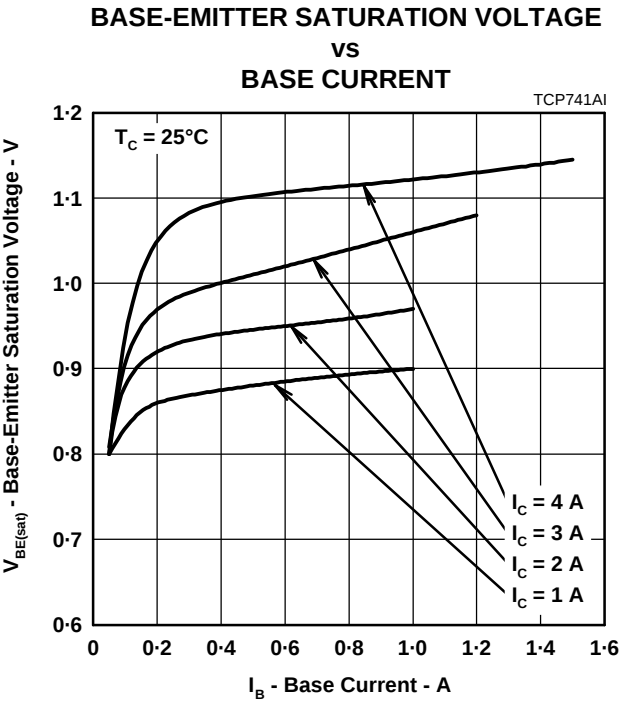


Figure 6.

MAXIMUM SAFE OPERATING REGIONS

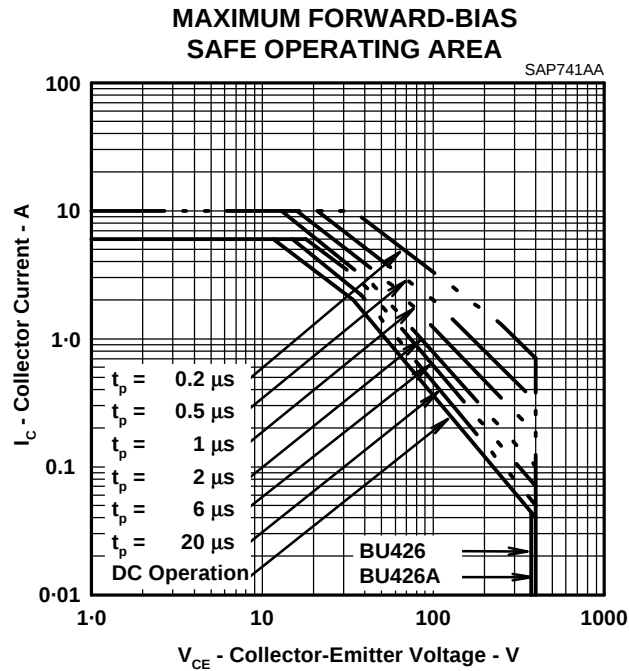


Figure 7.

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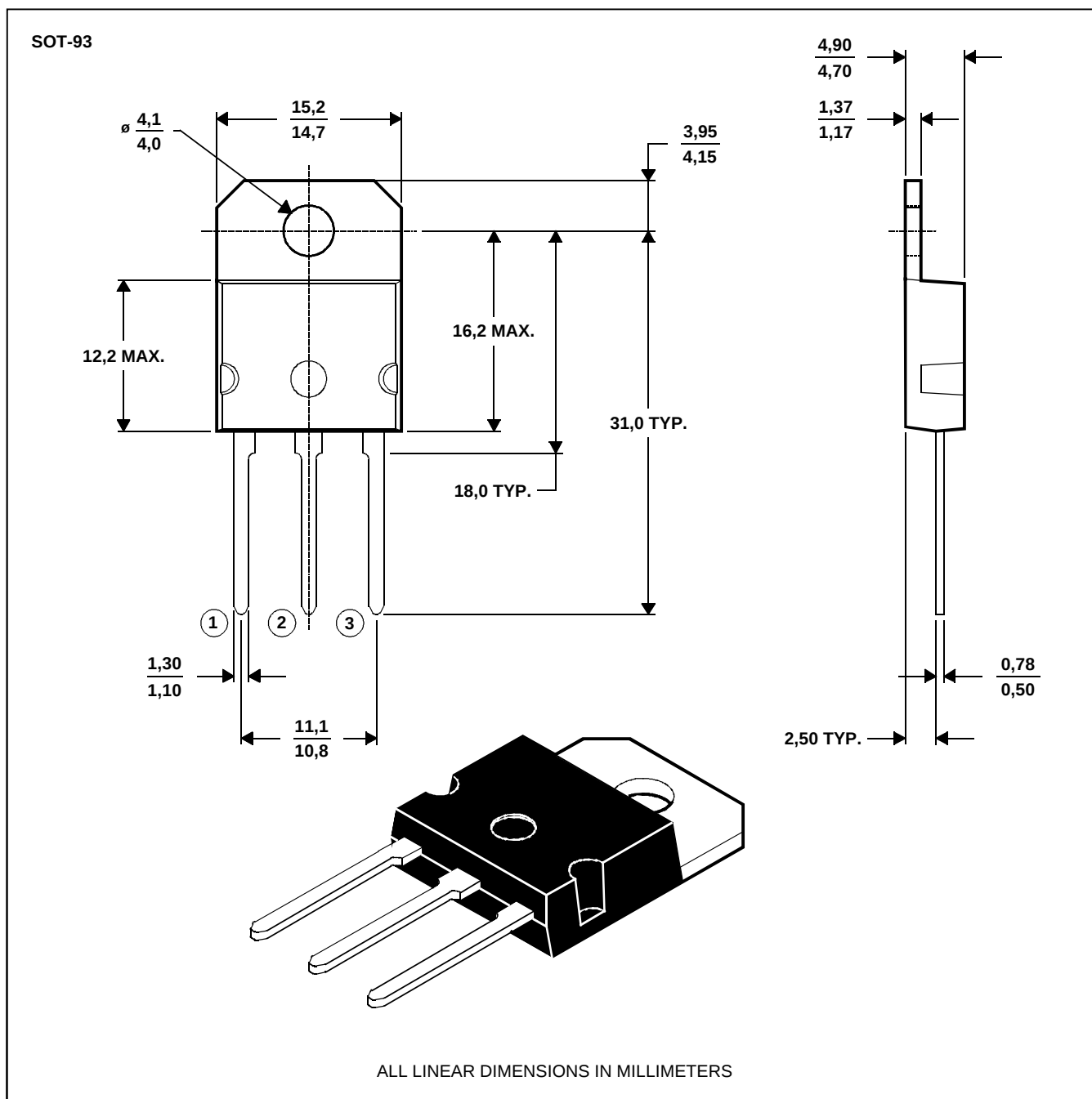
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MECHANICAL DATA

SOT-93

3-pin plastic flange-mount package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: The centre pin is in electrical contact with the mounting tab.

MDXXAW

PRODUCT INFORMATION

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