

2SD1280

Silicon NPN epitaxial planar type

For low-voltage type medium output power amplification

■ Features

- Low collector-emitter saturation voltage $V_{CE(sat)}$
- Satisfactory operation performances at high efficiency with the low-voltage power supply.
- Mini power type package, allowing downsizing of the equipment and automatic insertion through the tape packing and the magazine packing.

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	20	V
Collector-emitter voltage (Base open)	V_{CEO}	20	V
Emitter-base voltage (Collector open)	V_{EBO}	5	V
Collector current	I_C	1	A
Peak collector current	I_{CP}	2	A
Collector power dissipation *	P_C	1	W
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note) *: Printed circuit board: Copper foil area of 1 cm² or more, and the board thickness of 1.7 mm for the collector portion

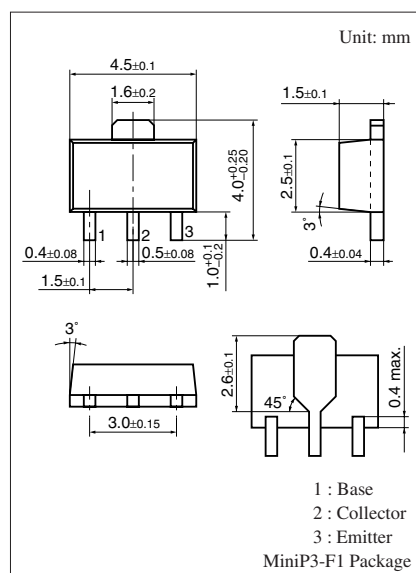
■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = 1 \text{ mA}, I_B = 0$	20			V
Emitter-base voltage (Collector open)	V_{EBO}	$I_E = 10 \mu\text{A}, I_C = 0$	5			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = 10 \text{ V}, I_E = 0$			1	μA
Forward current transfer ratio	h_{FE1} *	$V_{CE} = 2 \text{ V}, I_C = 0.5 \text{ A}$	90		280	—
	h_{FE2}	$V_{CE} = 2 \text{ V}, I_C = 1.5 \text{ A}$	50			
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 1 \text{ A}, I_B = 50 \text{ mA}$			0.5	V
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = 500 \text{ mA}, I_B = 50 \text{ mA}$			1.2	V
Transition frequency	f_T	$V_{CB} = 6 \text{ V}, I_E = -50 \text{ mA}, f = 200 \text{ MHz}$		150		MHz
Collector output capacitance (Common base, input open circuited)	C_{ob}	$V_{CB} = 6 \text{ V}, I_E = 0, f = 1 \text{ MHz}$		18		pF

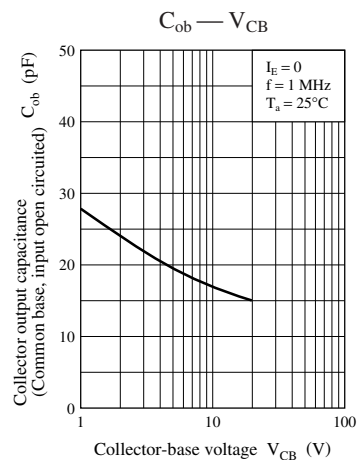
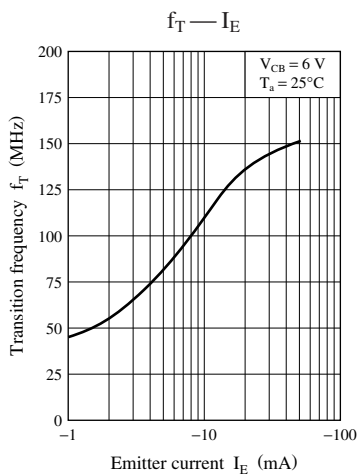
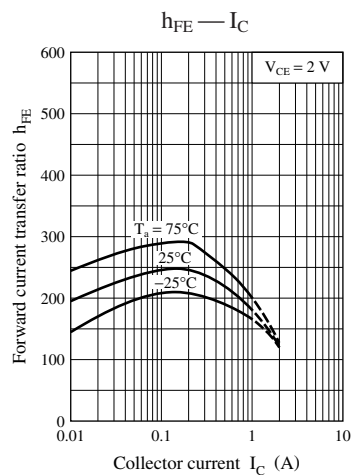
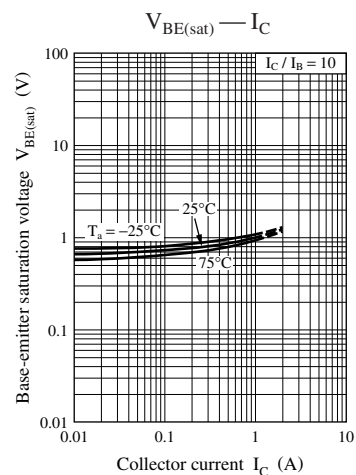
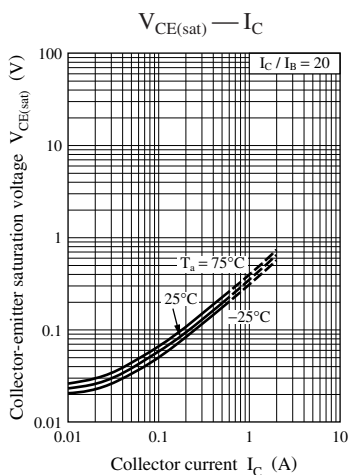
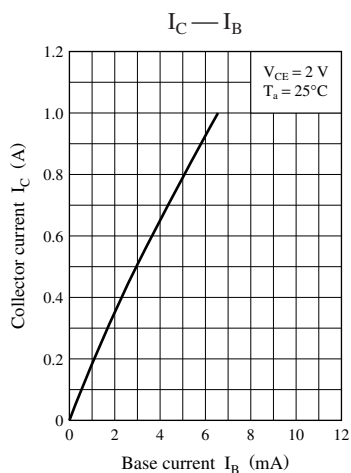
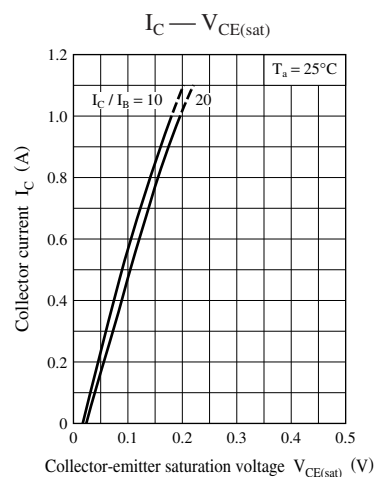
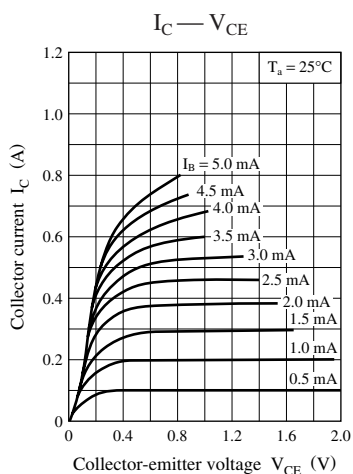
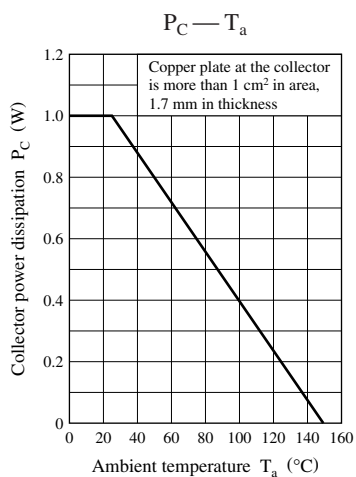
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

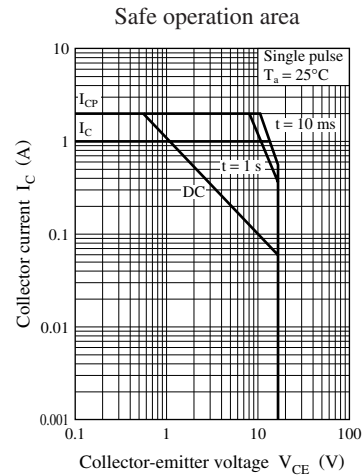
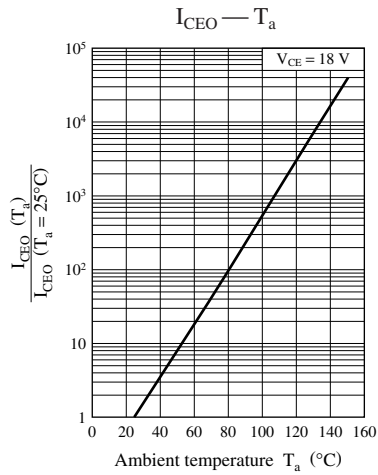
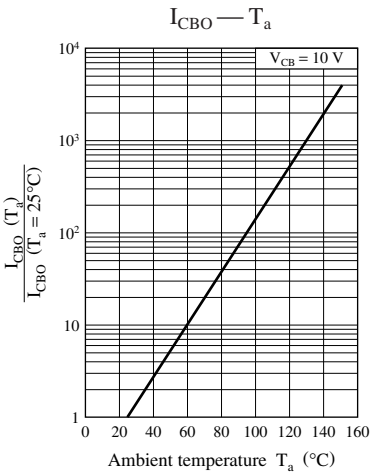
2. *: Rank classification

Rank	Q	R	S
h_{FE1}	90 to 155	130 to 210	180 to 280



Marking Symbol: R





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