

**IRF1407S**  
**IRF1407L**

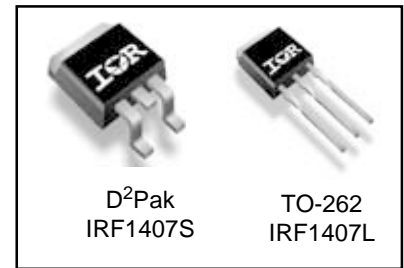
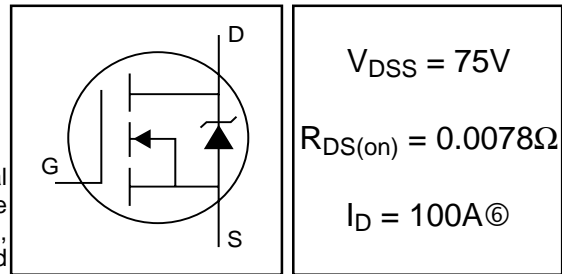
**Benefits**

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

**Description**

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications. The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRF1407L) is available for low-profile applications.

HEXFET® Power MOSFET



**Absolute Maximum Ratings**

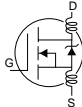
	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V®	100®	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V®	70®	
I <sub>DM</sub>	Pulsed Drain Current ①®	520	
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Power Dissipation	3.8	W
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy®②	390	mJ
I <sub>AR</sub>	Avalanche Current①	See Fig.12a, 12b, 15, 16	A
E <sub>AR</sub>	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③®	4.6	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Thermal Resistance**

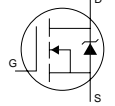
	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	0.75	°C/W
R <sub>θJA</sub>	Junction-to-Ambient(PCB Mounted, steady-state)**	—	40	

\*\*When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.09	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑧
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.0078	$\Omega$	$V_{GS} = 10V, I_D = 78A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	74	—	—	S	$V_{DS} = 25V, I_D = 78A$ ⑧
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 60V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	160	250	nC	$I_D = 78A$
$Q_{gs}$	Gate-to-Source Charge	—	35	52		$V_{DS} = 60V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	54	81		$V_{GS} = 10V$ ④ ⑧
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 38V$
$t_r$	Rise Time	—	150	—		$I_D = 78A$
$t_{d(off)}$	Turn-Off Delay Time	—	150	—		$R_G = 2.5\Omega$
$t_f$	Fall Time	—	140	—		$V_{GS} = 10V$ ④ ⑧
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	5600	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	890	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	190	—		$f = 1.0\text{KHz}$ , See Fig. 5 ⑧
$C_{oss}$	Output Capacitance	—	5800	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{KHz}$
$C_{oss}$	Output Capacitance	—	560	—		$V_{GS} = 0V, V_{DS} = 60V, f = 1.0\text{KHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	1100	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$

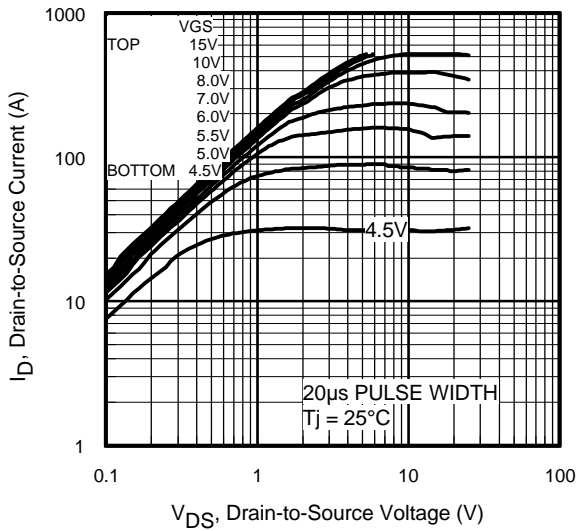
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	100 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	520		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 78A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	110	170	ns	$T_J = 25^\circ\text{C}, I_F = 78A$
$Q_{rr}$	Reverse Recovery Charge	—	390	590	nC	$di/dt = 100A/\mu s$ ④ ⑧
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

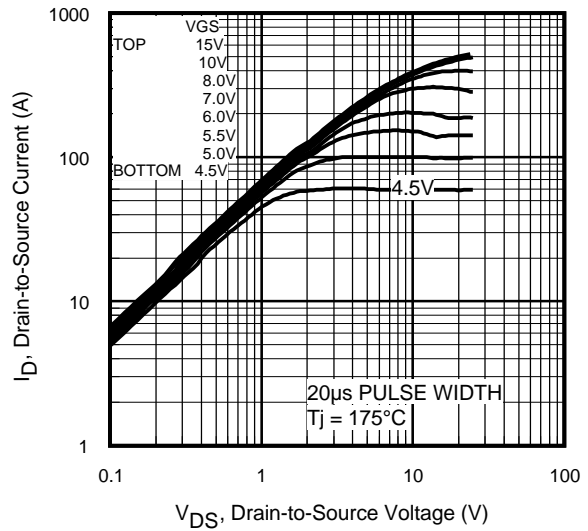
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.13\text{mH}$   
 $R_G = 25\Omega, I_{AS} = 78A$ . (See Figure 12).
- ③  $I_{SD} \leq 78A, di/dt \leq 320A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .

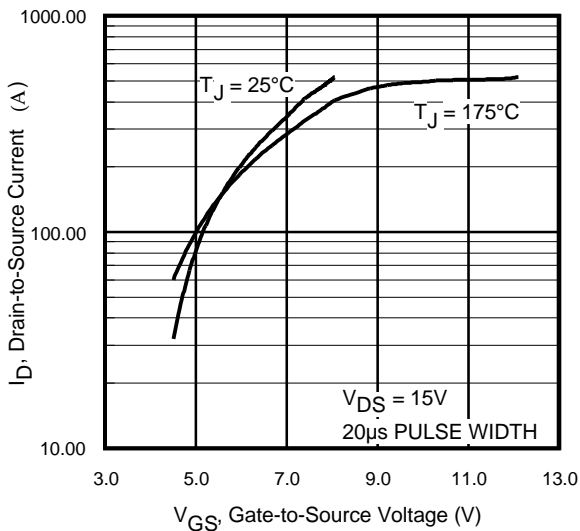
- ⑤  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑦ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑧ Uses IRF1407 data and test conditions.



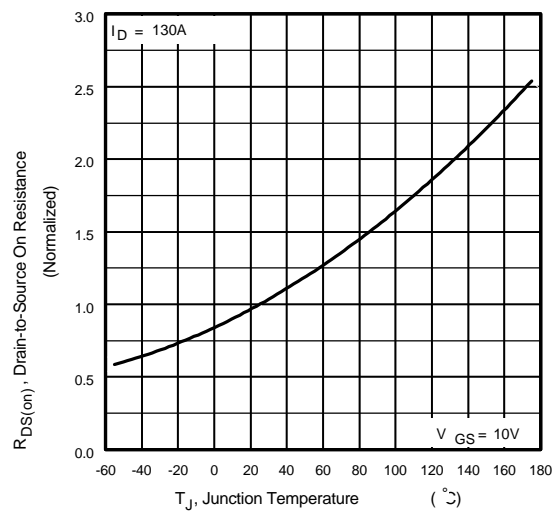
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



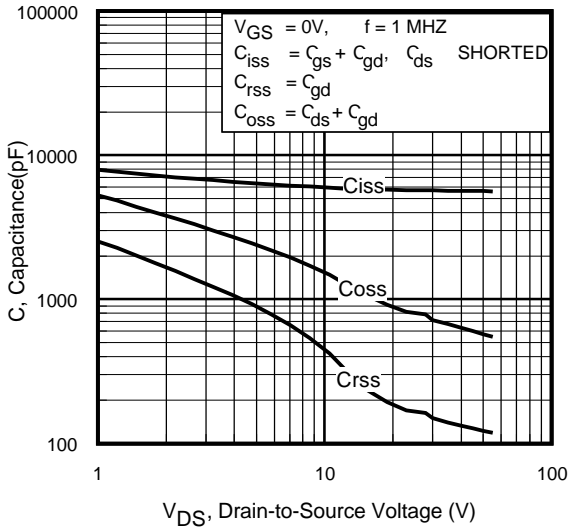
**Fig 3.** Typical Transfer Characteristics



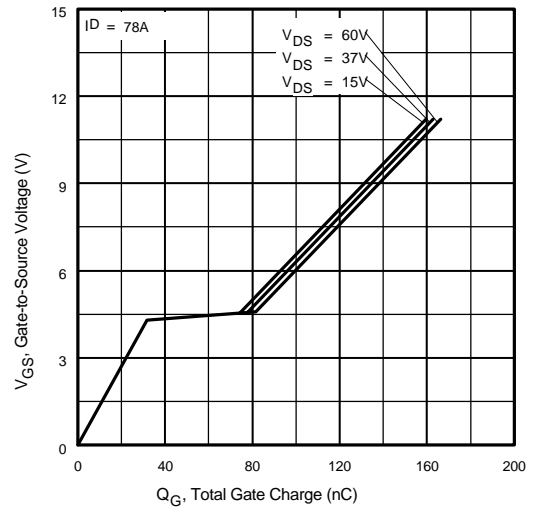
**Fig 4.** Normalized On-Resistance Vs. Temperature

# IRF1407S/IRF1407L

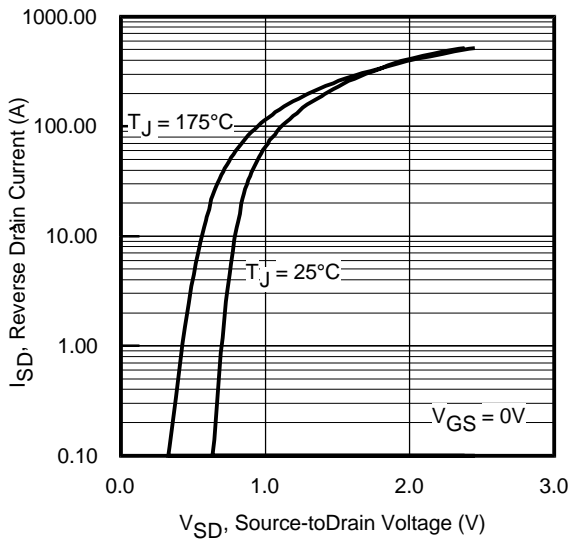
International  
**IR** Rectifier



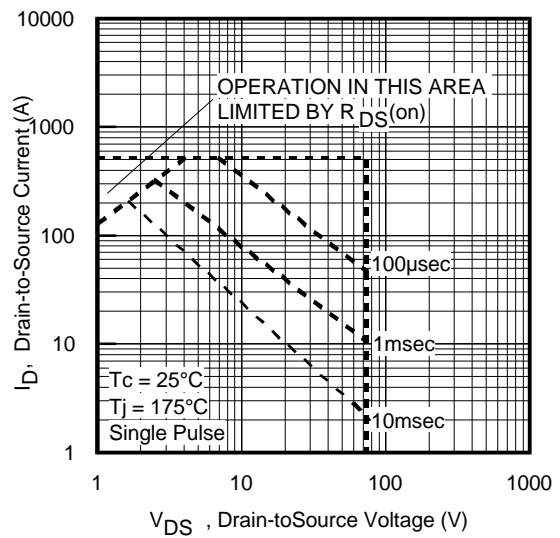
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



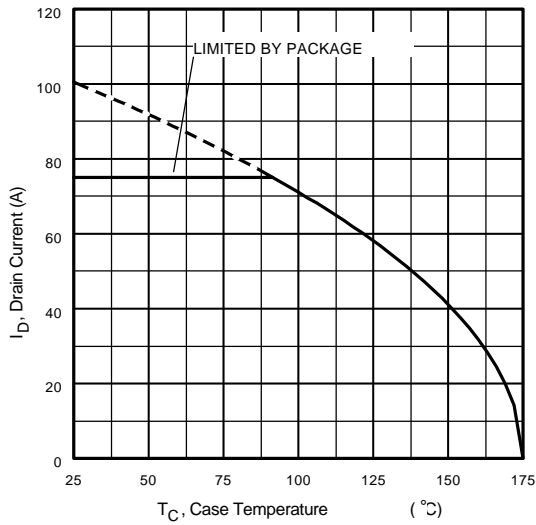
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



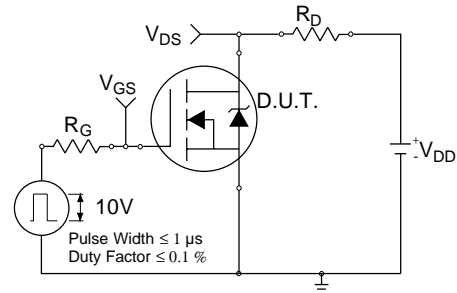
**Fig 7.** Typical Source-Drain Diode Forward Voltage



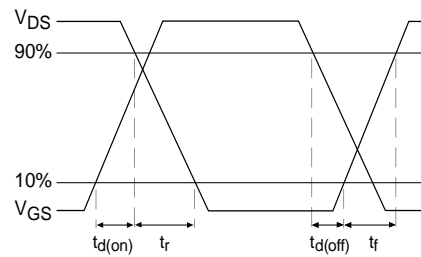
**Fig 8.** Maximum Safe Operating Area



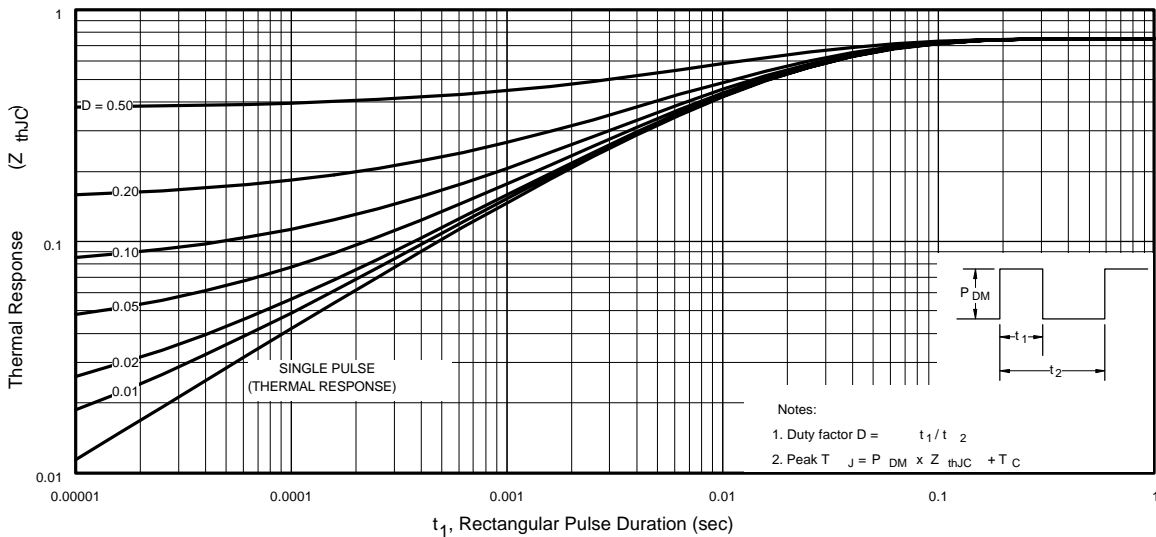
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



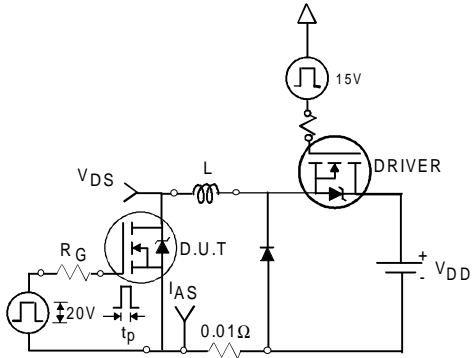
**Fig 10b.** Switching Time Waveforms



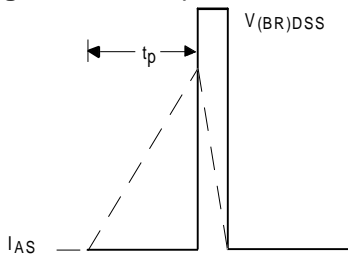
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRF1407S/IRF1407L

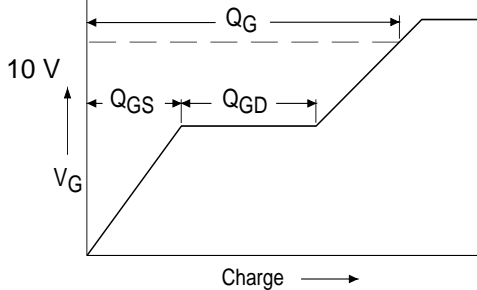
International  
**IR** Rectifier



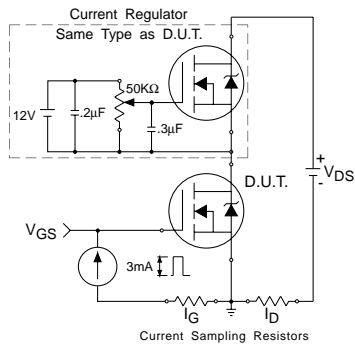
**Fig 12a.** Unclamped Inductive Test Circuit



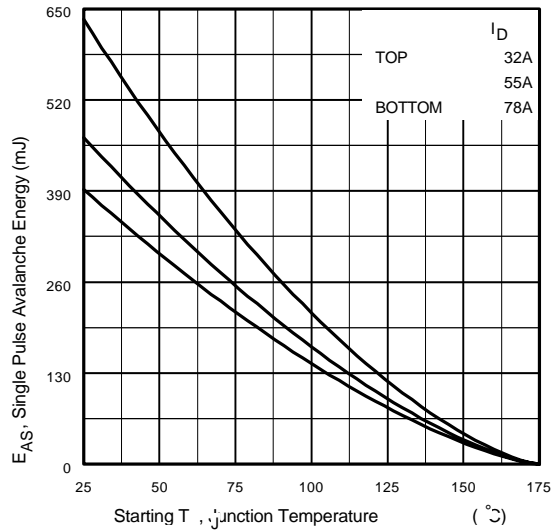
**Fig 12b.** Unclamped Inductive Waveforms



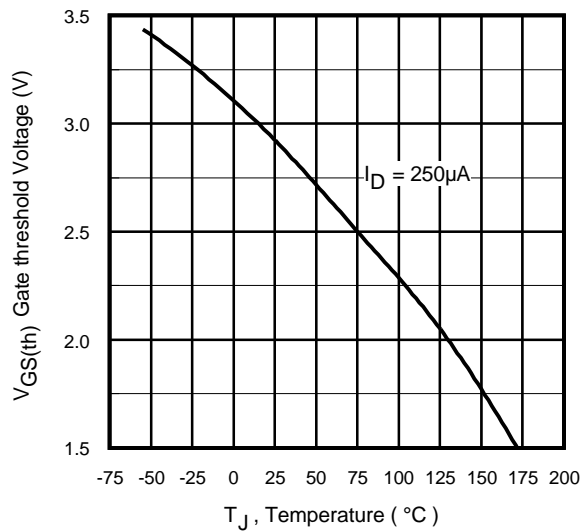
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Threshold Voltage Vs. Temperature

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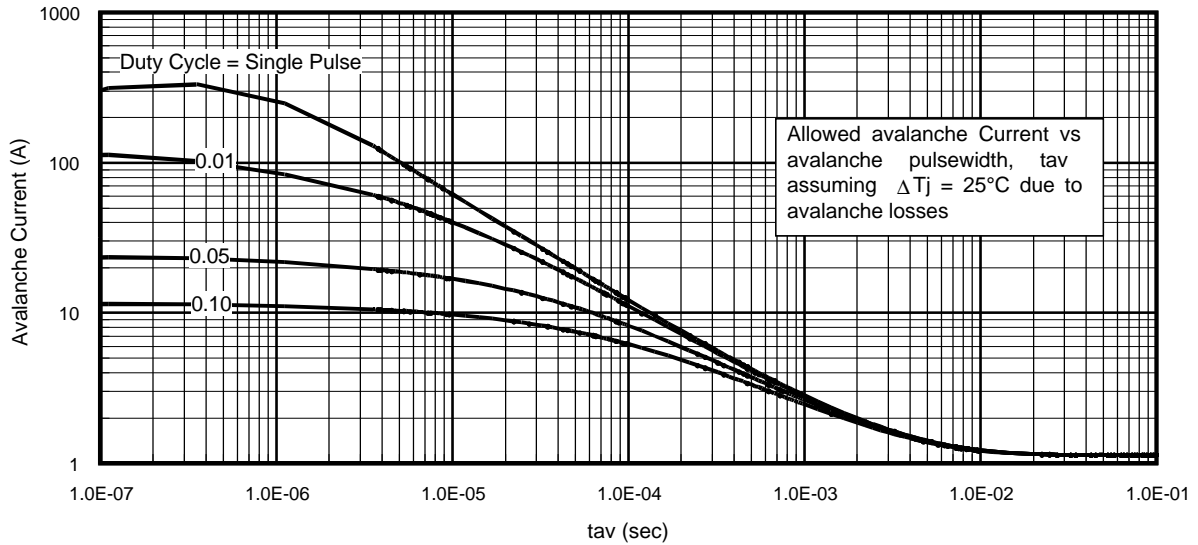


Fig 15. Typical Avalanche Current Vs. Pulsewidth

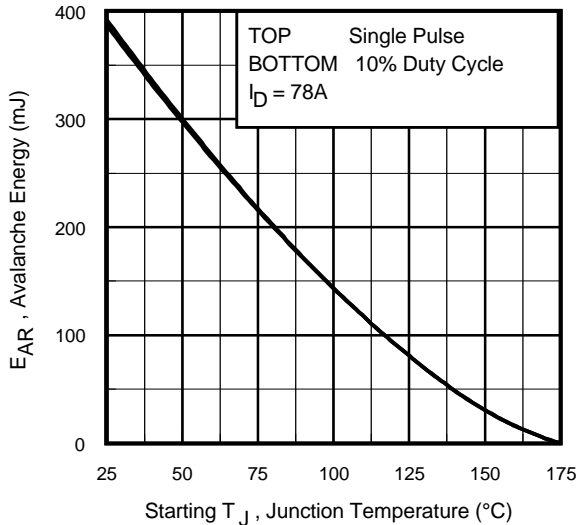


Fig 16. Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

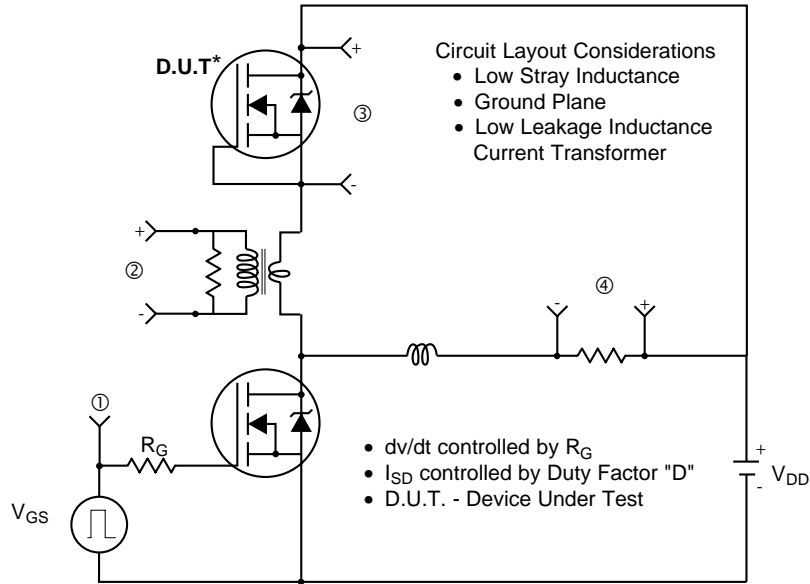
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

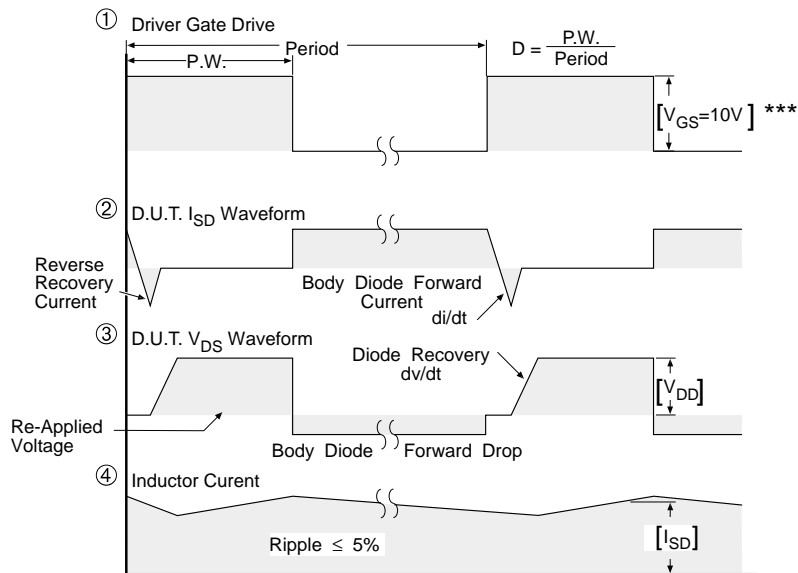
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



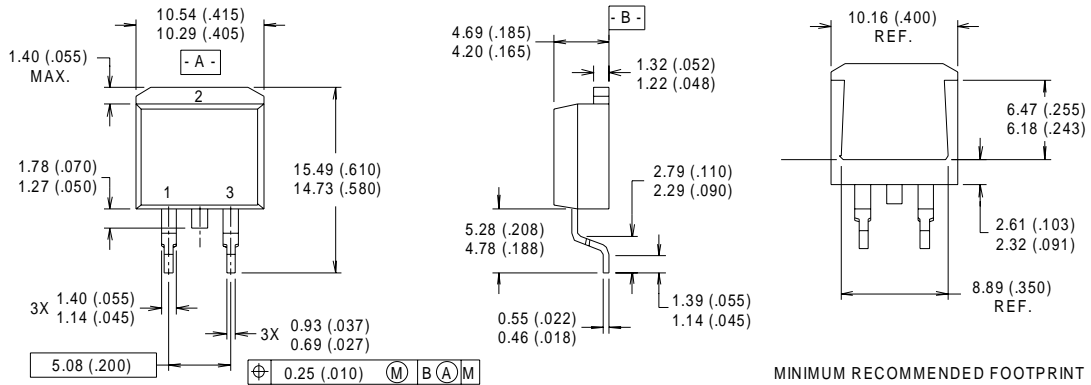
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 17.** For N-channel HEXFET® power MOSFETs



## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)

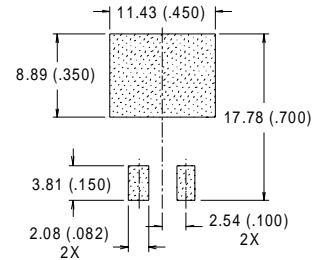


**NOTES:**

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

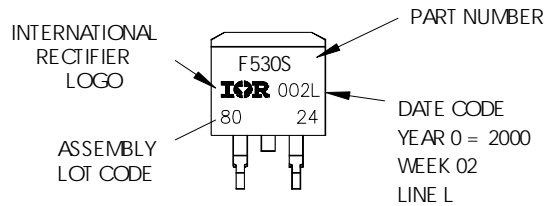
**LEAD ASSIGNMENTS**

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE



## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
 LOT CODE 8024  
 ASSEMBLED ON WW02, 2000  
 IN THE ASSEMBLY LINE "L"

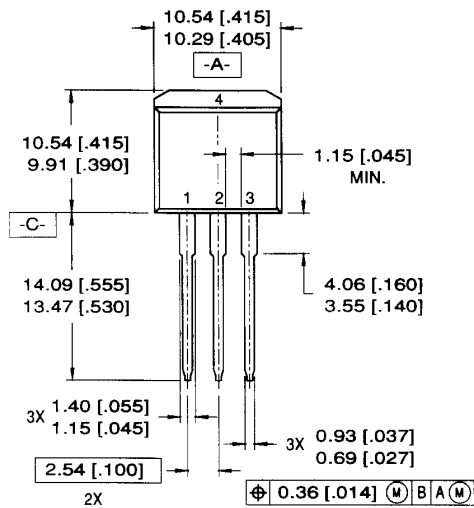


# IRF1407S/IRF1407L

International  
**IR** Rectifier

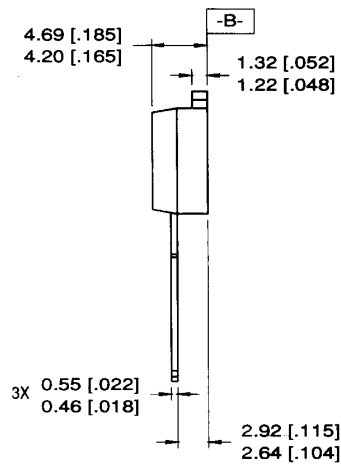
## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



### LEAD ASSIGNMENTS

1 = GATE      3 = SOURCE  
2 = DRAIN      4 = DRAIN

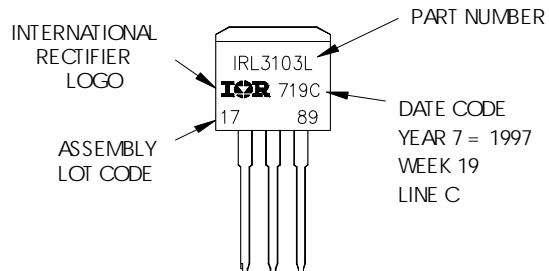


### NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

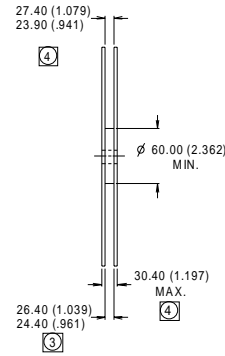
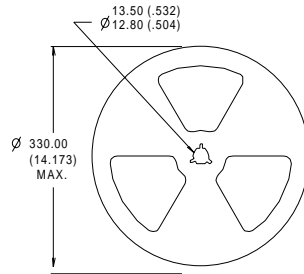
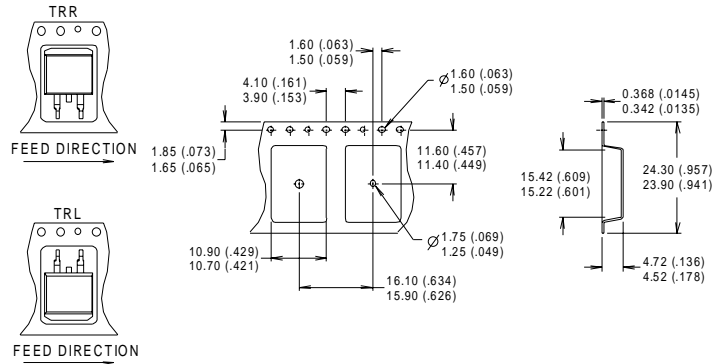
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION MEASURED @ HUB.
  4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.