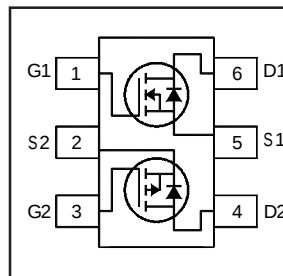


IRF5851

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Low Gate Charge

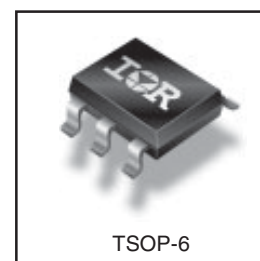


	N-Ch	P-Ch
V_{DS}	20V	-20V
$R_{DS(on)}$	0.090 Ω	0.135 Ω

Description

These N and P channel MOSFETs from International Rectifier utilize advanced processing techniques to achieve the extremely low on-resistance per silicon area. This benefit provides the designer with an extremely efficient device for use in battery and load management applications.

This Dual TSOP-6 package is ideal for applications where printed circuit board space is at a premium and where maximum functionality is required. With two die per package, the IRF5851 can provide the functionality of two SOT-23 packages in a smaller footprint. Its unique thermal design and $R_{DS(on)}$ reduction enables an increase in current-handling capability.



Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
V _{DS}	Drain-to-Source Voltage	20	-20	A
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	2.7	-2.2	
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	2.2	-1.7	
I _{DM}	Pulsed Drain Current ①	11	-9.0	
P _D @T _A = 25°C	Power Dissipation ③	0.96		W
P _D @T _A = 70°C	Power Dissipation ③	0.62		
	Linear Derating Factor	7.7		mW/°C
V _{GS}	Gate-to-Source Voltage	± 12		V
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ③	—	130	$^\circ\text{C/W}$

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-20	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.016	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
		P-Ch	—	-0.011	—		Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.090	Ω	$V_{GS} = 4.5V, I_D = 2.7A$ ②
			—	—	0.120		$V_{GS} = 2.5V, I_D = 2.2A$ ②
		P-Ch	—	—	0.135		$V_{GS} = -4.5V, I_D = -2.2A$ ②
			—	—	0.220		$V_{GS} = -2.5V, I_D = -1.7A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	0.60	—	1.25	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-0.45	—	-1.2		$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	N-Ch	5.2	—	—	S	$V_{DS} = 10V, I_D = 2.7A$ ②
		P-Ch	3.5	—	—		$V_{DS} = -10V, I_D = -2.2A$ ②
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{DS} = 16V, V_{GS} = 0V$
		P-Ch	—	—	-1.0		$V_{DS} = -16V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 16V, V_{GS} = 0V, T_J = 70^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100		$V_{GS} = \pm 12V$
Q_g	Total Gate Charge	N-Ch	—	4.0	6.0		N-Channel $I_D = 2.7A, V_{DS} = 10V, V_{GS} = 4.5V$ ②
		P-Ch	—	3.6	5.4		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	0.95	—	nC	P-Channel $I_D = -2.2A, V_{DS} = -10V, V_{GS} = -4.5V$
		P-Ch	—	0.66	—		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	0.83	—		N-Channel $V_{DD} = 10V, I_D = 1.0A, R_G = 6.2\Omega, V_{GS} = 4.5V$ ②
		P-Ch	—	5.7	—		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	6.6	—	ns	P-Channel $V_{DD} = -10V, I_D = -1.0A, R_G = 6.0\Omega, V_{GS} = -4.5V$ ②
t_r	Rise Time	N-Ch	—	1.2	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	15	—		
t_f	Fall Time	N-Ch	—	2.4	—		
C_{iss}	Input Capacitance	N-Ch	—	400	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$
		P-Ch	—	320	—		
C_{oss}	Output Capacitance	N-Ch	—	48	—		P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$
		P-Ch	—	56	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	32	—		
		P-Ch	—	40	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	0.96	A	
		P-Ch	—	—	-0.96		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	11		
		P-Ch	—	—	-9.0		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 0.96A, V_{GS} = 0V$ ②
		P-Ch	—	—	-1.2		$T_J = 25^\circ\text{C}, I_S = -0.96A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	N-Ch	—	25	38	ns	N-Channel $T_J = 25^\circ\text{C}, I_F = 0.96A, di/dt = 100A/\mu s$
		P-Ch	—	23	35		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	6.5	9.8	nC	P-Channel $T_J = 25^\circ\text{C}, I_F = -0.96A, di/dt = -100A/\mu s$ ②
		P-Ch	—	7.7	12		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 10 & 26)
 ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

- ③ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

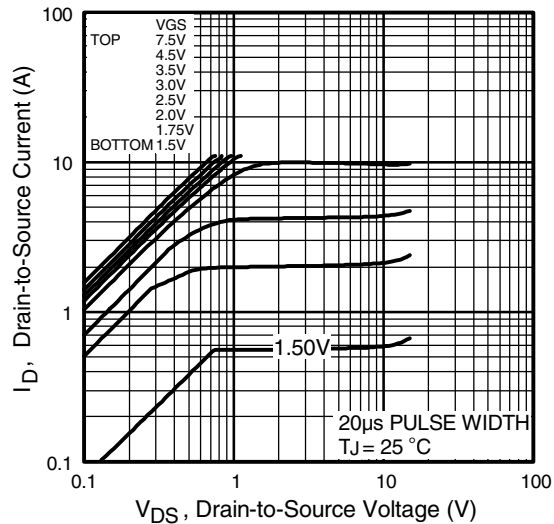


Fig 1. Typical Output Characteristics

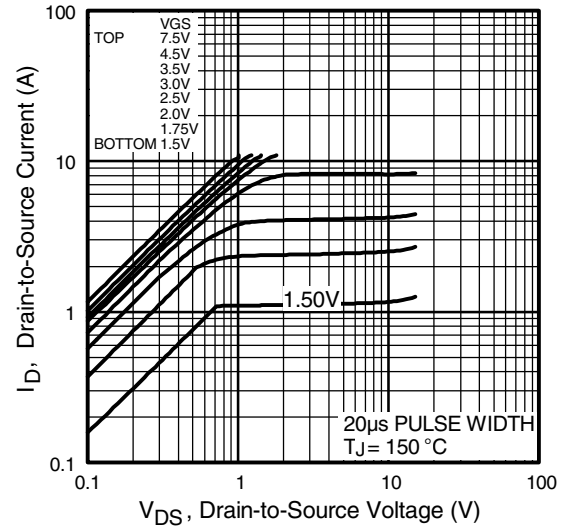


Fig 2. Typical Output Characteristics

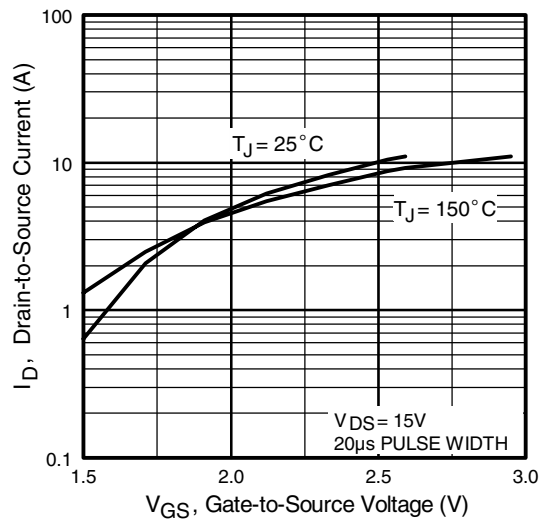


Fig 3. Typical Transfer Characteristics

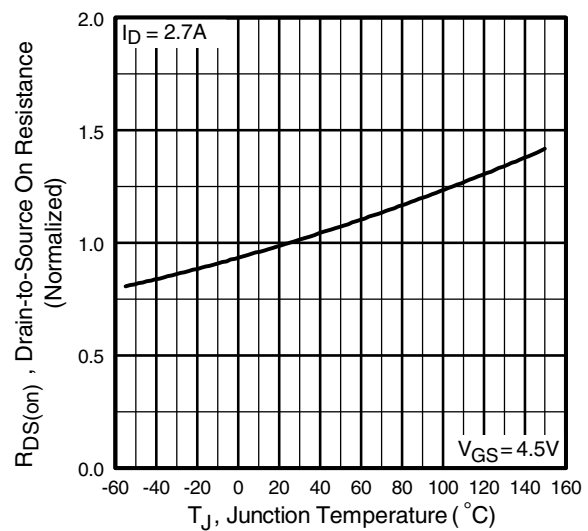


Fig 4. Normalized On-Resistance Vs. Temperature

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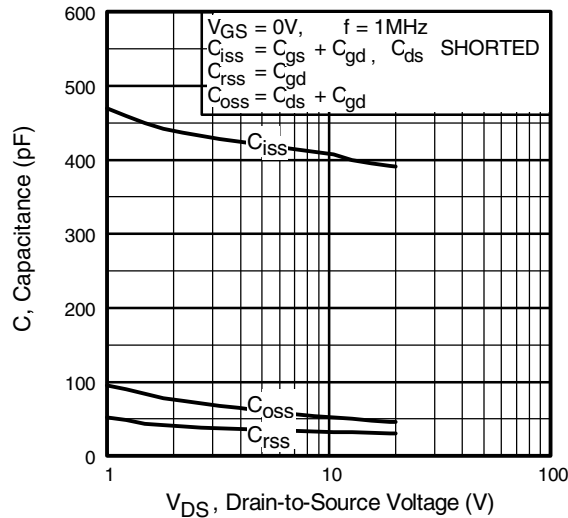


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

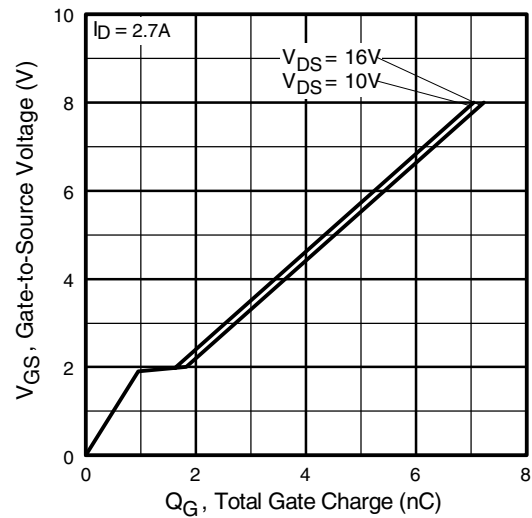


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

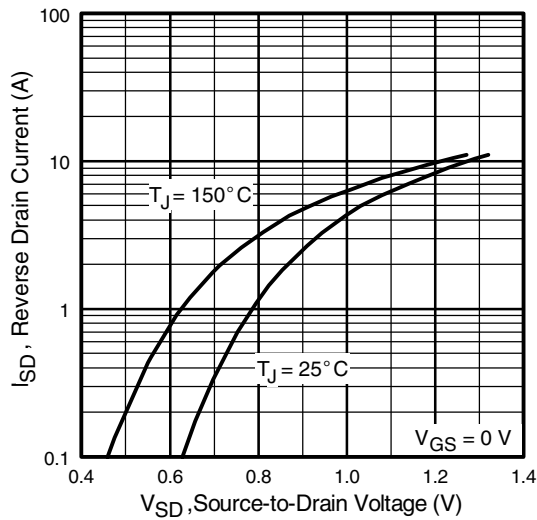


Fig 7. Typical Source-Drain Diode Forward Voltage

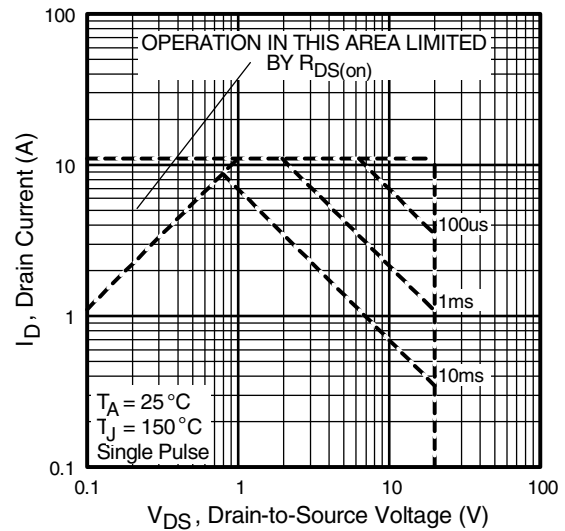


Fig 8. Maximum Safe Operating Area

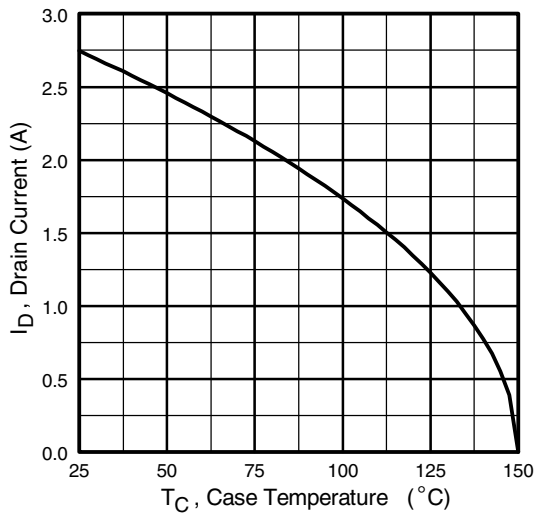


Fig 9. Maximum Drain Current Vs. Case Temperature

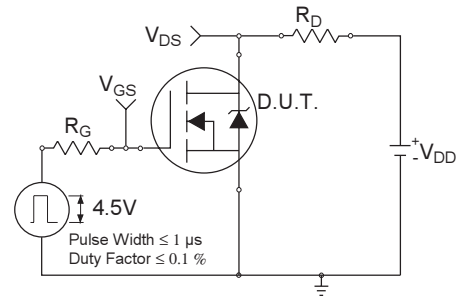


Fig 10a. Switching Time Test Circuit

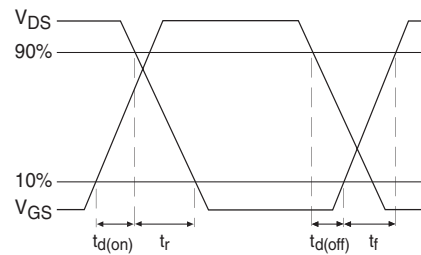


Fig 10b. Switching Time Waveforms

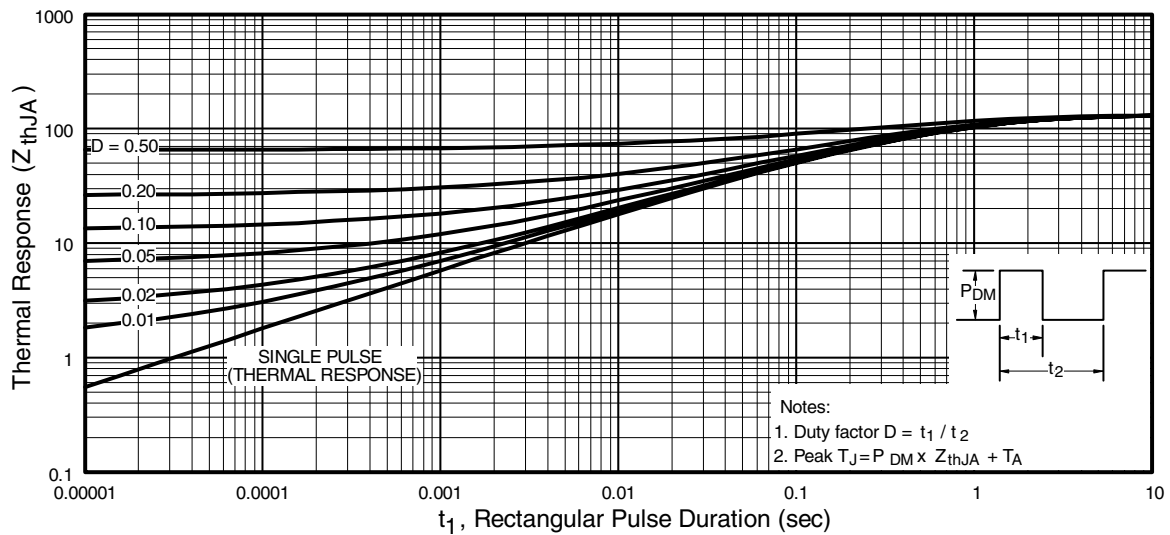


Fig 10. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

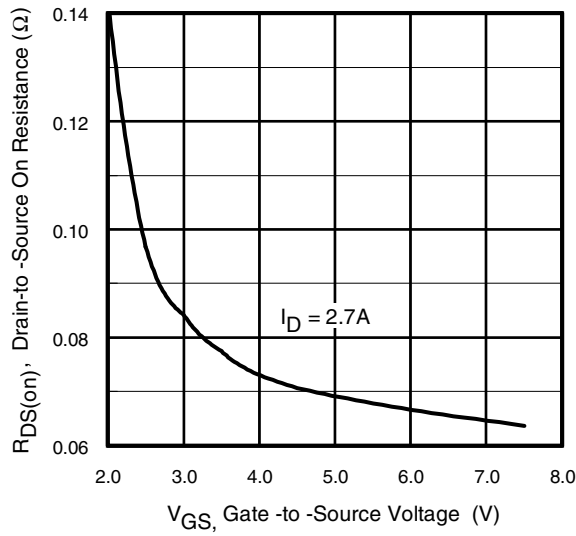


Fig 11. Typical On-Resistance Vs. Gate Voltage

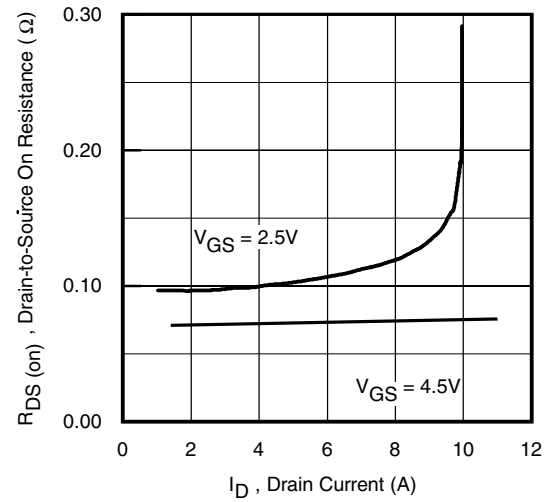


Fig 12. Typical On-Resistance Vs. Drain Current

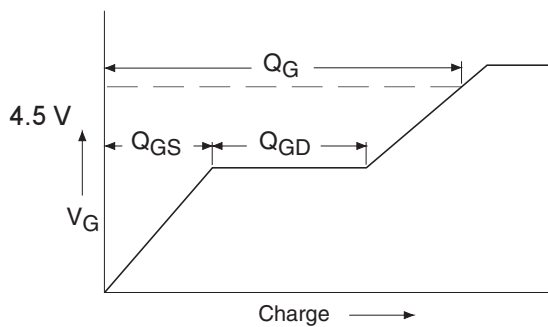


Fig 13a. Basic Gate Charge Waveform

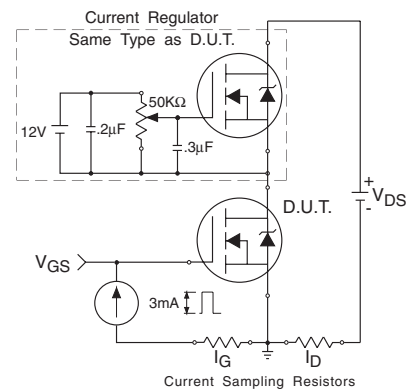


Fig 13b. Gate Charge Test Circuit

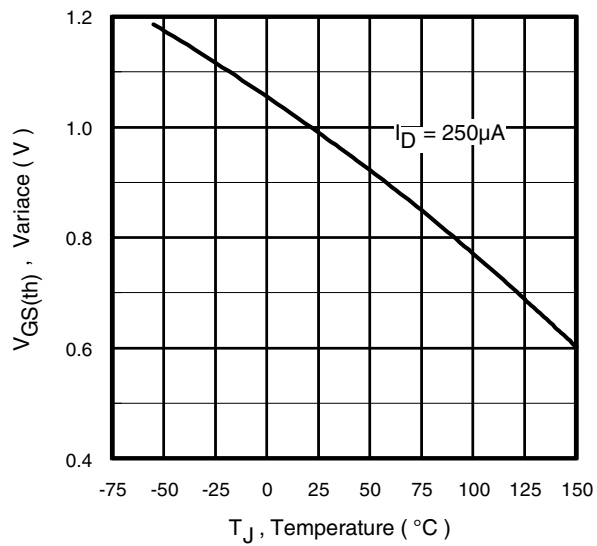


Fig 14. Threshold Voltage Vs. Temperature

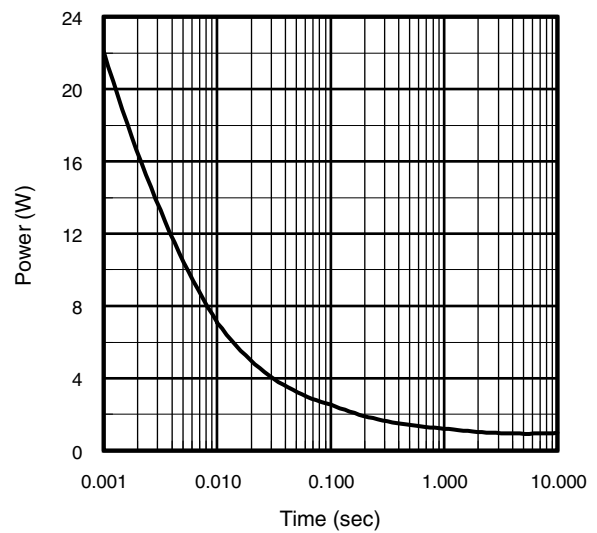


Fig 15. Typical Power Vs. Time

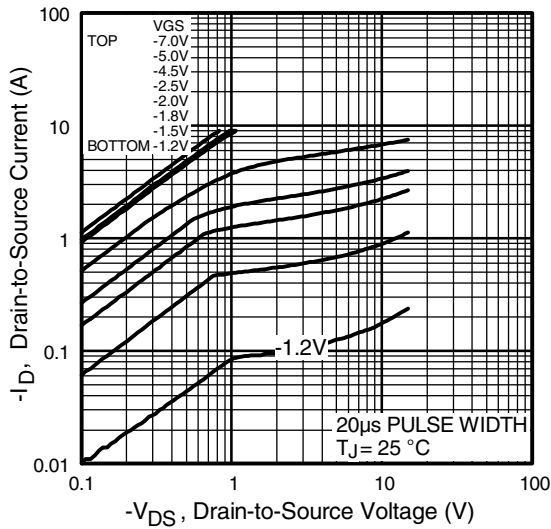


Fig 16. Typical Output Characteristics

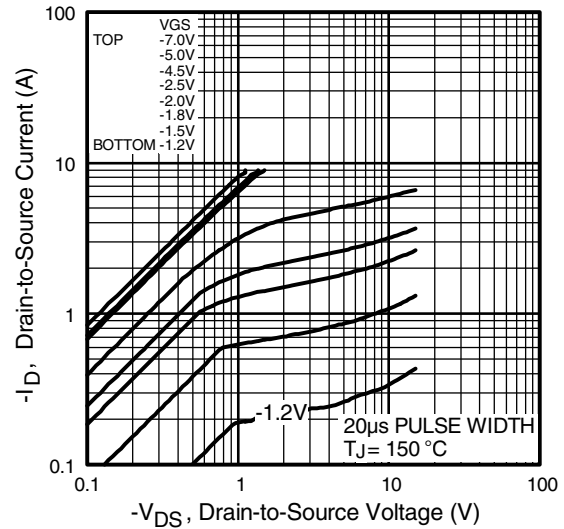


Fig 17. Typical Output Characteristics

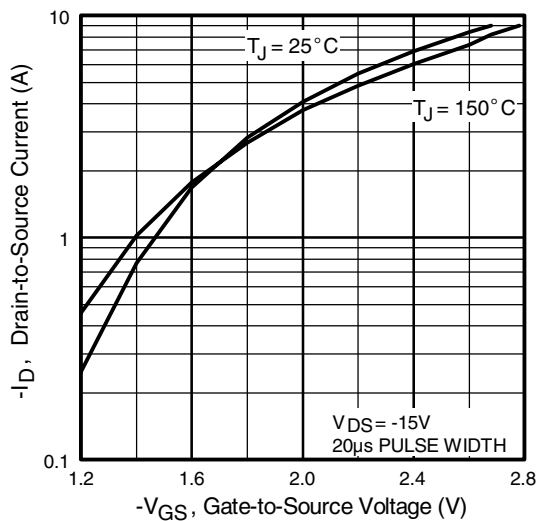


Fig 18. Typical Transfer Characteristics

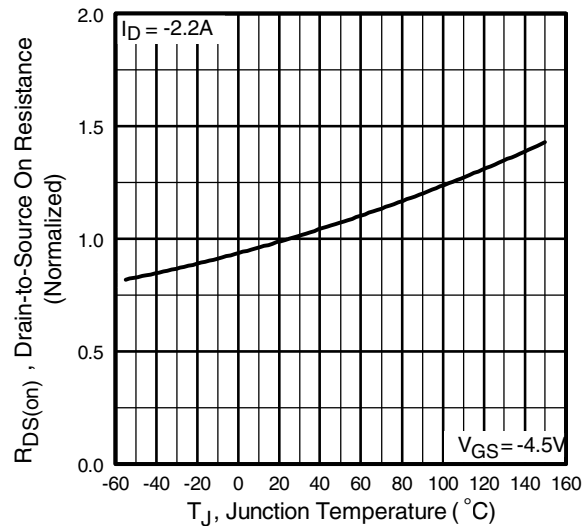


Fig 19. Normalized On-Resistance
Vs. Temperature

P-Channel

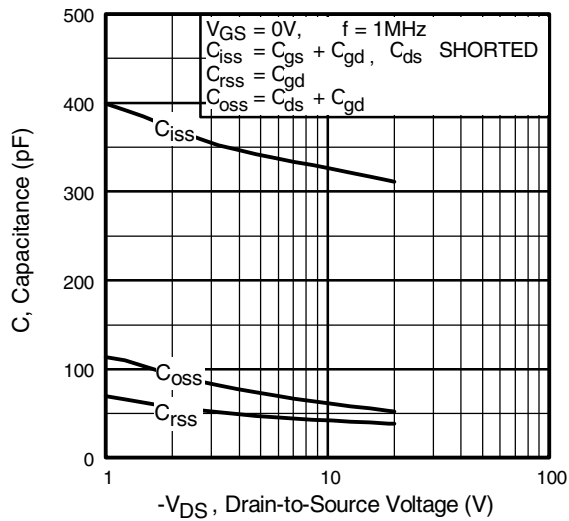


Fig 20. Typical Capacitance Vs. Drain-to-Source Voltage

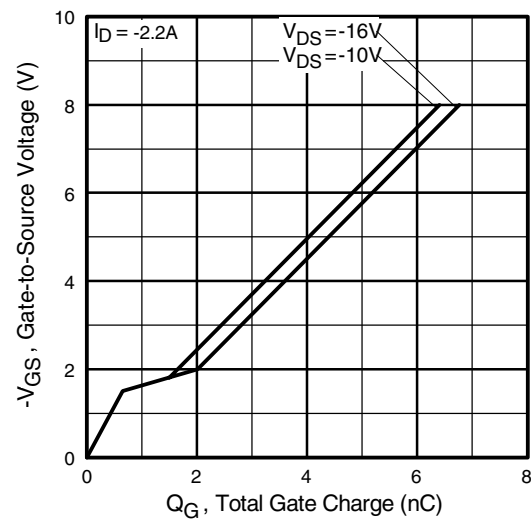


Fig 21. Typical Gate Charge Vs. Gate-to-Source Voltage

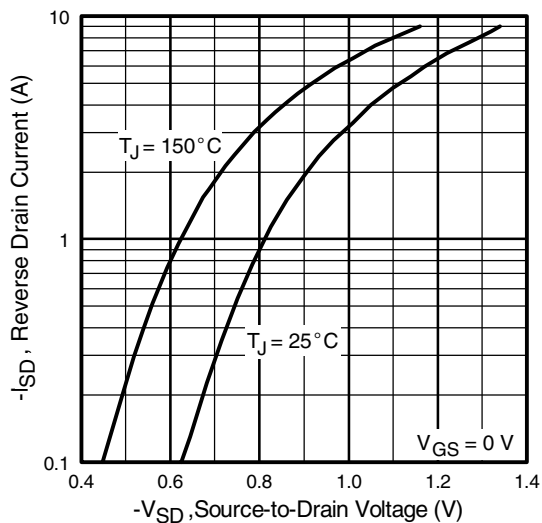


Fig 22. Typical Source-Drain Diode Forward Voltage

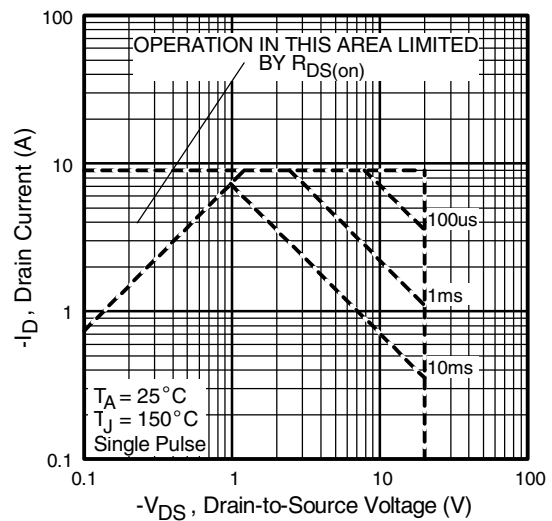


Fig 23. Maximum Safe Operating Area

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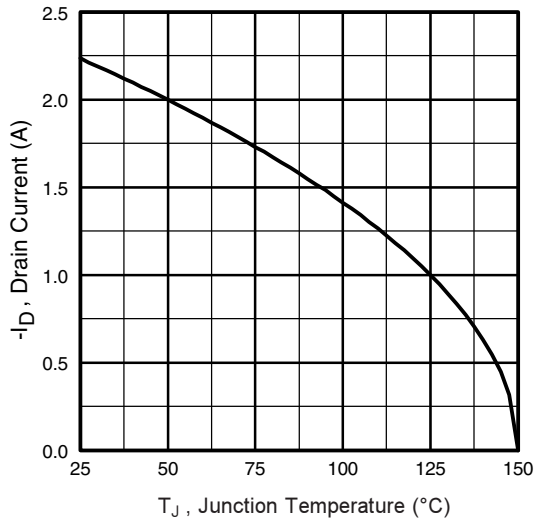


Fig 24. Maximum Drain Current Vs. Junction Temperature

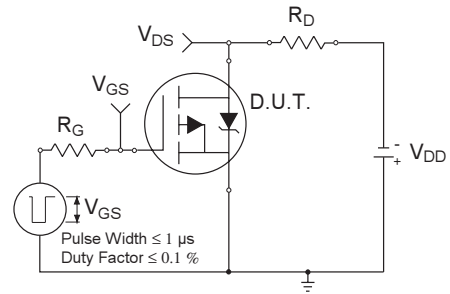


Fig 25a. Switching Time Test Circuit

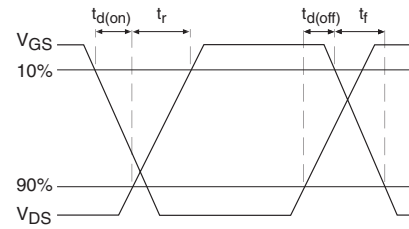


Fig 25b. Switching Time Waveforms

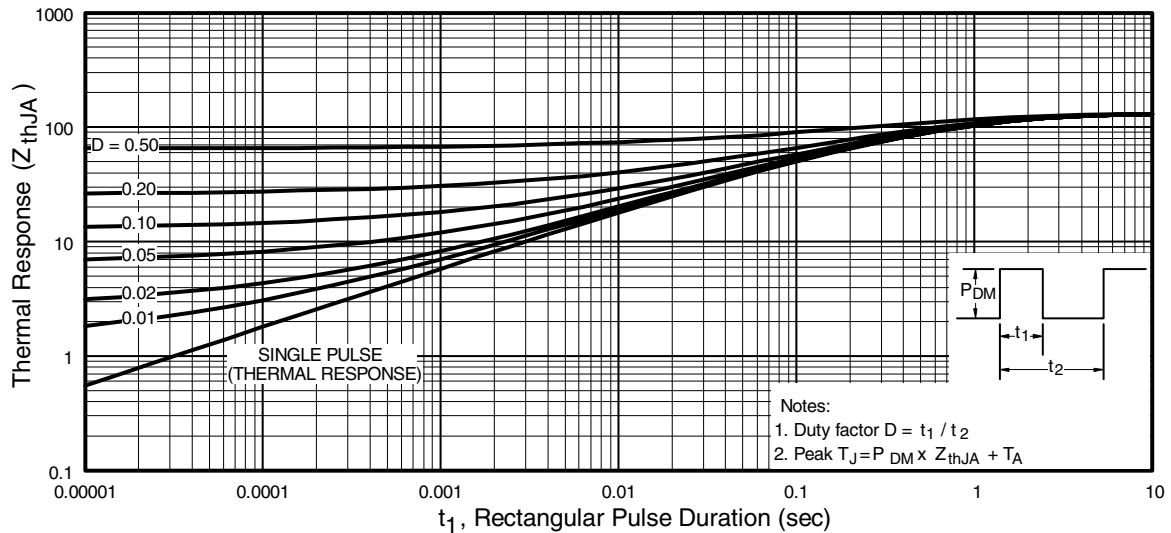


Fig 26. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

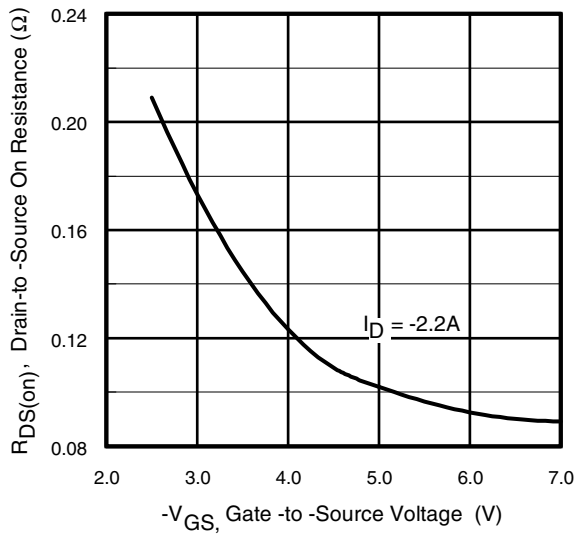


Fig 27. Typical On-Resistance Vs. Gate Voltage

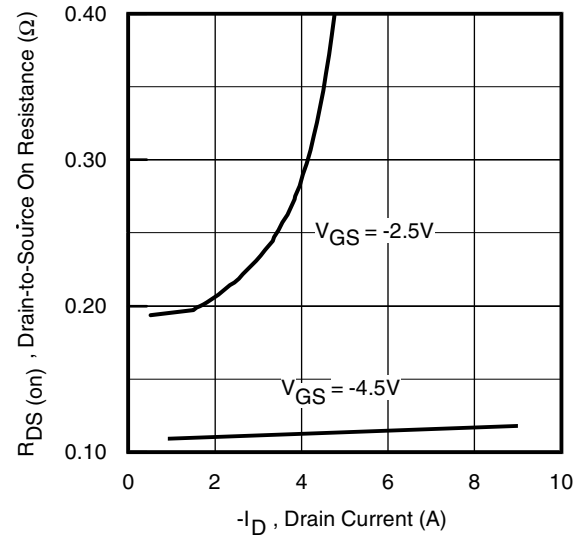


Fig 28. Typical On-Resistance Vs. Drain Current

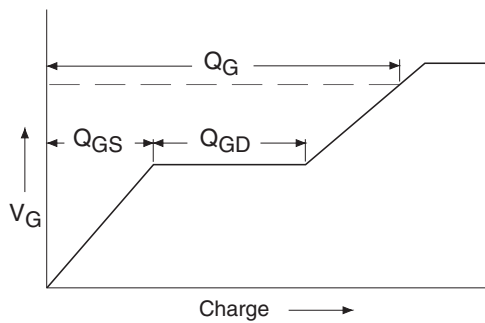


Fig 29a. Basic Gate Charge Waveform

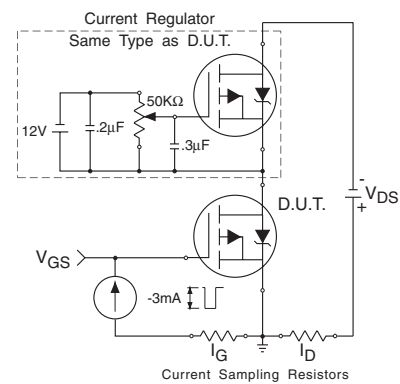


Fig 29b. Gate Charge Test Circuit

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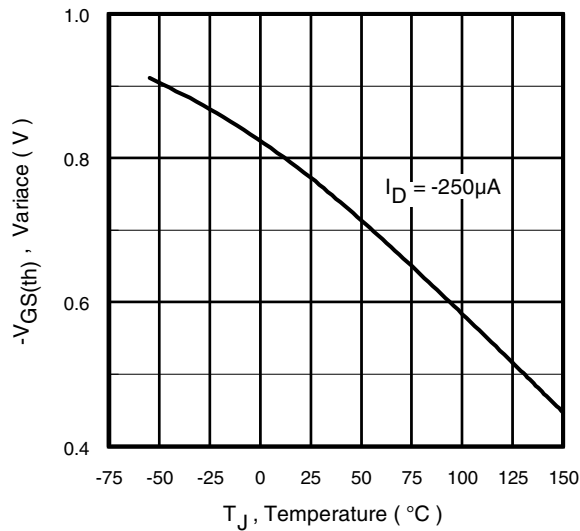


Fig 30. Threshold Voltage Vs. Temperature

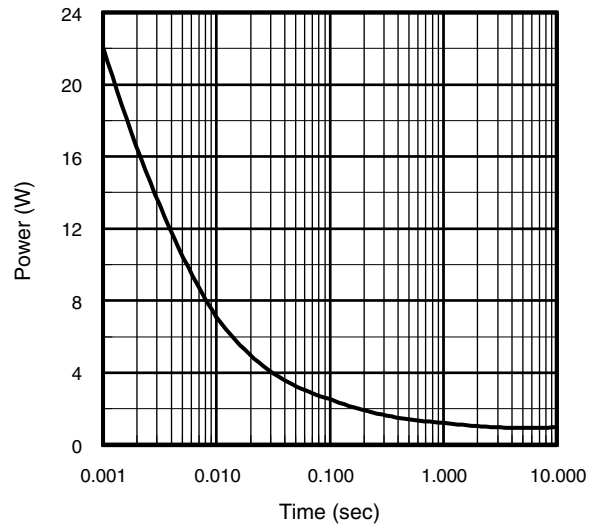
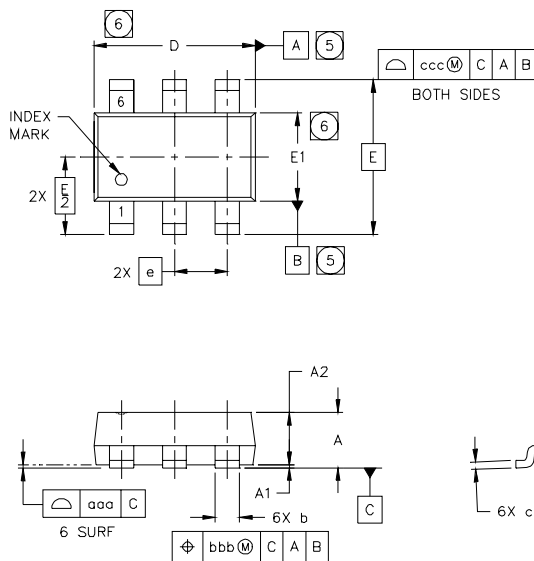
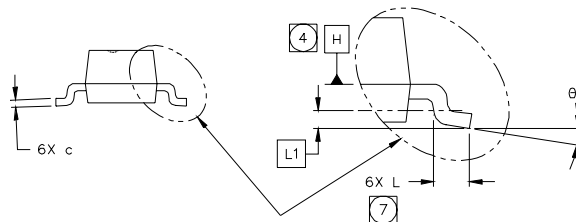


Fig 31. Typical Power Vs. Time

TSOP-6 Package Outline



SYMBOL	MO-193AA DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	.0433
A1	0.01	---	0.10	.0004	---	.0039
A2	0.80	0.90	1.00	.0315	.0354	.0393
b	0.25	---	0.50	.0099	---	.0196
c	0.10	---	0.26	.004	---	.010
D	2.90	3.00	3.10	.115	.118	.122
E	2.75 BSC			.108 BSC		
E1	1.30	1.50	1.70	.052	.059	.066
e	1.00 BSC			.039 BSC		
L	0.20	0.40	0.60	.0079	.0157	.0236
L1	0.30 BSC			.0118 BSC		
θ	0°	---	8°	0°	---	8°
aaa	0.10			.004		
bbb	0.15			.006		
ccc	0.25			.010		

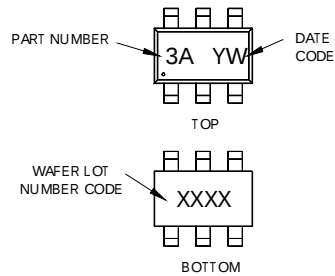


TSOP-6 Part Marking Information (Old)

Note: This part marking information applies to devices produced before 02/26/2001.

EXAMPLE: THIS IS AN SI3443DV

WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR



YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
1996	6		
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

PART NUMBER CODE REFERENCE:

3A = SI3443DV
3B = IRF5800
3C = IRF5850
3D = IRF5851
3E = IRF5852
3I = IRF5805
3J = IRF5806

DATE CODE EXAMPLES:

YWW = 9603 = 6C
YWW = 9632 = FF

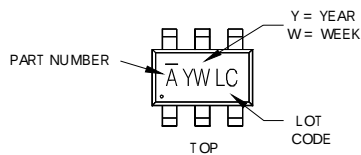
WW = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
1996	F		
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

TSOP-6 Part Marking Information (New)

Note: This part marking information applies to devices produced after 02/26/2001.

W = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR



YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
1996	6		
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

PART NUMBER CODE REFERENCE:

A = SI3443DV
B = IRF5800
C = IRF5850
D = IRF5851
E = IRF5852
I = IRF5805
J = IRF5806
K = IRF5810
L = IRF5804
M = IRF5803
N = IRF5820

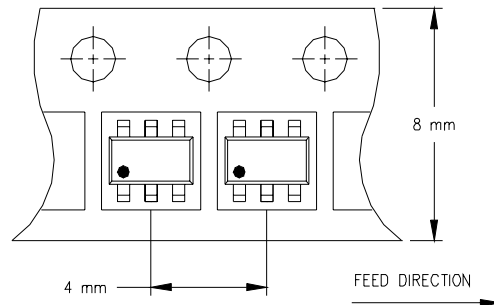
W = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
1996	F		
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

IRF5851

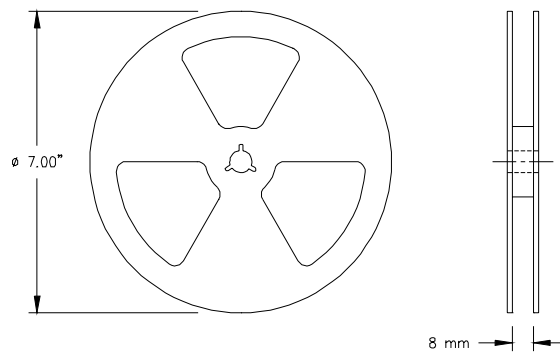
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TSOP-6 Tape & Reel Information



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information. 09/02