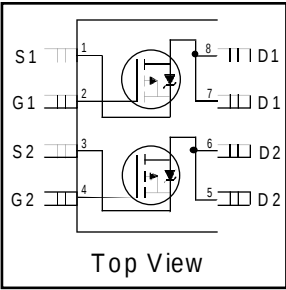


- Generation V Technology
- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Very Small SOIC Package
- Low Profile (<1.1mm)
- Available in Tape & Reel
- Fast Switching

Description

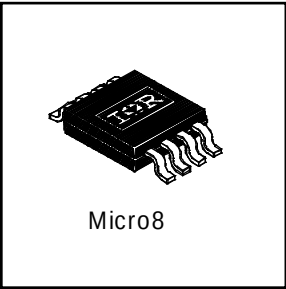
Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The new Micro8 package, with half the footprint area of the standard SO-8, provides the smallest footprint available in an SOIC outline. This makes the Micro8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



$V_{DSS} = -20V$

$R_{DS(on)} = 0.27\Omega$



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_A = 25^{\circ}C$	Continuous Drain Current, V_{GS} @ -4.5V	-1.7	A
I_D @ $T_A = 70^{\circ}C$	Continuous Drain Current, V_{GS} @ -4.5V	-1.4	
I_{DM}	Pulsed Drain Current ①	-9.6	
P_D @ $T_A = 25^{\circ}C$	Power Dissipation	1.25	W
	Linear Derating Factor	10	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt ②	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④	—	100	°C/W

All Micro8 Data Sheets reflect improved Thermal Resistance, Power and Current -Handling Ratings- effective only for product marked with Date Code 505 or later .

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.012	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.27	Ω	$V_{GS} = -4.5V, I_D = -1.2A$ ③
		—	—	0.40		$V_{GS} = -2.7V, I_D = -0.60A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-0.70	—	—	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	1.3	—	—	S	$V_{DS} = -10V, I_D = -0.60A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -16V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = +12V$
Q_g	Total Gate Charge	—	5.4	8.2	nC	$I_D = -1.2A$
Q_{gs}	Gate-to-Source Charge	—	0.96	1.4		$V_{DS} = -16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	2.4	3.6		$V_{GS} = -4.5V$, See Fig. 6 and 9 ③
$t_{d(on)}$	Turn-On Delay Time	—	9.1	—	ns	$V_{DD} = -10V$
t_r	Rise Time	—	35	—		$I_D = -1.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	38	—		$R_G = 6.0\Omega$
t_f	Fall Time	—	43	—		$R_D = 8.3\Omega$, See Fig. 10 ③
C_{iss}	Input Capacitance	—	240	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	130	—		$V_{DS} = -15V$
C_{rss}	Reverse Transfer Capacitance	—	64	—		$f = 1.0MHz$, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.25	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-9.6		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -1.2A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	52	78	ns	$T_J = 25^\circ\text{C}, I_F = -1.2A$
Q_{rr}	Reverse Recovery Charge	—	63	95	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

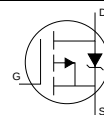
Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

② $I_{SD} \leq -1.2A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

④ Surface mounted on FR-4 board, $t \leq 10sec$.



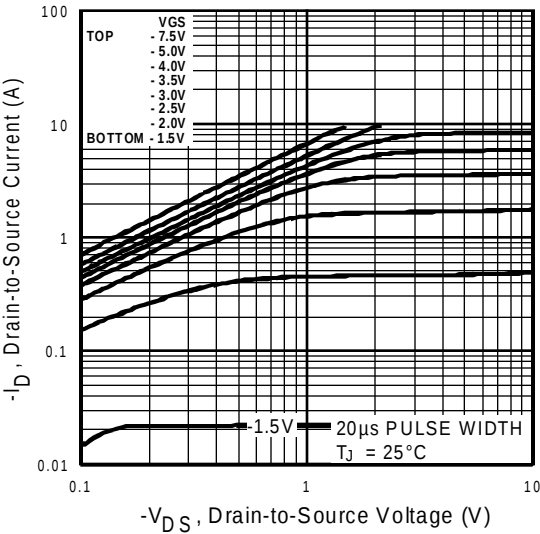


Fig 1. Typical Output Characteristics

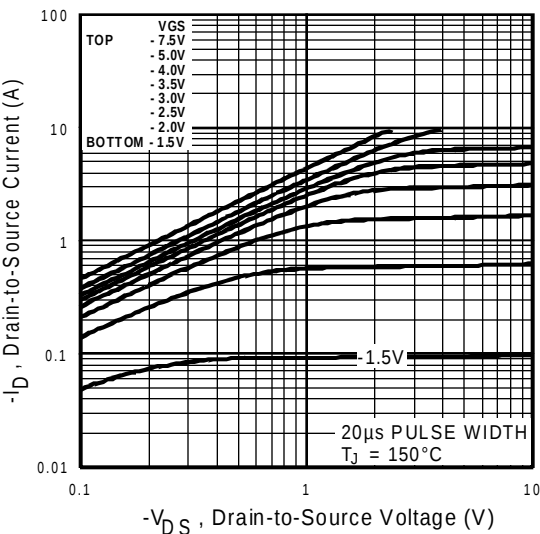


Fig 2. Typical Output Characteristics

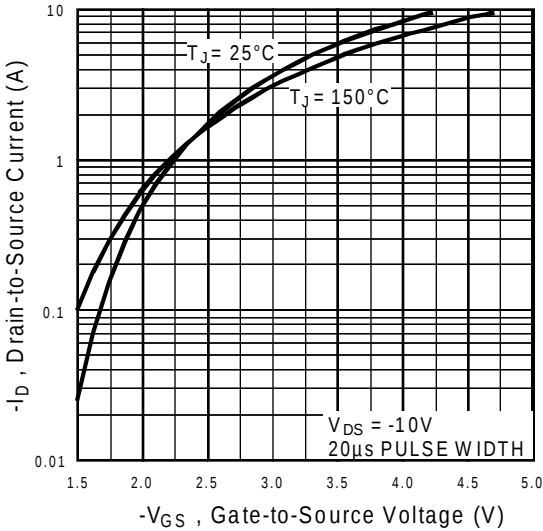


Fig 3. Typical Transfer Characteristics

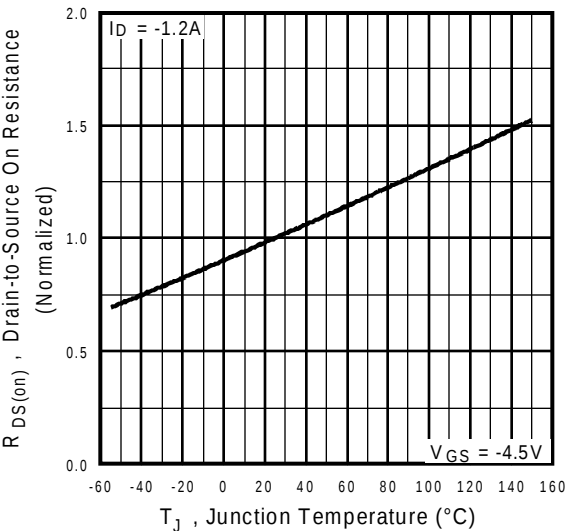


Fig 4. Normalized On-Resistance Vs. Temperature

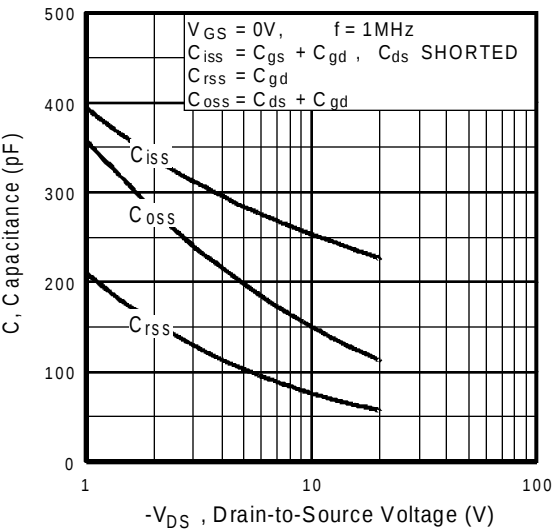


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

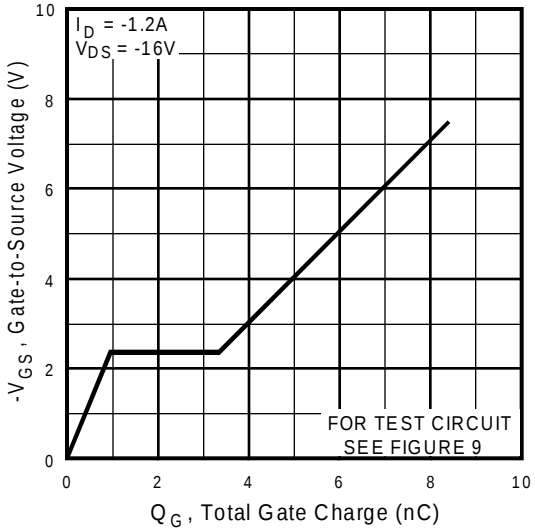


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

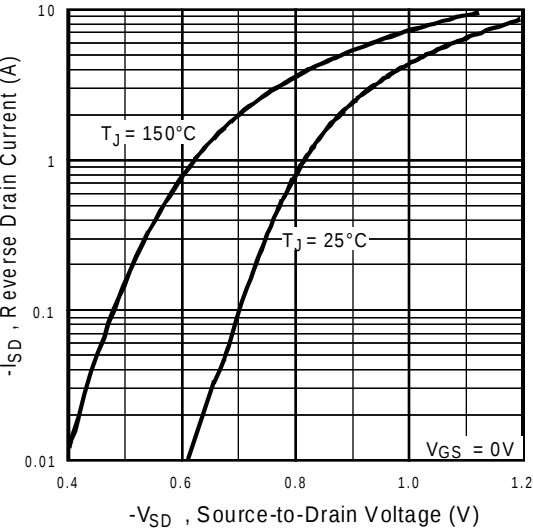


Fig 7. Typical Source-Drain Diode Forward Voltage

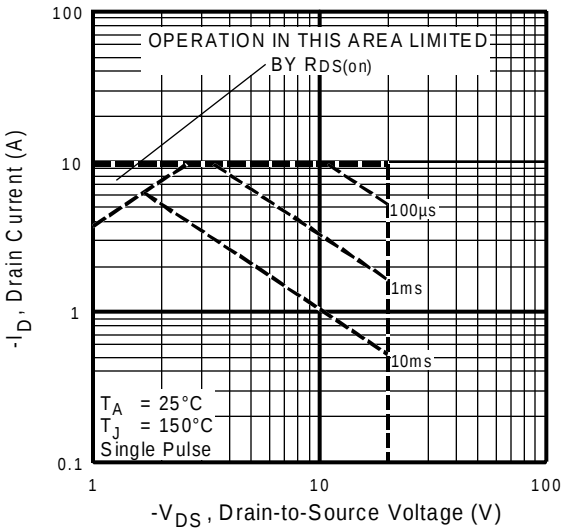


Fig 8. Maximum Safe Operating Area

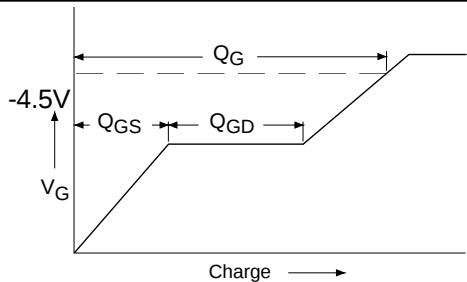


Fig 9a. Basic Gate Charge Waveform

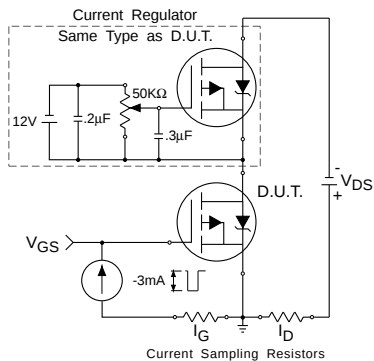


Fig 9b. Gate Charge Test Circuit

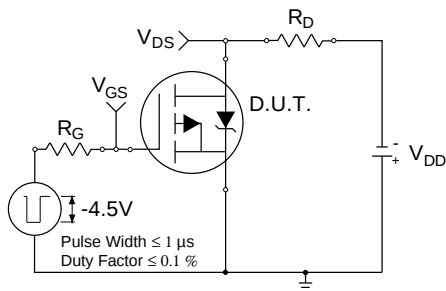


Fig 10a. Switching Time Test Circuit

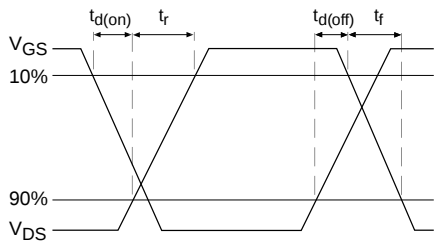


Fig 10b. Switching Time Waveforms

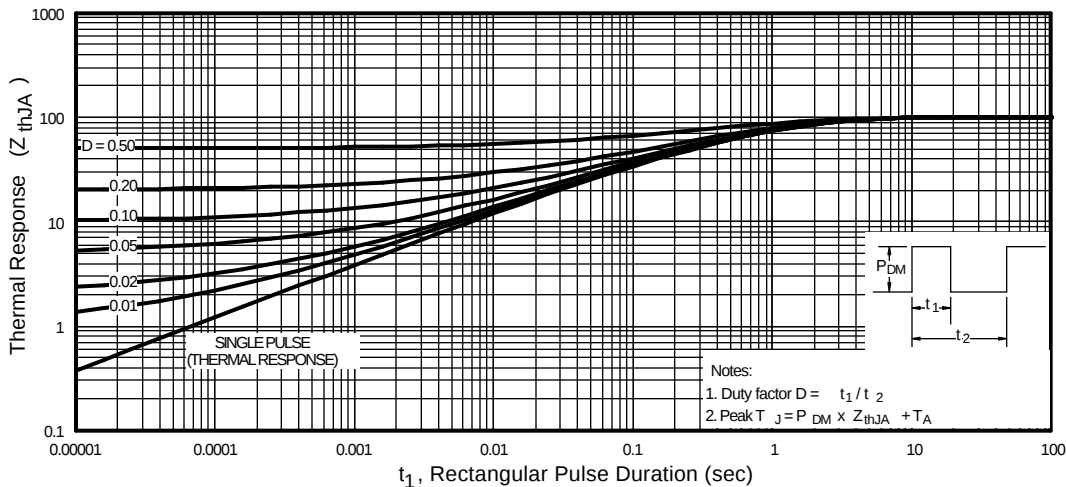


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

The diagram illustrates a common-emitter amplifier circuit. The input signal, V_{GS}^* , is applied to the base of the BJT through a resistor R_G . The base is also connected to a voltage divider network consisting of a resistor and a capacitor. The emitter is connected to ground through a resistor. The collector is connected to a load consisting of a resistor and a capacitor. The output voltage is taken across the collector load. The circuit is powered by a DC supply V_{DD} . The BJT is represented by a circle with a triangle inside, and the load is represented by a circle with a triangle inside. The input signal is represented by a square wave. The output voltage is represented by a sine wave. The circuit is labeled with various components and their connections.

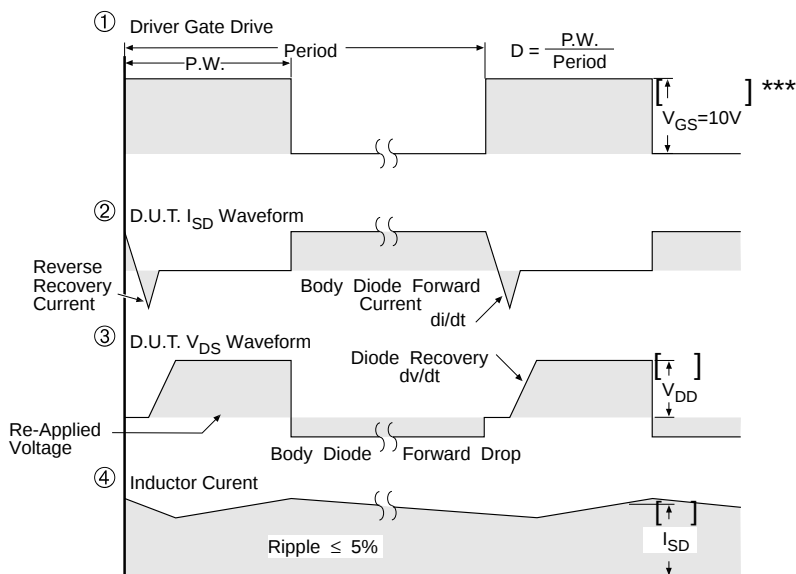
Circuit Layout Considerations

- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance

Current Transformer

- dv/dt controlled by R_G
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

**** Use P-Channel Driver for P-Channel Measurements**



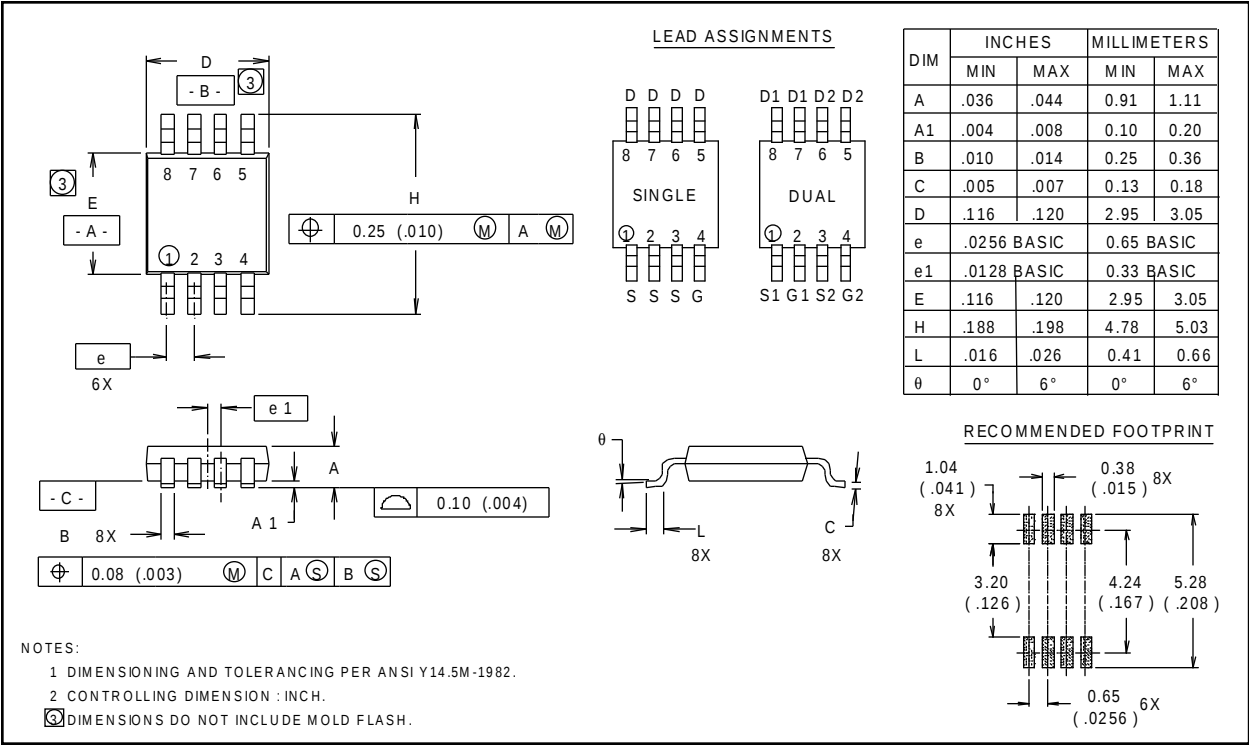
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 12. For P-Channel HEXFETS

Package Outline

Micro8 Outline

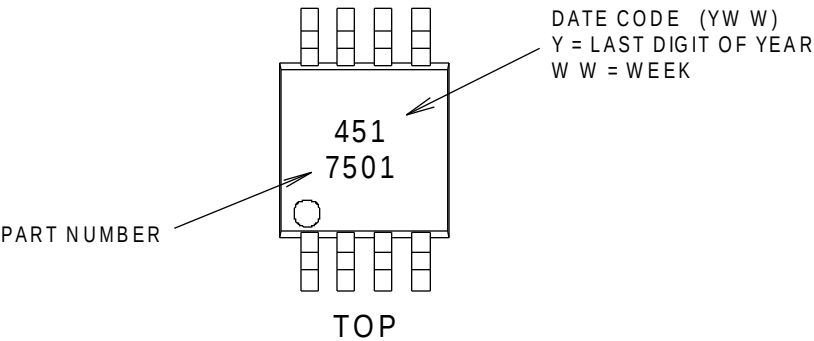
Dimensions are shown in millimeters (inches)



Part Marking Information

Micro8

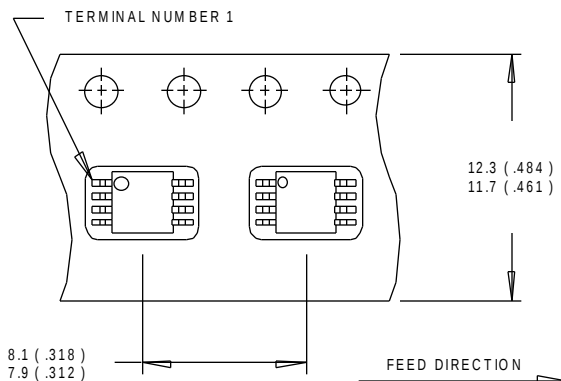
EXAMPLE : THIS IS AN IRF7501



Tape & Reel Information

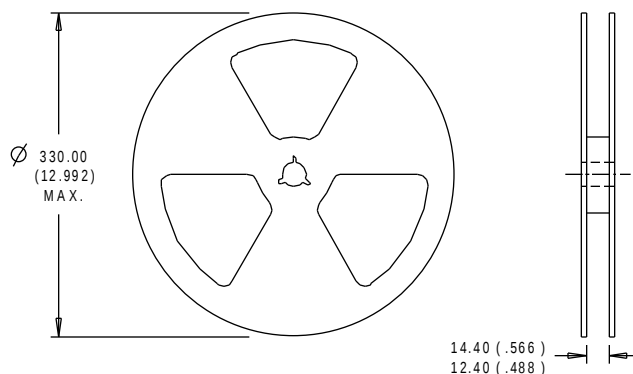
Micro8

Dimensions are shown in millimeters (inches)



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

International
IR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331

EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

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