

IRF9540NS/L

HEXFET® Power MOSFET

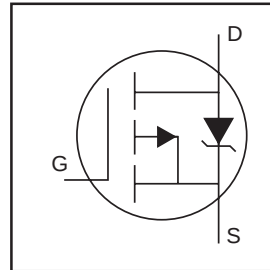
- Advanced Process Technology
- Surface Mount (IRF9540NS)
- Low-profile through-hole (IRF9540NL)
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

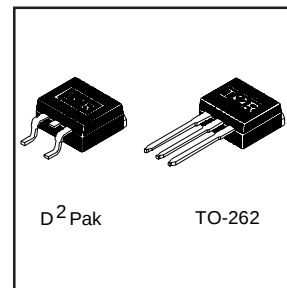
The through-hole version (IRF9540L) is available for low-profile applications.



$$V_{DS} = -100V$$

$$R_{DS(on)} = 0.117\Omega$$

$$I_D = -23A$$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$ ⑤	-23	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$ ⑤	-16	
I_{DM}	Pulsed Drain Current ① ⑤	-76	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	140	W
	Linear Derating Factor	0.91	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy② ⑤	430	mJ
I_{AR}	Avalanche Current①	-11	A
E_{AR}	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ⑤	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

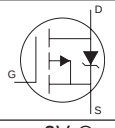
IRF9540NS/L

International
IR Rectifier

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V$, $I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.117	Ω	$V_{GS} = -10V$, $I_D = -11A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
g_{fs}	Forward Transconductance	5.3	—	—	S	$V_{DS} = -50V$, $I_D = -11A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{DS} = -100V$, $V_{GS} = 0V$
		—	—	-250		$V_{DS} = -80V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	97	nC	$I_D = -11A$
Q_{gs}	Gate-to-Source Charge	—	—	15		$V_{DS} = -80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	51		$V_{GS} = -10V$, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = -50V$
t_r	Rise Time	—	67	—		$I_D = -11A$
$t_{d(off)}$	Turn-Off Delay Time	—	51	—		$R_G = 5.1\Omega$
t_f	Fall Time	—	51	—		$R_D = 4.2\Omega$, See Fig. 10 ④
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	400	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	240	—		$f = 1.0MHz$, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-23	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-76		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	$T_J = 25^\circ\text{C}$, $I_S = -11A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	150	220	ns	$T_J = 25^\circ\text{C}$, $I_F = -11A$
Q_{rr}	Reverse Recovery Charge	—	830	1200	nC	$di/dt = -100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25^\circ\text{C}$, $L = 7.1mH$
 $R_G = 25\Omega$, $I_{AS} = -11A$. (See Figure 12)

③ $I_{SD} \leq -11A$, $di/dt \leq -470A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ Uses IRF9540N data and test conditions

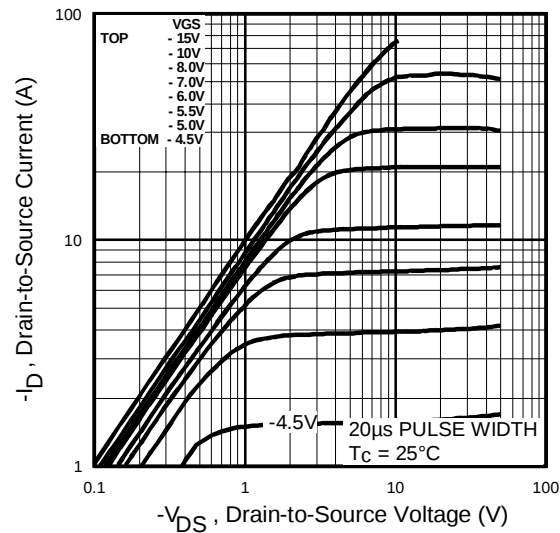


Fig 1. Typical Output Characteristics

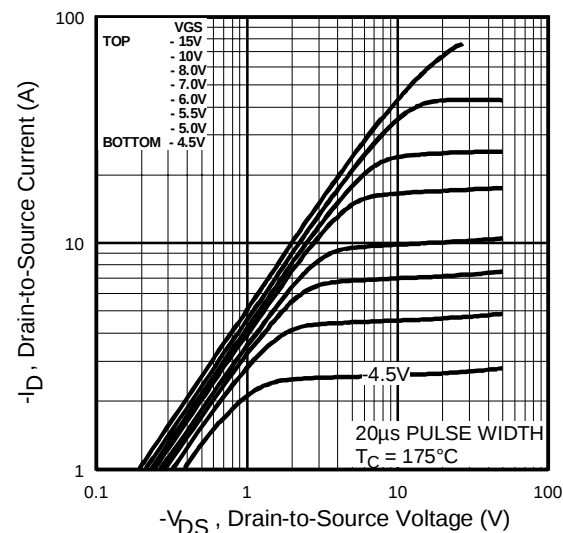


Fig 2. Typical Output Characteristics

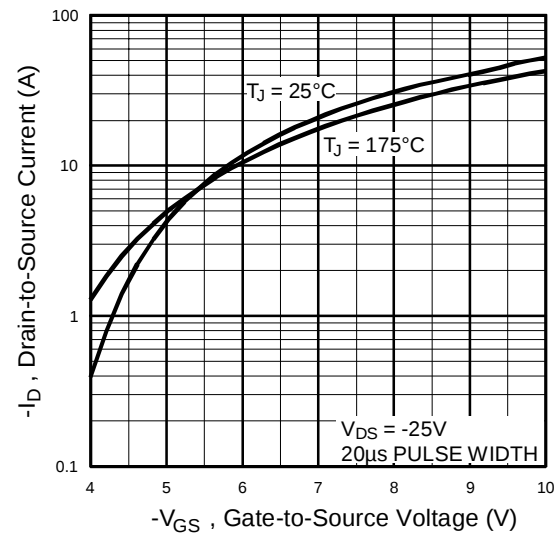


Fig 3. Typical Transfer Characteristics

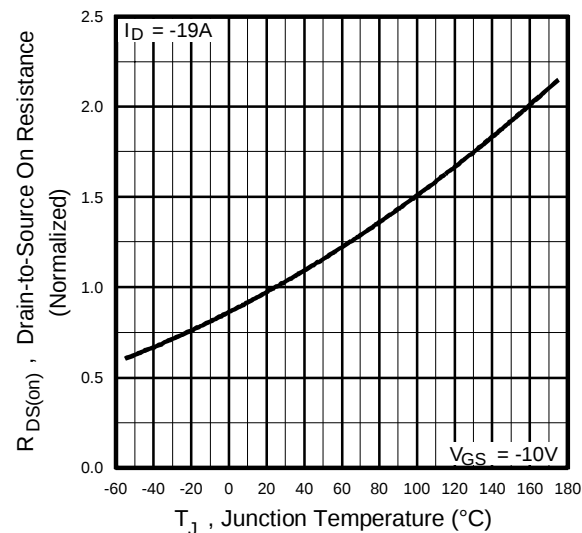


Fig 4. Normalized On-Resistance
Vs. Temperature

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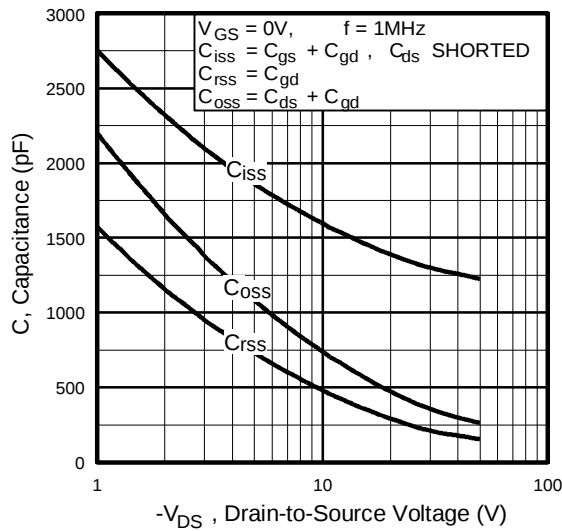


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

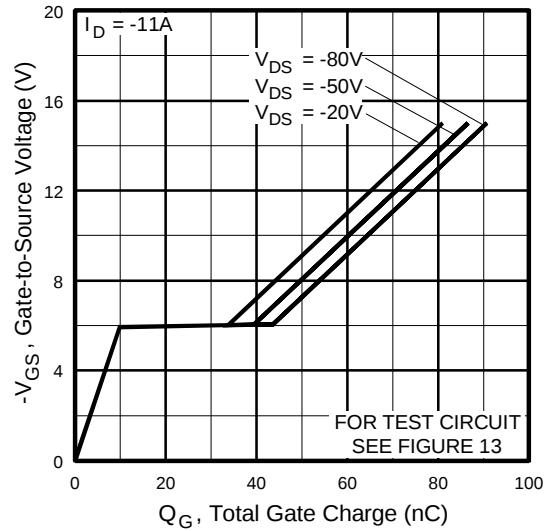


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

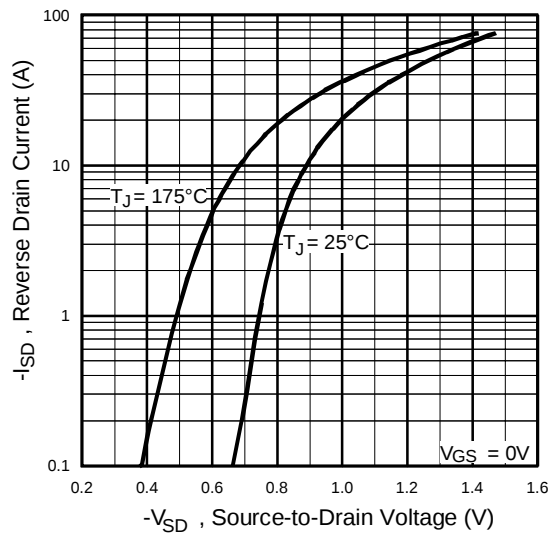


Fig 7. Typical Source-Drain Diode Forward Voltage

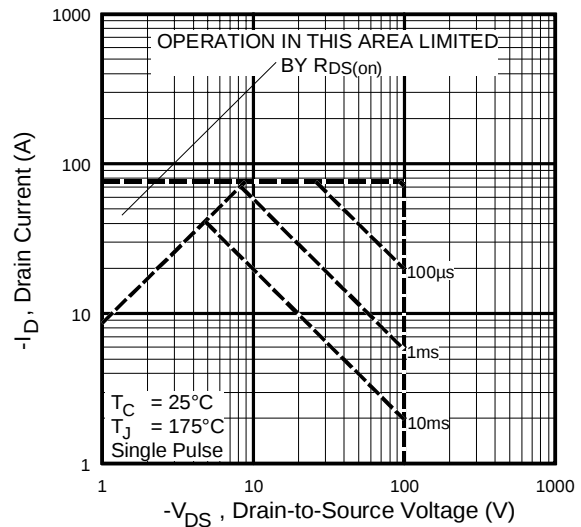


Fig 8. Maximum Safe Operating Area

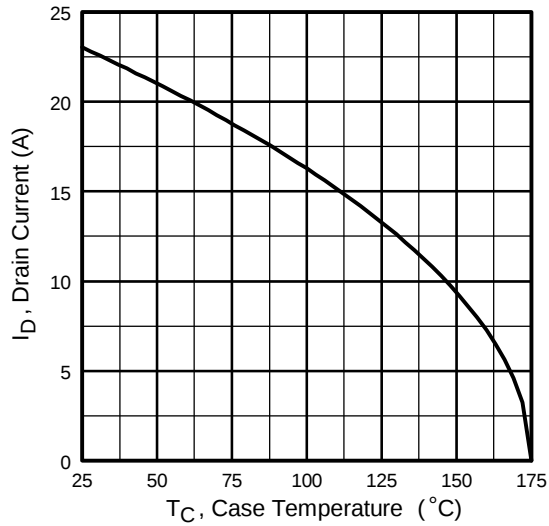


Fig 9. Maximum Drain Current Vs. Case Temperature

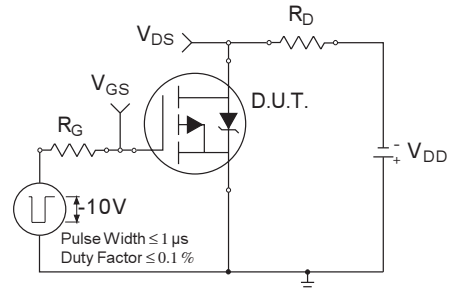


Fig 10a. Switching Time Test Circuit

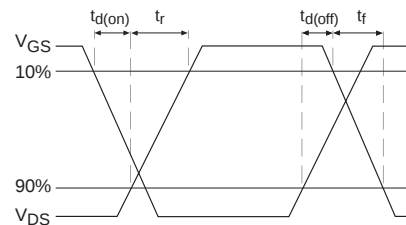


Fig 10b. Switching Time Waveforms

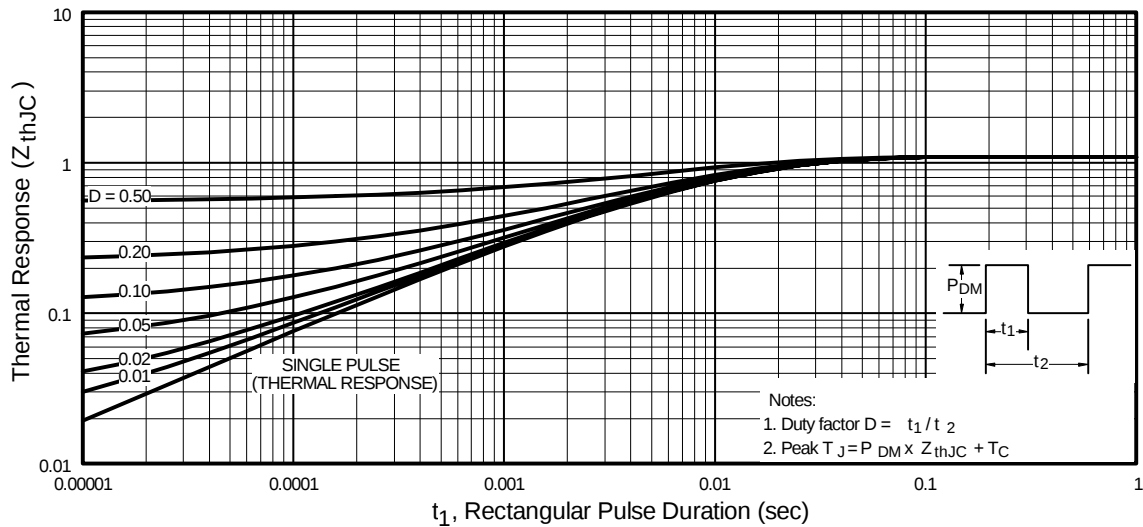


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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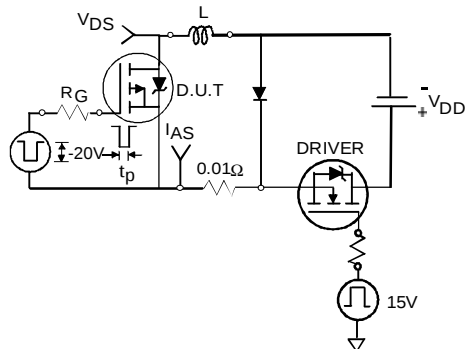


Fig 12a. Unclamped Inductive Test Circuit

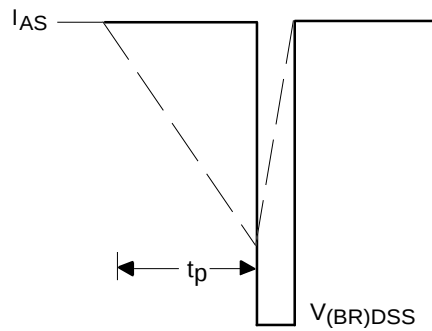


Fig 12b. Unclamped Inductive Waveforms

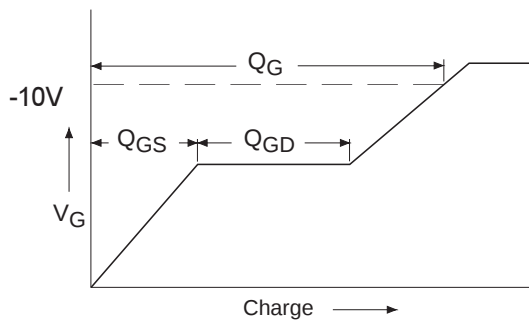


Fig 13a. Basic Gate Charge Waveform

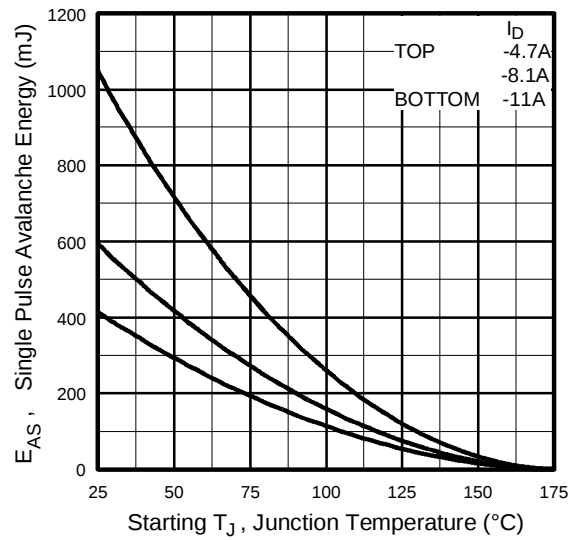


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

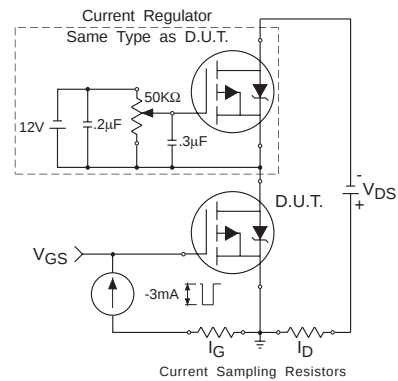
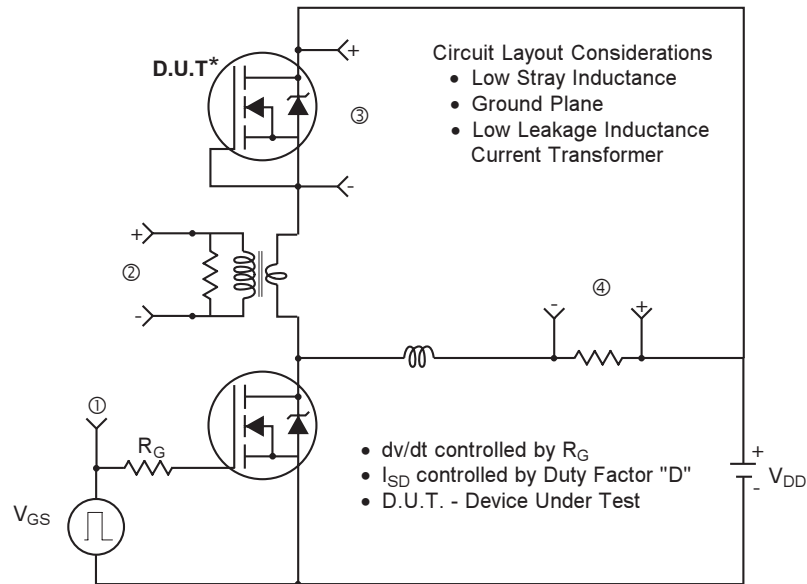
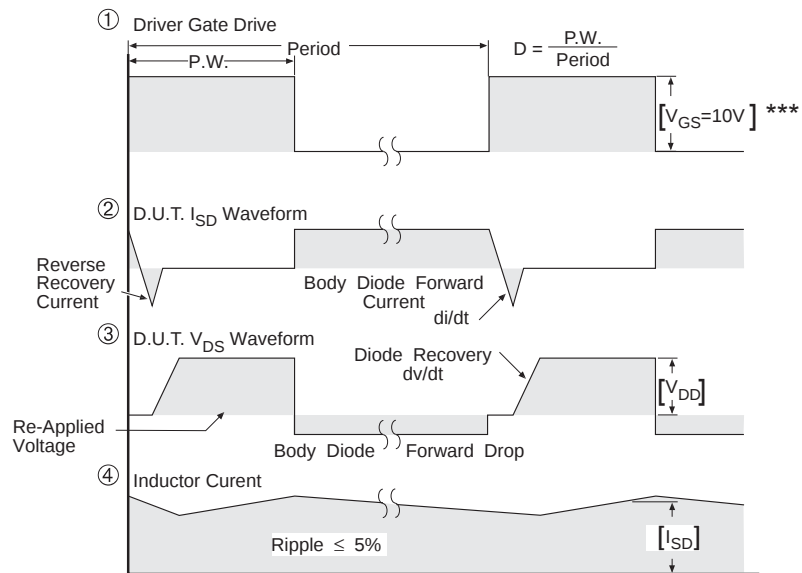


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T. for P-Channel

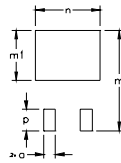
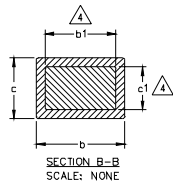
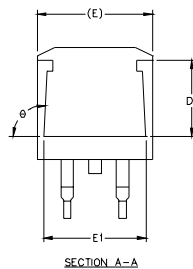


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

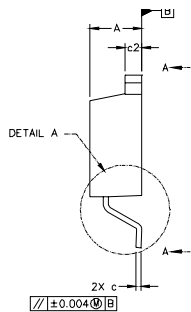
Fig 14. For P-Channel HEXFETS

D²Pak Package Outline

Diagram showing the elevation view of a bridge pier and abutment. The structure includes a pier with a curved profile and an abutment on the right. A detail 'A' is indicated by a triangle and labeled 'DETAIL "A" ROTATED 90° SCALE 8:1'. The diagram also shows the 'GAUGE PLANE' and 'SEATING PLANE' with dimensions: 0'-8" for the distance from the gauge plane to the pier, L1 for the pier length, and A1 for the distance from the pier to the seating plane. A small triangle labeled 'L4' is shown near the gauge plane.



Technical drawing of a 3D-printed part. The drawing shows a top view and a side view. Dimensions are indicated by arrows and labels: L2, D, L3, E, L, and A. The part has a central circular feature (1) and two side features (2 and 3). Tolerances are specified for various features: ± 0.05 for feature 1, ± 0.05 for feature 2, ± 0.05 for feature 3, ± 0.05 for feature 4, ± 0.05 for feature 5, ± 0.05 for feature 6, ± 0.05 for feature 7, ± 0.05 for feature 8, ± 0.05 for feature 9, ± 0.05 for feature 10, ± 0.05 for feature 11, ± 0.05 for feature 12, ± 0.05 for feature 13, ± 0.05 for feature 14, ± 0.05 for feature 15, ± 0.05 for feature 16, ± 0.05 for feature 17, ± 0.05 for feature 18, ± 0.05 for feature 19, ± 0.05 for feature 20, ± 0.05 for feature 21, ± 0.05 for feature 22, ± 0.05 for feature 23, ± 0.05 for feature 24, ± 0.05 for feature 25, ± 0.05 for feature 26, ± 0.05 for feature 27, ± 0.05 for feature 28, ± 0.05 for feature 29, ± 0.05 for feature 30, ± 0.05 for feature 31, ± 0.05 for feature 32, ± 0.05 for feature 33, ± 0.05 for feature 34, ± 0.05 for feature 35, ± 0.05 for feature 36, ± 0.05 for feature 37, ± 0.05 for feature 38, ± 0.05 for feature 39, ± 0.05 for feature 40, ± 0.05 for feature 41, ± 0.05 for feature 42, ± 0.05 for feature 43, ± 0.05 for feature 44, ± 0.05 for feature 45, ± 0.05 for feature 46, ± 0.05 for feature 47, ± 0.05 for feature 48, ± 0.05 for feature 49, ± 0.05 for feature 50, ± 0.05 for feature 51, ± 0.05 for feature 52, ± 0.05 for feature 53, ± 0.05 for feature 54, ± 0.05 for feature 55, ± 0.05 for feature 56, ± 0.05 for feature 57, ± 0.05 for feature 58, ± 0.05 for feature 59, ± 0.05 for feature 60, ± 0.05 for feature 61, ± 0.05 for feature 62, ± 0.05 for feature 63, ± 0.05 for feature 64, ± 0.05 for feature 65, ± 0.05 for feature 66, ± 0.05 for feature 67, ± 0.05 for feature 68, ± 0.05 for feature 69, ± 0.05 for feature 70, ± 0.05 for feature 71, ± 0.05 for feature 72, ± 0.05 for feature 73, ± 0.05 for feature 74, ± 0.05 for feature 75, ± 0.05 for feature 76, ± 0.05 for feature 77, ± 0.05 for feature 78, ± 0.05 for feature 79, ± 0.05 for feature 80, ± 0.05 for feature 81, ± 0.05 for feature 82, ± 0.05 for feature 83, ± 0.05 for feature 84, ± 0.05 for feature 85, ± 0.05 for feature 86, ± 0.05 for feature 87, ± 0.05 for feature 88, ± 0.05 for feature 89, ± 0.05 for feature 90, ± 0.05 for feature 91, ± 0.05 for feature 92, ± 0.05 for feature 93, ± 0.05 for feature 94, ± 0.05 for feature 95, ± 0.05 for feature 96, ± 0.05 for feature 97, ± 0.05 for feature 98, ± 0.05 for feature 99, ± 0.05 for feature 100.

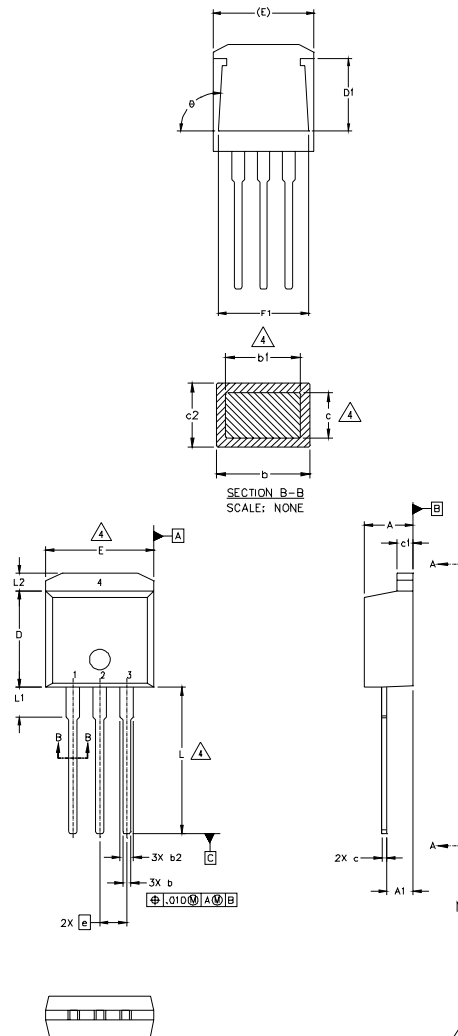


5. CONTROLLING DIMENSION: INCH.

- PART DEPENDENT.

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

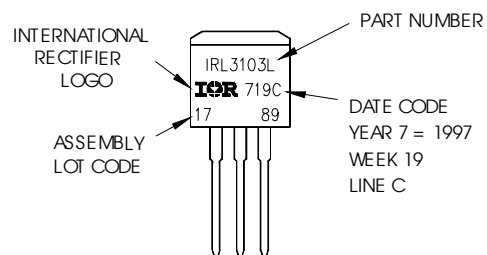
- 1. - GATE
- 2. - DRAIN
- 3. - SOURCE
- 4. - DRAIN

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [".005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

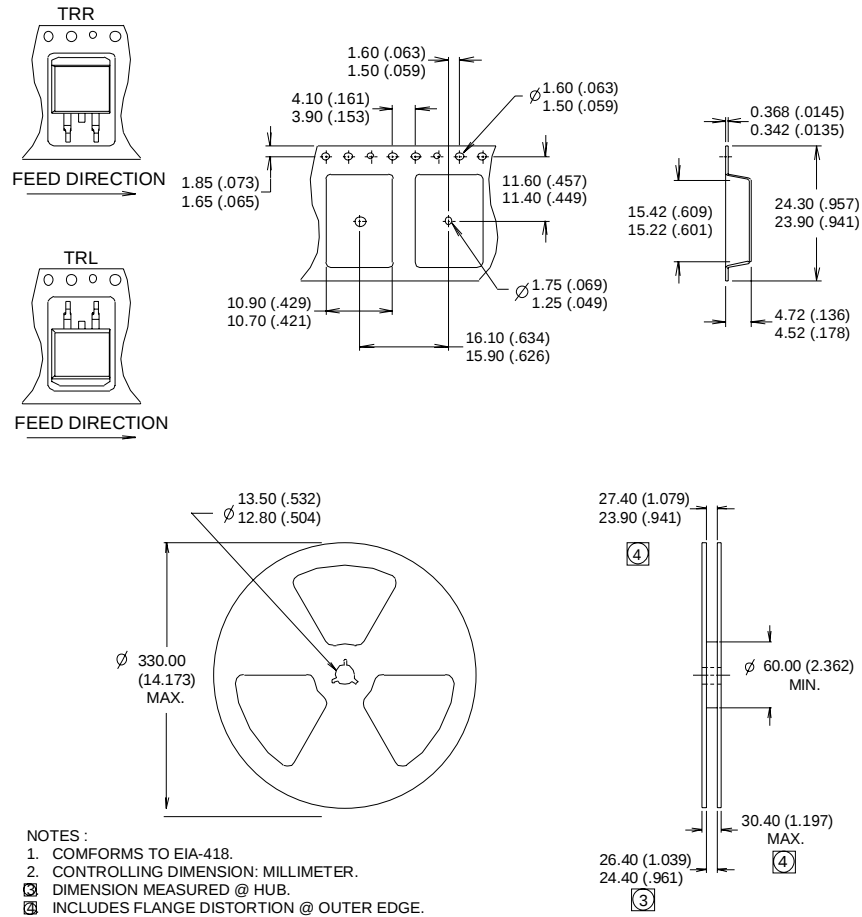
EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



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D²Pak Tape & Reel Information



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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

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