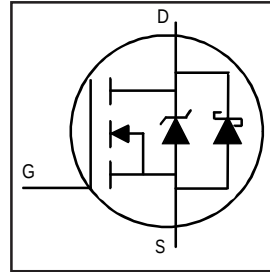


IRL3103D1S

FETKY™ MOSFET & SCHOTTKY RECTIFIER

- Co-packaged HEXFET® Power MOSFET and Schottky Diode
- Generation 5 Technology
- Logic Level Gate Drive
- Minimize Circuit Inductance
- Ideal For Synchronous Regulator Application

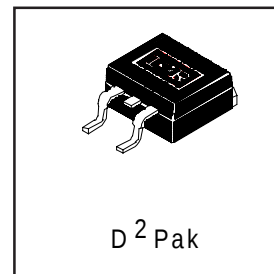


$V_{DSS} = 30V$
$R_{DS(on)} = 0.014\Omega$
$I_D = 64A$

Description

The FETKY family of co-packaged HEXFET power MOSFETs and Schottky Diodes offer the designer an innovative board space saving solution for switching regulator applications. A low on resistance Gen5 MOSFET with a low forward voltage drop Schottky diode and minimized component interconnect inductance and resistance result in maximized converter efficiencies.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	64	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	45	
I_{DM}	Pulsed Drain Current ① ③	220	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.1	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	89	W
	Linear Derating Factor	0.56	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

IRL3103D1S

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MOSFET Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.037	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$ ③
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.014	Ω	$V_{GS} = 10V, I_D = 34A$ ②
		—	—	0.019		$V_{GS} = 4.5V, I_D = 28A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	23	—	—	S	$V_{DS} = 25V, I_D = 34A$ ③
I_{DSS}	Drain-to-Source Leakage Current	—	—	0.10	mA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	22		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	43	nC	$I_D = 32A$
Q_{gs}	Gate-to-Source Charge	—	—	14		$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	23		$V_{GS} = 4.5V$, See Fig. 6 ②
$t_{d(on)}$	Turn-On Delay Time	—	9.0	—	ns	$V_{DD} = 15V$
t_r	Rise Time	—	210	—		$I_D = 32A$
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		$R_G = 3.4\Omega, V_{GS} = 4.5V$
t_f	Fall Time	—	54	—		$R_D = 0.43\Omega$, ②③
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	1900	—		$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	810	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	240	—		$f = 1.0MHz$, See Fig. 5
C_{iss}	Input Capacitance	—	3500	—		$V_{GS} = 0V, V_{DS} = 0V$

Body Diode & Schottky Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_F (AV)$	(Schottky)	—	—	2.0	A	MOSFET symbol showing the integral reverse p-n junction and Schottky diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	220		
V_{SD1}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 32A, V_{GS} = 0V$ ②
V_{SD2}	Diode Forward Voltage	—	—	0.50	V	$T_J = 25^\circ\text{C}, I_S = 1.0A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	51	77	ns	$T_J = 25^\circ\text{C}, I_F = 32A$
Q_{rr}	Reverse Recovery Charge	—	49	73	nC	$di/dt = 100A/\mu s$ ②
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 10)
- ② Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ③ Uses IRL3103D1 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

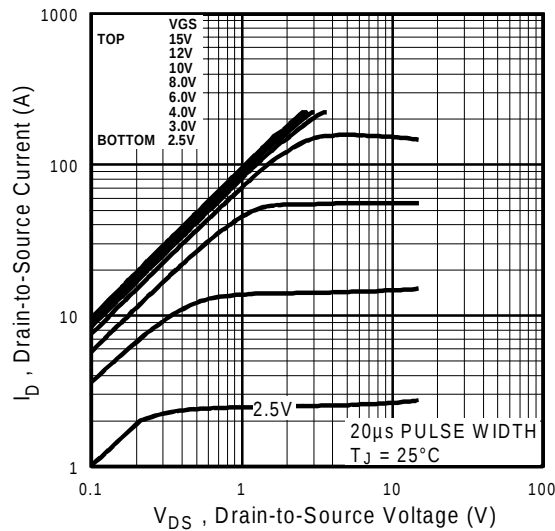


Fig 1. Typical Output Characteristics

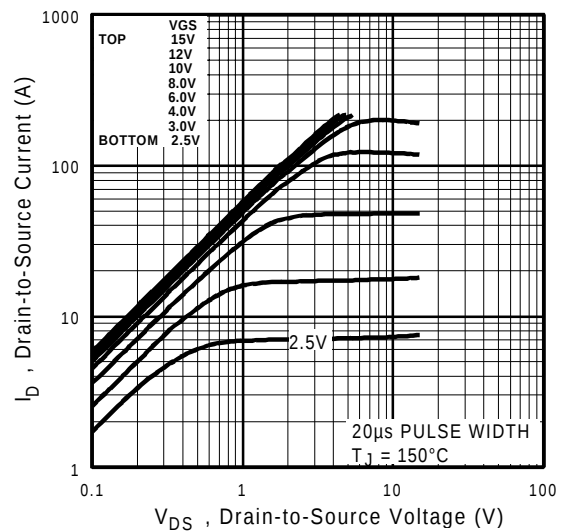


Fig 2. Typical Output Characteristics

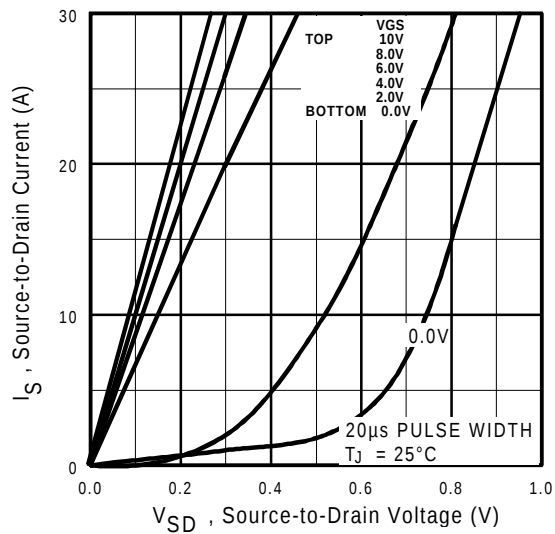


Fig 3. Typical Reverse Output Characteristics

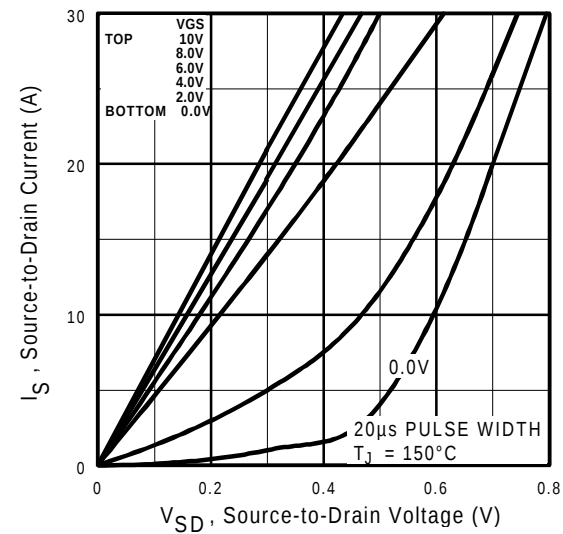


Fig 4. Typical Reverse Output Characteristics

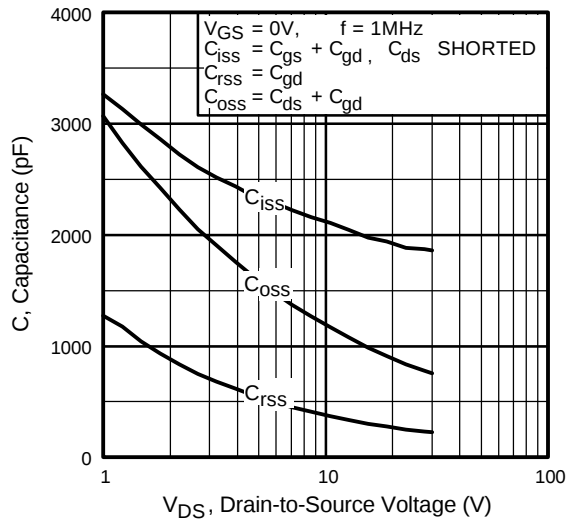


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

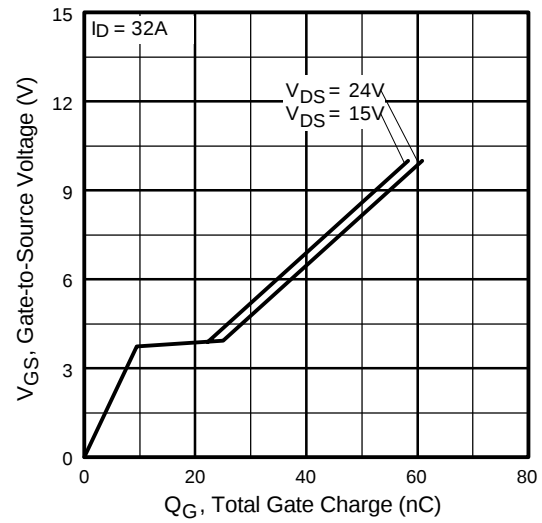


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

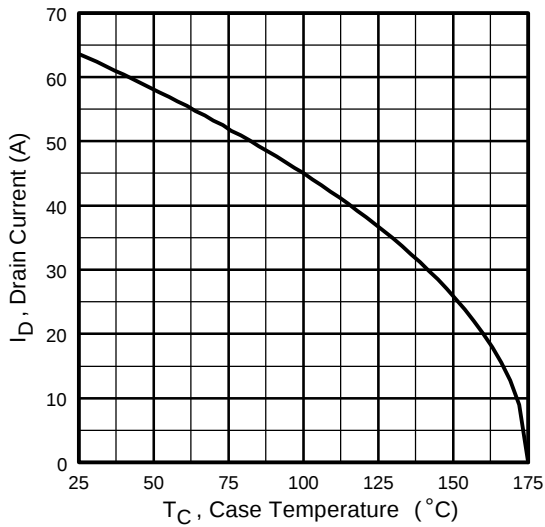


Fig 7. Maximum Drain Current Vs. Case Temperature

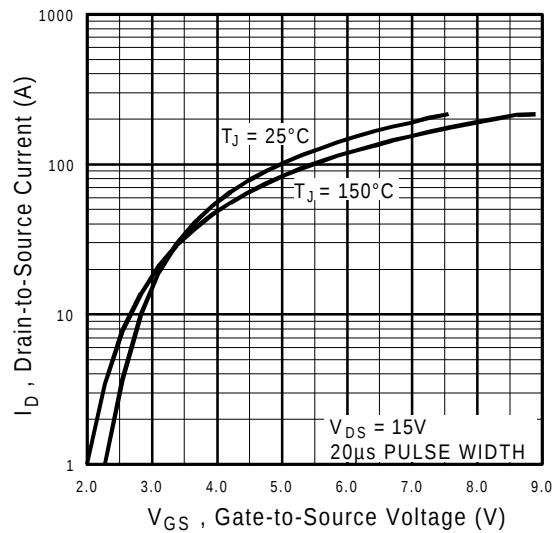


Fig 8. Typical Transfer Characteristics

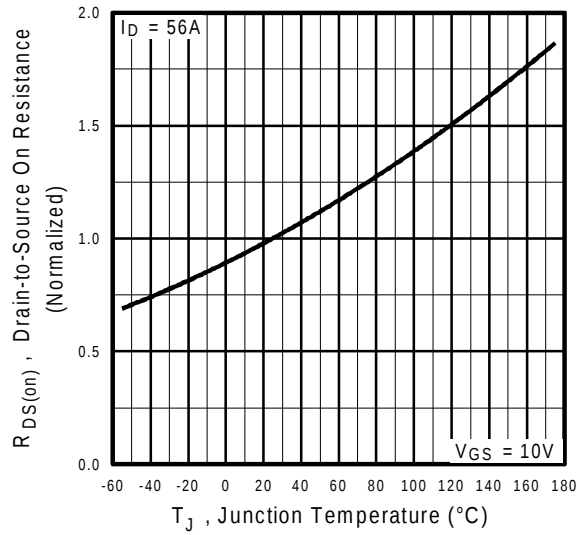


Fig 9. Normalized On-Resistance
Vs. Temperature

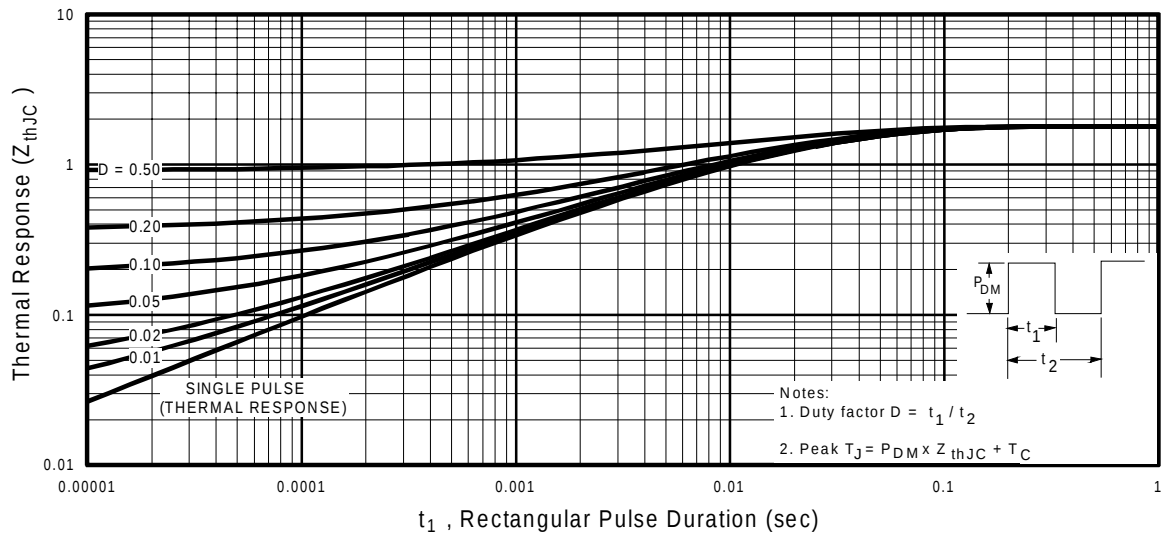


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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The technical drawing illustrates the dimensions for a 3-lead gate array package. It includes three views: a top view, a side view, and a minimum recommended footprint.

Top View Dimensions:

- Overall width: 10.54 (.415) and 10.29 (.405)
- Lead pitch: 1.40 (.055) MAX.
- Lead width: 1.78 (.070) and 1.27 (.050)
- Lead spacing: 15.49 (.610) and 14.73 (.580)
- Lead width (3X): 1.40 (.055) and 1.14 (.045)
- Lead spacing (3X): 0.93 (.037) and 0.69 (.027)
- Overall length: 5.08 (.200)
- Package marking: $\oplus$ 0.25 (.010) (M) B (A) M

Side View Dimensions:

- Lead height: 4.69 (.185) and 4.20 (.165)
- Lead width: 1.32 (.052) and 1.22 (.048)
- Lead spacing: 2.79 (.110) and 2.29 (.090)
- Lead width (3X): 5.28 (.208) and 4.78 (.188)
- Lead spacing (3X): 0.55 (.022) and 0.46 (.018)
- Lead width (3X): 1.39 (.055) and 1.14 (.045)

Minimum Recommended Footprint Dimensions:

- Overall width: 10.16 (.400) REF.
- Lead width: 6.47 (.255) and 6.18 (.243)
- Lead spacing: 2.61 (.103) and 2.32 (.091)
- Overall length: 8.89 (.350) REF.

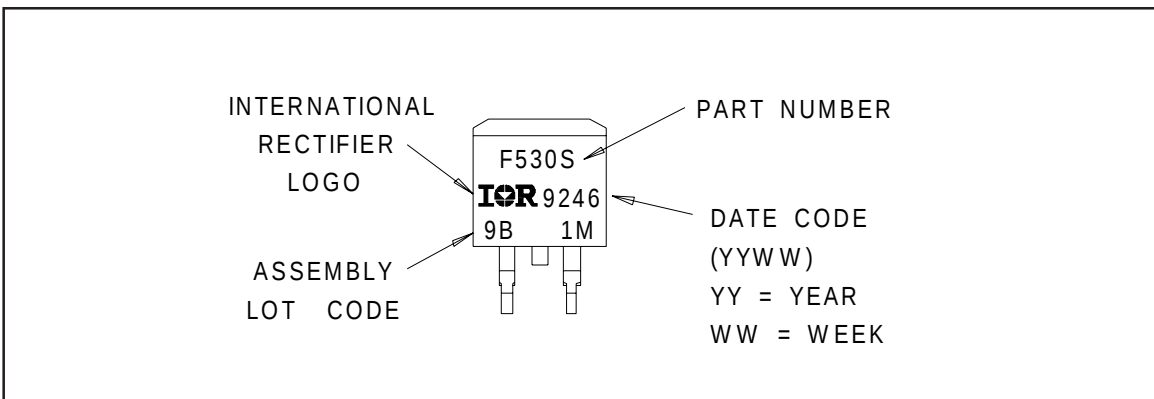
Lead Assignments:

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

Notes:

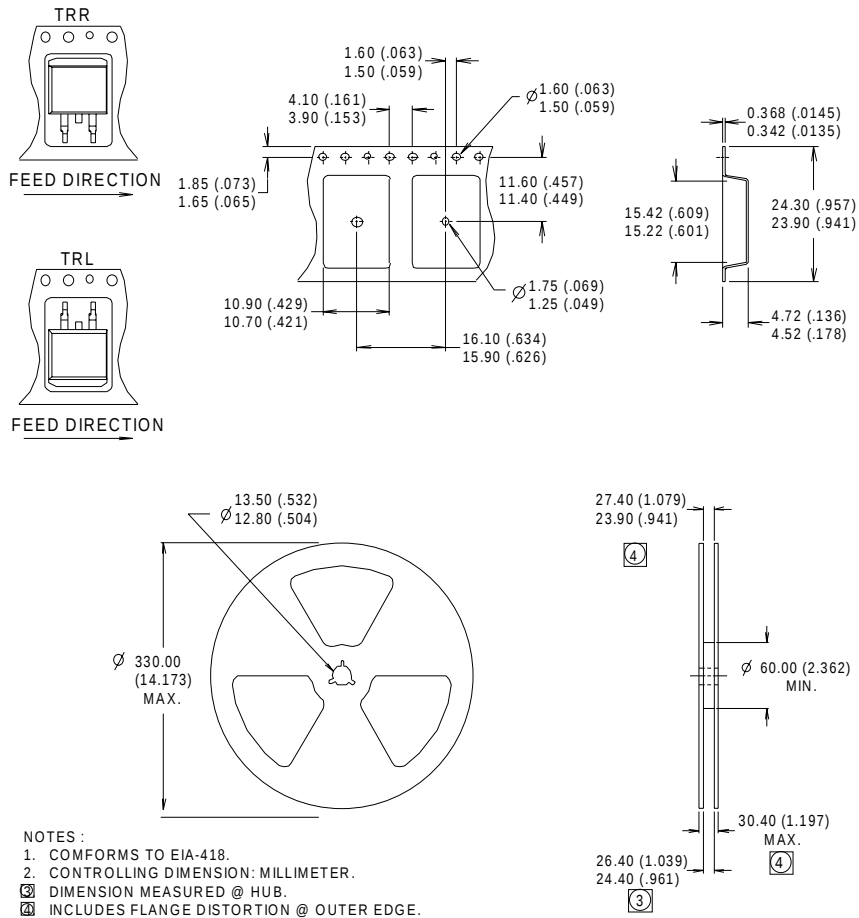
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

D²Pak



Tape & Reel Information

D²Pak



NOTES :

1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

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IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

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