Features

- **2.7V to 3.6V Read/Write Operation**
- **Fast Read Access Time - 120 ns**
- **Internal Erase/Program Control**
- **Sector Architecture**
  - **One 8K Words (16K bytes) Boot Block with Programming Lockout**
  - **Two 4K Words (8K bytes) Parameter Blocks**
  - **One 496K Words (992K bytes) Main Memory Array Block**
- **Fast Sector Erase Time - 10 seconds**
- **Byte-by-Byte or Word-By-Word Programming - 30 µs Typical**
- **Hardware Data Protection**
- **$\overline{\text{DATA}}$ Polling For End Of Program Detection**
- **Low-Power Dissipation**
  - **25 mA Active Current**
  - **50 µA CMOS Standby Current**
- **Typical 10,000 Write Cycles**

Description

The AT49BV008A(T) and AT49BV8192A(T) are 3-volt, 8-megabit Flash Memories organized as 1,048,576 words of 8 bits each or 512K words of 16 bits each. Manufactured with Atmel's advanced nonvolatile CMOS technology, the devices offer access times to 120 ns with power dissipation of just 67 mW at 2.7V read. When deselected, the CMOS standby current is less than 50 µA.

The device contains a user-enabled "boot block" protection feature. Two versions of the feature are available: the AT49BV008A/8192A locates the boot block at lowest order addresses ("bottom boot"); the AT49BV008AT/8192AT locates it at highest order addresses ("top boot").

To allow for simple in-system reprogrammability, the AT49BV008A(T)/8192A(T) does not require high input voltages for programming. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{WE}}$ inputs to avoid bus contention. Reprogramming the AT49BV008A(T)/8192A(T) is performed by first erasing a block of data and then programming on a byte-by-byte or word-by-word basis.

(continued)

Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RESET}}$	Reset
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{Busy}}$ Output
VPP	Optional Power Supply for Faster Program/Erase Operations
I/O0 - I/O14	Data Inputs/Outputs
I/O15 (A-1)	I/O15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
$\overline{\text{BYTE}}$	Selects Byte or Word Mode
NC	No Connect

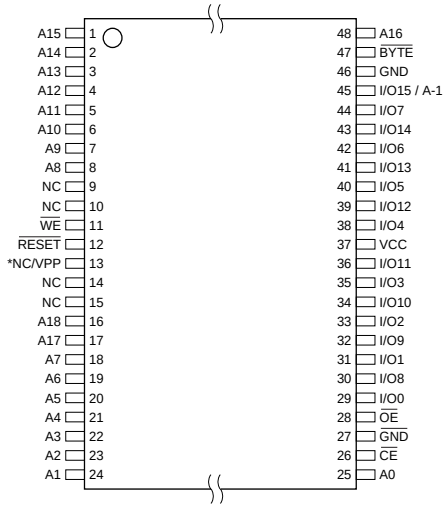
8-Megabit (1M x 8/ 512K x 16) CMOS Flash Memory

AT49BV008A
AT49BV008AT
AT49BV8192A
AT49BV8192AT
Preliminary

Rev. 1049C–09/98

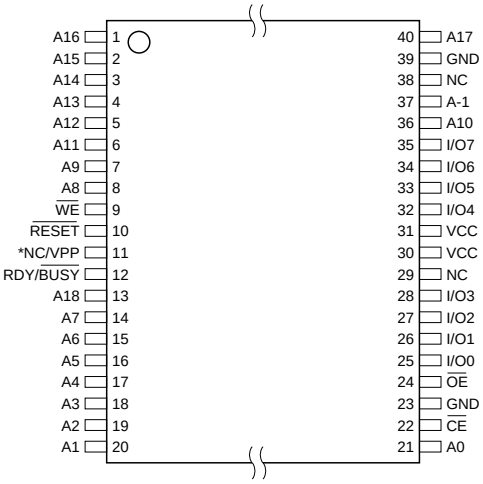
AT49BV8192A(T) TSOP Top View

Type 1



AT49BV008A(T) TSOP Top View

Type 1



AT49BV8192A(T)
CBGA Top View (Ball Down)

	1	2	3	4	5	6	7	8
A	A13	A11	A8	*NC/VPP	NC	NC	A7	A4
B	A14	A10	WE	RST	A18	A17	A5	A2
C	A15	A12	A9	NC	NC	A6	A3	A1
D	A16	I/O14	I/O5	I/O11	I/O2	I/O8	CE	A0
E	BYTE	I/O15	I/O6	I/O12	I/O3	I/O9	I/O0	GND
F	GND	I/O7	I/O13	I/O4	VCC	I/O10	I/O1	OE

AT49BV008A(T) Standard Pin Definition
CBGA Top View (Ball Down)

	1	2	3	4	5	6	7	8
A	A13	A11	A8	VPP	NC	NC	A7	A4
B	A14	A10	WE	RST	A18	A17	A5	A2
C	A15	A12	A9	NC	NC	A6	A3	A1
D	A16	NC	I/O5	NC	I/O2	NC	CE	A0
E	NC	A-1	I/O6	NC	I/O3	NC	I/O0	GND
F	GND	I/O7	NC	I/O4	VCC	NC	I/O1	OE

AT49BV008A(T) Alternate Pin Definition
CBGA Top View (Ball Down)

	1	2	3	4	5	6	7	8
A	A14	A12	A8	VPP	NC	NC	A7	A4
B	A15	A10	WE	RST	A19	A18	A5	A2
C	A16	A13	A9	NC	NC	A6	A3	A1
D	A17	NC	I/O5	NC	I/O2	NC	CE	A0
E	NC	A11	I/O6	NC	I/O3	NC	I/O0	GND
F	GND	I/O7	NC	I/O4	VCC	NC	I/O1	OE

*Standard device is a NC. Please contact Atmel for VPP option.

The device is erased by executing the erase command sequence; the device internally controls the erase operation. The memory is divided into four blocks for erase operations. There are two 4K word parameter block sections, the boot block, and the main memory array block. The typical number of program and erase cycles is in excess of 10,000 cycles.

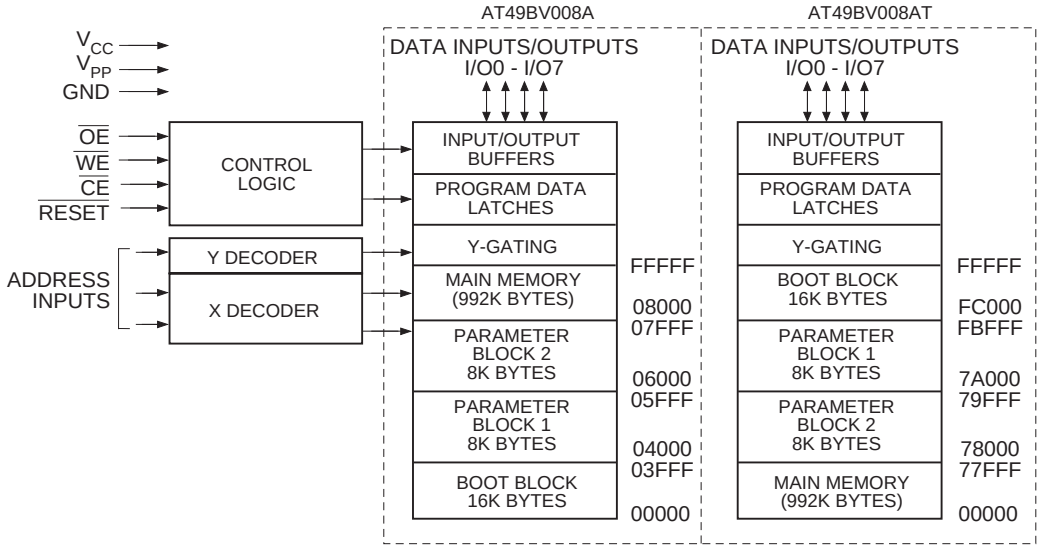
The optional 8K word boot block section includes a reprogramming lock out feature to provide data integrity. This feature is enabled by a command sequence. Once the boot block programming lockout feature is enabled, the data in the boot block cannot be changed when input levels of 3.6 volts or less are used. The boot sector is designed to contain user secure code.

For the AT49BV8192A(T), the $\overline{\text{BYTE}}$ pin controls whether the device data I/O pins operate in the byte or word configuration. If the $\overline{\text{BYTE}}$ pin is set at a logic “1” or left open, the device is in word configuration, I/O0 - I/O15 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$.

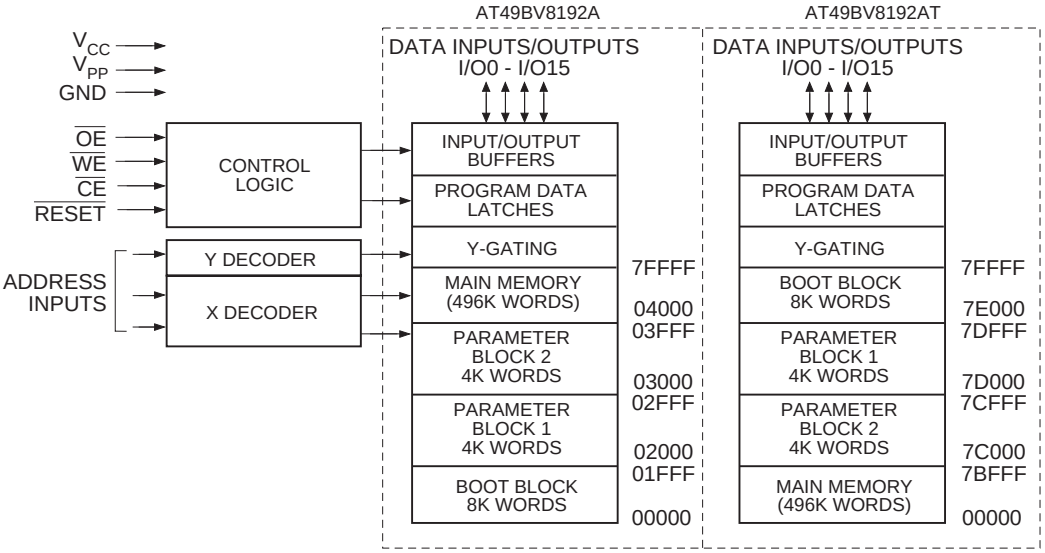
If the $\overline{\text{BYTE}}$ pin is set at logic “0”, the device is in byte configuration, and only data I/O pins I/O0 - I/O7 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$. The data I/O pins I/O8 - I/O14 are tri-stated and the I/O15 pin is used as an input for the LSB (A-1) address function.

An optional V_{PP} pin is available to improve program/erase times. Please contact Atmel for more information.

AT49BV008A(T) Block Diagram



AT49BV8192A(T) Block Diagram



Device Operation

READ: The AT49BV008A(T)/8192A(T) is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the

device is in its standard operating mode. A low level on the $\overline{\text{RESET}}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{\text{RESET}}$ pin, the device returns to the Read or Standby mode, depending upon the state of the control inputs. By applying a 12V ± 0.5V input signal to the $\overline{\text{RESET}}$ pin the boot block array can be reprogrammed even if the boot block program lockout feature has been enabled (see Boot Block Programming Lockout Override section).

ERASURE: Before a byte or word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase commands.

CHIP ERASE: The entire device can be erased at one time by using the 6-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC}.

If the boot block lockout has been enabled, the Chip Erase will not erase the data in the boot block; it will erase the main memory block and the parameter blocks only. After the chip erase, the device will return to the read or standby mode.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into four sectors that can be individually erased. There are two 4K word parameter block sections, one boot block, and the main memory array block. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling $\overline{\text{WE}}$ edge of the sixth cycle while the 30H data input command is latched at the rising edge of $\overline{\text{WE}}$. The sector erase starts after the rising edge of $\overline{\text{WE}}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. Whenever the main memory block is erased and reprogrammed, the two parameter blocks should be erased and reprogrammed before the main memory block is erased again. Whenever a parameter block is erased and reprogrammed, the other parameter block should be erased and reprogrammed before the first parameter block is erased again.

BYTE/WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a byte-by-byte or word-by-word basis. Programming is accomplished via the internal device command register and is a 4 bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified t_{BP} cycle time. The $\overline{\text{DATA}}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K words. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000H to 03FFFH for the AT49BV008A; FC000H to FFFFFH for the AT49BV008AT; 00000H to 01FFFH for the AT49BV8192A; and 7E000H to 7FFFFH for the AT49BV8192AT.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from the following address location will show if programming the boot block is locked out—00002H for the AT49BV008A and AT49BV8192A; FC002H for the AT49BV008AT; and 7E002H for the AT49BV8192AT. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been enabled and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

BOOT BLOCK PROGRAMMING LOCKOUT OVERRIDE: The user can override the boot block programming lockout by taking the $\overline{\text{RESET}}$ pin to 12 volts during the entire chip erase, sector erase or word programming operation. When the $\overline{\text{RESET}}$ pin is brought back to TTL levels the boot block programming lockout feature is again active.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49BV008A(T)/8192A(T) features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT49BV008A(T)/8192A(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

READY/$\overline{\text{BUSY}}$: For the AT49F008A(T), pin 12 is an open drain READY/$\overline{\text{BUSY}}$ output pin which provides another method of detecting the end of a program or erase operation. RDY/$\overline{\text{BUSY}}$ is actively pulled low during the internal program and erase cycles and it is released at the completion of the cycle. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{\text{BUSY}}$ line.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49BV008A(T)/8192A(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 2.7V to 3.6V power supply, the address inputs and control inputs ($\overline{\text{OE}}$, $\overline{\text{CE}}$, and $\overline{\text{WE}}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

AT49BV008A(T) ALTERNATE PIN DEFINITION: Two AT49BV008A(T) BGA pin definitions are shown. The standard pin definition allows use of the JEDEC standard programming algorithm. If the alternate pin definition is used, the programming algorithm must be modified as shown in the Command Definition for Alternate Pin Definition Table on page 7.

Command Definition in (in Hex)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA(4)	30
Byte/Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout(2)	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit(3)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit(3)	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   The ADDRESS FORMAT in each bus cycle is as follows: A15 - A0 (Hex), A-1, and A15 - A18 (Don't Care)
2. The boot sector has the address range 00000H to 03FFFH for the AT49BV008A; FC000H to FFFFFH for the AT49BV008AT; 00000H to 01FFFH for the AT49BV8192A; and 7E000H to 7FFFFH for the AT49BV8192AT.
3. Either one of the Product ID Exit commands can be used.
4. SA = sector addresses: (A0 - A18)
   For the AT49BV008A/8192A
   SA = 01XXX for BOOT BLOCK
   SA = 02XXX for PARAMETER BLOCK 1
   SA = 03XXX for PARAMETER BLOCK 2
   SA = 7FXXX for MAIN MEMORY ARRAY

   For the AT49BV008AT/8192AT
   SA = 7FXXX for BOOT BLOCK
   SA = 7DXXX for PARAMETER BLOCK 1
   SA = 7CXXX for PARAMETER BLOCK 2
   SA = 7BXXX for MAIN MEMORY ARRAY

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{RESET}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Command Definition (in Hex) for Alternate Pin Definition of AT49BV008A(T)[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	A555	AA	5AAA	55	A555	80	2555	AA	5AAA	55	A555	10
Sector Erase	6	A555	AA	5AAA	55	A555	80	2555	AA	5AAA	55	SA[4]	30
Byte/Word Program	4	A555	AA	5AAA	55	A555	A0	Addr	D_{IN}				
Boot Block Lockout[2]	6	A555	AA	5AAA	55	A555	80	2555	AA	5AAA	55	A555	40
Product ID Entry	3	A555	AA	5AAA	55	A555	90						
Product ID Exit[3]	3	A555	AA	5AAA	55	A555	F0						
Product ID Exit[3]	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   The ADDRESS FORMAT in each bus cycle is as follows: A15 - A0 (Hex), A-1, and A15 - A18 (Don't Care)
2. The boot sector has the address range 00000H to 03FFFH for the AT49BV008A; FC000H to FFFFFH for the AT49BV008AT; 00000H to 01FFFH for the AT49BV8192A; and 7E000H to 7FFFFH for the AT49BV8192AT.
3. Either one of the Product ID Exit commands can be used.
4. SA = sector addresses: (A0 - A18)
   For the AT49BV008A/8192A
   SA = 02XXX for BOOT BLOCK
   SA = 04XXX for PARAMETER BLOCK 1
   SA = 06XXX for PARAMETER BLOCK 2
   SA = FEXXX for MAIN MEMORY ARRAY

   For the AT49BV008AT/8192AT
   SA = FEXXX for BOOT BLOCK
   SA = FAXXX for PARAMETER BLOCK 1
   SA = 78XXX for PARAMETER BLOCK 2
   SA = 76XXX for MAIN MEMORY ARRAY

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{RESET}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49BV008A(T)/8192A(T)-12	AT49BV008A(T)/8192A(T)-15	AT49BV008A(T)/8192A(T)-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}[6]	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Program/Erase[2]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	5V ± 10%	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}	V_{IL}		
Program Inhibit	X	V_{IL}	X	V_{IH}	V_{IL}		
Output Disable	X	V_{IH}	X	V_{IH}	X		High Z
Reset	X	X	X	V_{IL}	X	X	High Z
Product Identification							
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}		A1 - A18 = V_{IL}, A9 = V_H,[3] A0 = V_{IL}	Manufacturer Code[4]
						A1 - A18 = V_{IL}, A9 = V_H,[3] A0 = V_{IH}	Device Code[4]
Software[5]				V_{IH}		A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code[4]
						A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH
   Device Code: 22H (AT49BV008A), A0H (AT49BV8192A), 21H (AT49BV008AT), A3H (AT49BV8192AT).
5. See details under Software Product Identification Entry/Exit.
6. A V_{PP} pin is optional. Please contact Atmel.

DC Characteristics

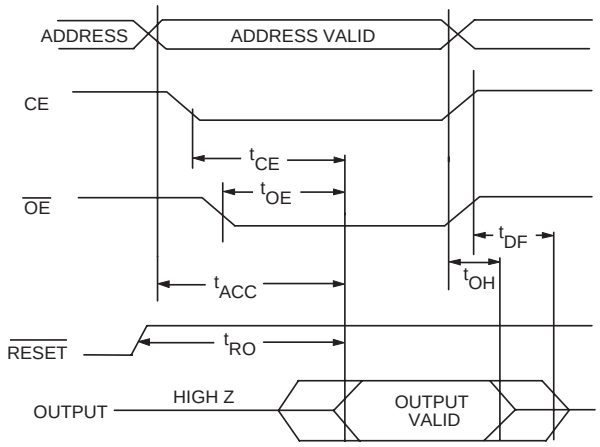
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1	mA
I_{CC}[1]	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		25	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Note: 1. In the erase mode, I_{CC} is 50 mA.

AC Read Characteristics

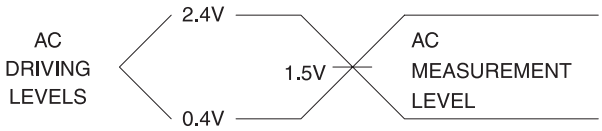
Symbol	Parameter	AT49BV008A(T)/8192A(T)-12		AT49BV008A(T)/8192A(T)-15		AT49BV008A(T)/8192A(T)-20		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}(1)	$\overline{CE}$ to Output Delay		120		150		200	ns
t_{OE}(2)	$\overline{OE}$ to Output Delay	0	50	0	70	0	70	ns
t_{DF}(3)(4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	30	0	40	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns
t_{RO}	$\overline{RESET}$ to Output Delay		800		800		800	ns

AC Read Waveforms(1)(2)(3)(4)



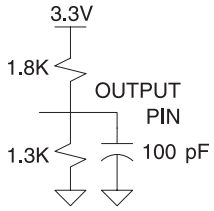
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C(1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

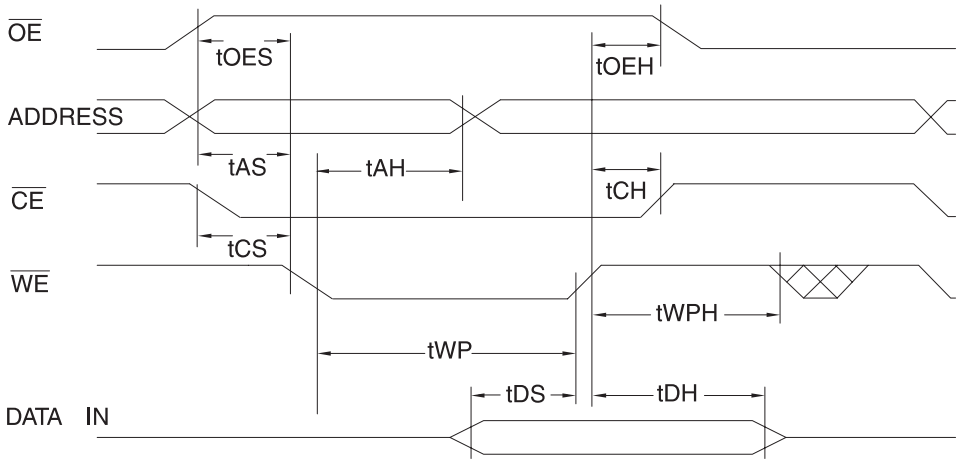
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

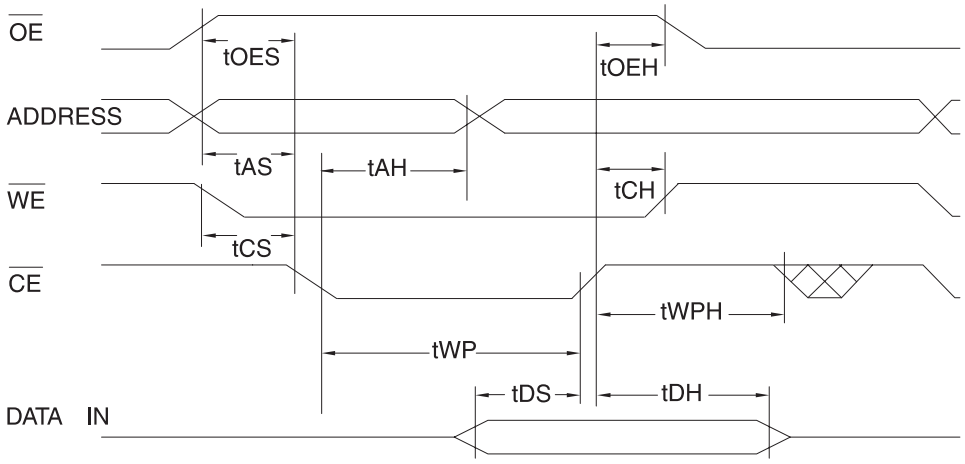
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	50		ns

AC Byte/Word Load Waveforms

$\overline{WE}$ Controlled



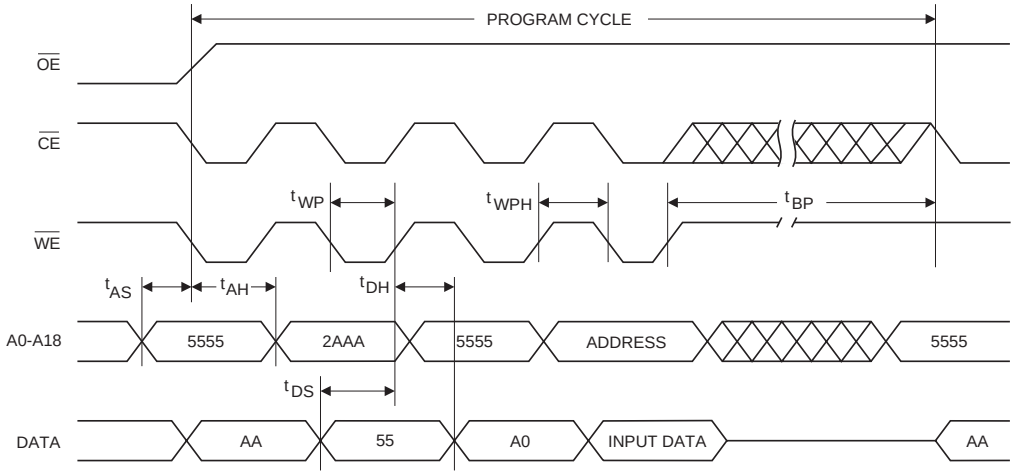
$\overline{CE}$ Controlled



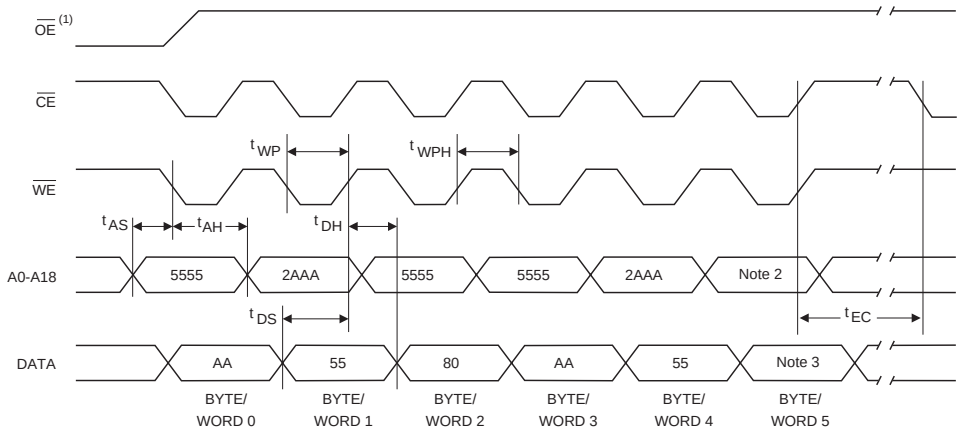
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte/Word Programming Time		30		µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	100			ns
t_{DS}	Data Set-up Time	100			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100			ns
t_{WPH}	Write Pulse Width High	50			ns
t_{EC}	Erase Cycle Time			10	seconds

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 4 under command definitions.)

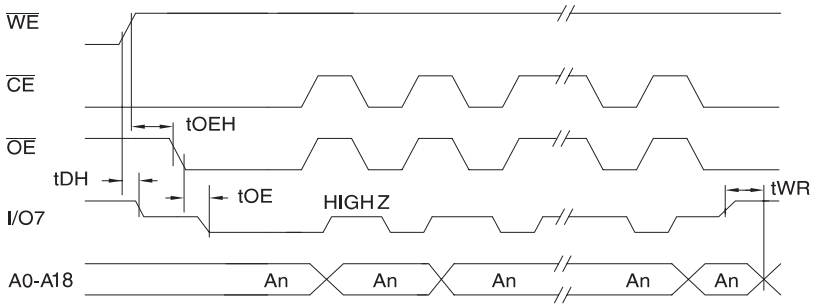
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

Data Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Data Polling Waveforms

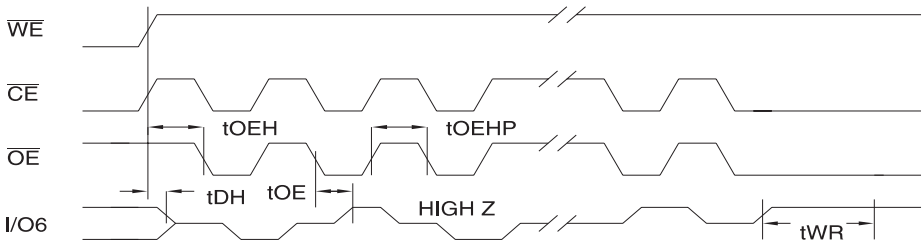


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

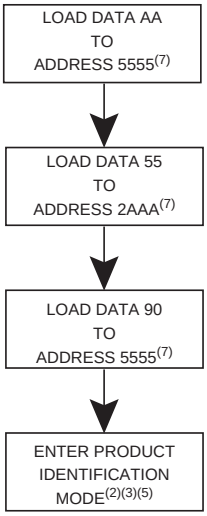
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms(1)(2)(3)

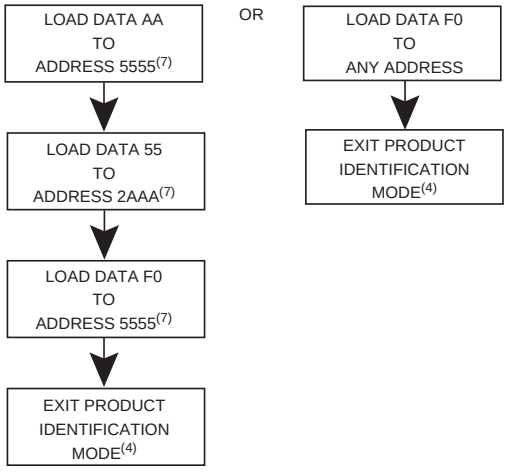


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

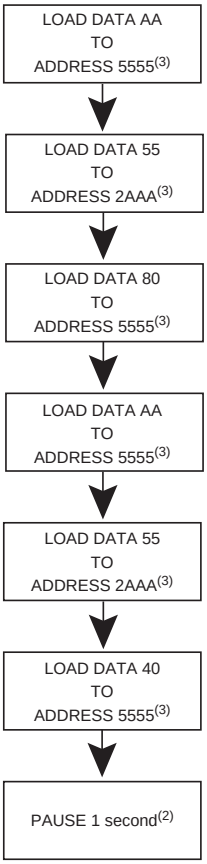


Software Product Identification Exit[1][6]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A15 - A0 (Hex), A-1, and A15 - A18 (Don't Care).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 22H (AT49BV008A), A0H (AT49BV8192A), 21H (AT49BV008AT), A3H (AT49BV8192AT)
6. Either one of the Product ID Exit commands can be used.
7. If the alternate pin definition is used, 5555 should be replaced with A555, 2AAA should be replaced with 5AAA.

Boot Block Lockout Enable Algorithm[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A15 - A0 (Hex), A-1, and A15 - A18 (Don't Care).
2. Boot block lockout feature enabled.
3. If the alternate pin definition is used, 5555 should be replaced with A555, 2AAA should be replaced with 5AAA.

AT49BV008A(T) Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.05	AT49BV008A-12TC AT49BV008A-12CC	40T 48C1	Commercial (0° to 70°C)
			AT49BV008A-12TI AT49BV008A-12CI	40T 48C1	Industrial (-40° to 85°C)
150	25	0.05	AT49BV008A-15TC AT49BV008A-15CC	40T 48C1	Commercial (0° to 70°C)
			AT49BV008A-15TI AT49BV008A-15CI	40T 48C1	Industrial (-40° to 85°C)
200	25	0.05	AT49BV008A-20TC AT49BV008A-20CC	40T 48C1	Commercial (0° to 70°C)
			AT49BV008A-20TI AT49BV008A-20CI	40T 48C1	Industrial (-40° to 85°C)
120	25	0.05	AT49BV008AT-12TC AT49BV008AT-12CC	40T 48C1	Commercial (0° to 70°C)
			AT49BV008AT-12TI AT49BV008AT-12CI	40T 48C1	Industrial (-40° to 85°C)
150	25	0.05	AT49BV008AT-15TC AT49BV008AT-15CC	40T 48C1	Commercial (0° to 70°C)
			AT49BV008AT-15TI AT49BV008AT-15CI	40T 48C1	Industrial (-40° to 85°C)
200	25	0.05	AT49BV008AT-20TC AT49BV008AT-20CC	40T 48C1	Commercial (0° to 70°C)
			AT49BV008AT-20TI AT49BV008AT-20CI	40T 48C1	Industrial (-40° to 85°C)

Package Type	
40T	40-Lead, Plastic Thin Small Outline Package (TSOP)
48C1	48-Ball, Chip-Size Ball Grid Array Package (CBGA)

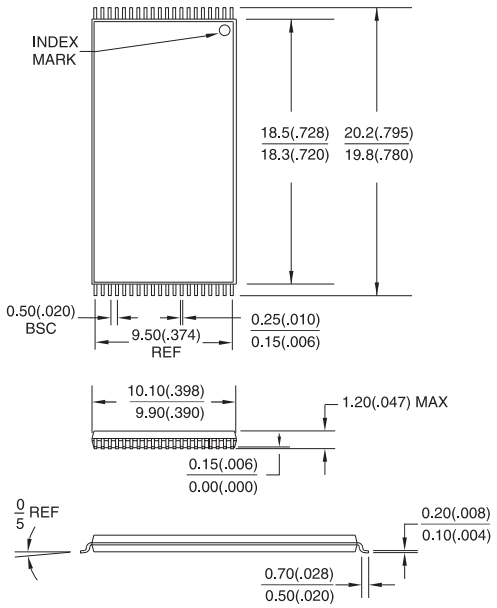
AT49BV8192A(T) Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.05	AT49BV8192A-12TC AT49BV8192A-12CC	48T 48C1	Commercial (0° to 70°C)
			AT49BV8192A-12TI AT49BV8192A-12CI	48T 48C1	Industrial (-40° to 85°C)
150	25	0.05	AT49BV8192A-15TC AT49BV8192A-15CC	48T 48C1	Commercial (0° to 70°C)
			AT49BV8192A-15TI AT49BV8192A-15CI	48T 48C1	Industrial (-40° to 85°C)
200	25	0.05	AT49BV8192A-20TC AT49BV8192A-20CC	48T 48C1	Commercial (0° to 70°C)
			AT49BV8192A-20TI AT49BV8192A-20CI	48T 48C1	Industrial (-40° to 85°C)
120	25	0.05	AT49BV8192AT-12TC AT49BV8192AT-12CC	48T 48C1	Commercial (0° to 70°C)
			AT49BV8192AT-12TI AT49BV8192AT-12CI	48T 48C1	Industrial (-40° to 85°C)
150	25	0.05	AT49BV8192AT-15TC AT49BV8192AT-15CC	48T 48C1	Commercial (0° to 70°C)
			AT49BV8192AT-15TI AT49BV8192AT-15CI	48T 48C1	Industrial (-40° to 85°C)
200	25	0.05	AT49BV8192AT-20TC AT49BV8192AT-20CC	48T 48C1	Commercial (0° to 70°C)
			AT49BV8192AT-20TI AT49BV8192AT-20CI	48T 48C1	Industrial (-40° to 85°C)

Package Type	
48T	48-Lead, Plastic Thin Small Outline Package (TSOP)
48C1	48-Ball, Chip-Size Ball Grid Array Package (CBGA)

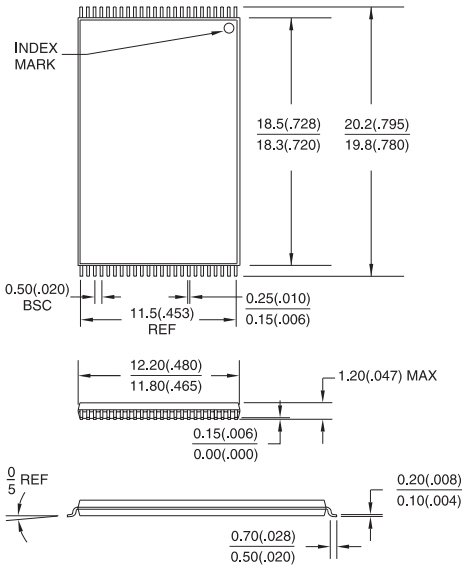
Packaging Information

40T, 40-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Inches and (Millimeters)



*Controlling dimension: millimeters

48T, 48-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 D



*Controlling dimension: millimeters

48C1, 48-Ball, Chip-Size Ball Grid Array Package (CBGA)
Dimensions in Millimeters

