Features

- MPEG I/II-Layer 3 Hardwired Decoder
  - Stand-alone MP3 Decoder
  - 48, 44.1, 32, 24, 22.05, 16 kHz Sampling Frequency
  - Separated Digital Volume Control on Left and Right Channels (Software Control Using 31 Steps)
  - Bass, Medium, and Treble Control (31 Steps)
  - Bass Boost Sound Effect
  - Ancillary Data Extraction
  - "CRC Error" and "MPEG Frame Synchronization" Indicators
- Programmable Audio Output for Interfacing With Common Audio DAC
  - PCM Format Compatible
  - I^2S Format Compatible
- 8-bit MCU C51 Core Based (F_{MAX} = 20 MHz)
- 2304 Bytes of Internal RAM
- 64K Bytes of Code Memory
  - Flash: AT89C51SND1C, ROM: AT83C51SND1C
- 4K Bytes of Boot Flash Memory (AT89C51SND1C)
  - ISP: Download from USB or UART to Any External Memory Cards
- USB Rev 1.1 Controller
  - "Full Speed" Data Transmission
- Built-in PLL
  - MP3 Audio Clocks
  - USB Clock
- MultiMedia Card™ Interface Compatibility
- Atmel DataFlash® SPI Interface Compatibility
- IDE/ATAPI Interface
- 2 Channels 10-bit ADC, 8 kHz (8-True Bit)
  - Battery Voltage Monitoring
  - Voice Recording Controlled by Software
- Up to 44 bits of General-purpose I/Os:
  - 4-bit Interrupt Keyboard Port for a 4 x n Matrix
  - SmartMedia™ Software Interface
- Standard Two 16-bit Timers/Counters
- Hardware Watchdog Timer
- Standard Full Duplex UART with Baud Rate Generator
- Two Wire Interface (TWI) Master and Slave Modes Controller
- SPI Master and Slave Modes Controller
- Power Management
  - Power-on Reset
  - Software Programmable MCU Clock
  - Idle Mode, Power-down Mode
- Operating Conditions:
  - 3V, ±10%, 25 mA Typical Operating at 25°C
  - Temperature Range: -40°C to +85°C
- Packages
  - TQFP80, PLCC84 (Development Board)
  - Dice

Description

The AT8xC51SND1C are fully integrated stand-alone hardwired MPEG I/II-Layer 3 decoders with a C51 microcontroller core handling data flow and MP3-player control.

The AT89C51SND1C includes 64K Bytes of Flash memory and allows In-System Programming through an embedded 4K Bytes of Boot Flash Memory.

Single-Chip Microcontroller with MP3 Decoder and Man-Machine Interface

AT83C51SND1C
AT89C51SND1C

Preliminary

Summary

Rev. 4106F–8051–10/02

The AT83C51SND1C includes 64K Bytes of ROM memory.

The AT8xC51SND1C includes 2304 Bytes of RAM memory.

The AT8xC51SND1C provides all necessary features for man machine interface like timers, keyboard port, serial or parallel interface (USB, TWI, SPI, IDE), ADC input, I^2S output, and all external memory interface (NAND or NOR Flash, SmartMedia, MultiMedia, DataFlash cards).

Typical Applications

- MP3 Player
- PDA, Camera, Mobile Phone MP3
- Car Audio/Multimedia MP3
- Home Audio/Multimedia MP3

Pin Descriptions

Figure 1. AT8xC51SND1C, 80-pin TQFP Package

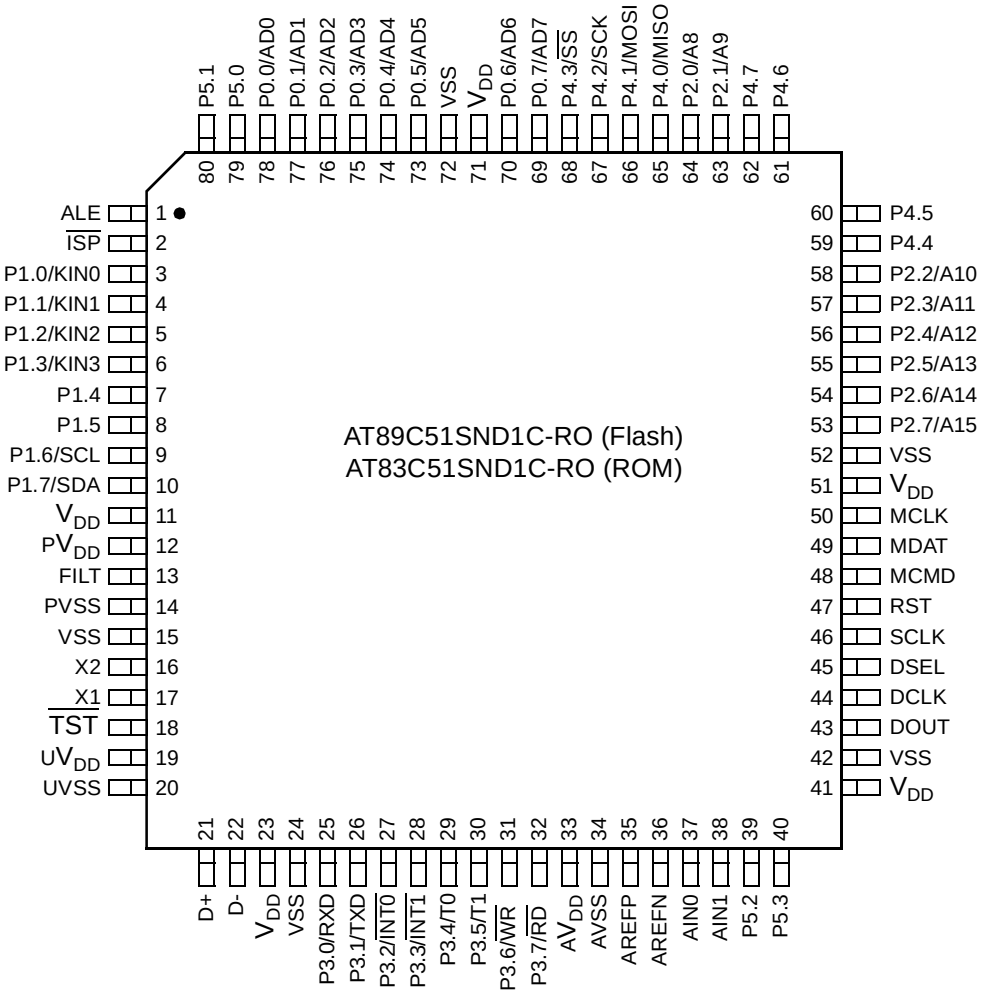
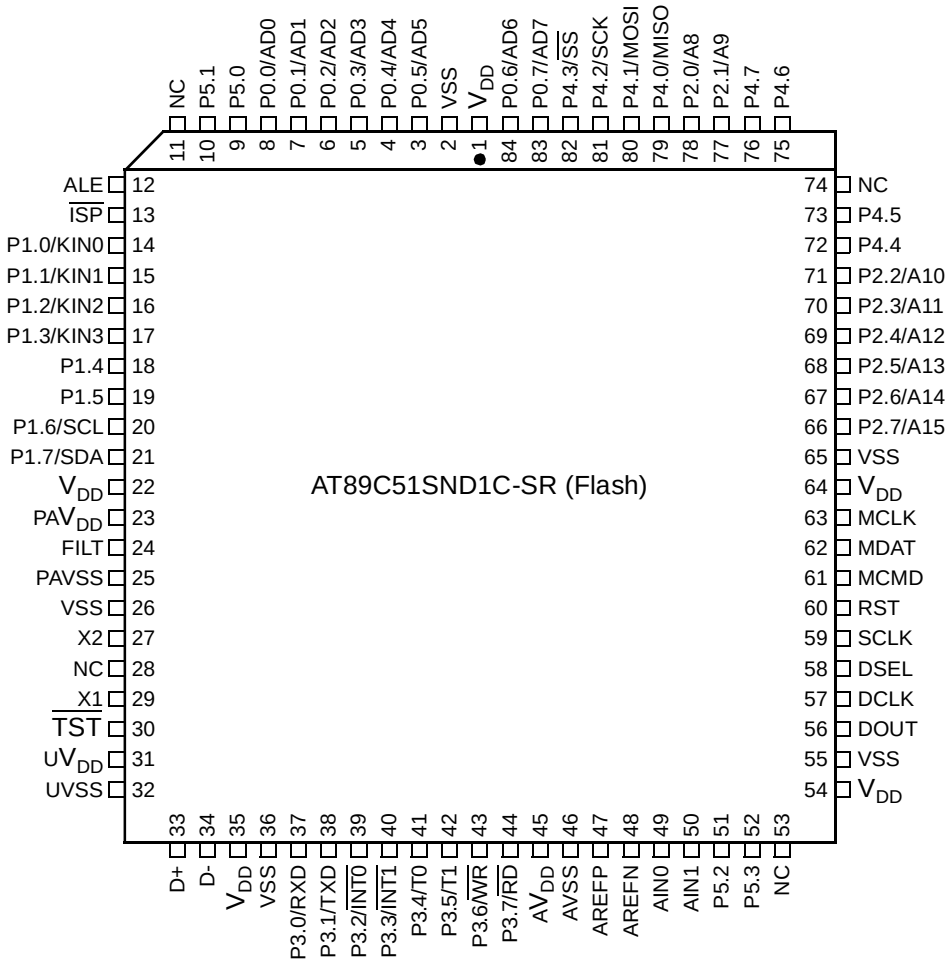


Figure 2. AT8xC51SND1C 84-pin PLCC Package[1]



Note: 1. Only samples for development board.

Pin Descriptions

All AT8xC51SND1C signals are detailed by functionality in Table 1 through Table 14.

Table 1. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0.7:0	I/O	**Port 0** P0 is an 8-bit open-drain bi-directional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.7:0	I/O	**Port 1** P1 is an 8-bit bi-directional I/O port with internal pull-ups.	KIN3:0 SCL SDA

Table 1. Ports Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
P2.7:0	I/O	**Port 2** P2 is an 8-bit bi-directional I/O port with internal pull-ups.	A15:8
P3.7:0	I/O	**Port 3** P3 is an 8-bit bi-directional I/O port with internal pull-ups.	RXD TXD $\overline{INT0}$ $\overline{INT1}$ T0 T1 $\overline{WR}$ $\overline{RD}$
P4.7:0	I/O	**Port 4** P4 is an 8-bit bi-directional I/O port with internal pull-ups.	MISO MOSI SCK $\overline{SS}$
P5.3:0	I/O	**Port 5** P5 is a 4-bit bi-directional I/O port with internal pull-ups.	-

Table 2. Clock Signal Description

Signal Name	Type	Description	Alternate Function
X1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. X1 is the clock source for internal timing.	-
X2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave X2 unconnected.	-
FILT	I	**PLL low pass filter input** FILT receives the RC network of the PLL low pass filter.	-

Table 3. Timer 0 and Timer 1 Signal Description

Signal Name	Type	Description	Alternate Function
$\overline{INT0}$	I	**Timer 0 Gate Input** $\overline{INT0}$ serves as external run control for timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** $\overline{INT0}$ input sets IE0 in the TCON register. If bit IT0 in this register is set, bit IE0 is set by a falling edge on $\overline{INT0}$. If bit IT0 is cleared, bit IE0 is set by a low level on $\overline{INT0}$.	P3.2
$\overline{INT1}$	I	**Timer 1 Gate Input** $\overline{INT1}$ serves as external run control for timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** $\overline{INT1}$ input sets IE1 in the TCON register. If bit IT1 in this register is set, bit IE1 is set by a falling edge on $\overline{INT1}$. If bit IT1 is cleared, bit IE1 is set by a low level on $\overline{INT1}$.	P3.3

Table 3. Timer 0 and Timer 1 Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
T0	I	**Timer 0 External Clock Input** When Timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4
T1	I	**Timer 1 External Clock Input** When Timer 1 operates as a counter, a falling edge on the T1 pin increments the count.	P3.5

Table 4. Audio Interface Signal Description

Signal Name	Type	Description	Alternate Function
DCLK	O	**DAC Data Bit Clock**	-
DOUT	O	**DAC Audio Data**	-
DSEL	O	**DAC Channel Select Signal** DSEL is the sample rate clock output.	-
SCLK	O	**DAC System Clock** SCLK is the oversampling clock synchronized to the digital audio data (DOUT) and the channel selection signal (DSEL).	-

Table 5. USB Controller Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	**USB Positive Data Upstream Port** This pin requires an external 1.5 kΩ pull-up to V_{DD} for full speed operation.	-
D-	I/O	**USB Negative Data Upstream Port**	-

Table 6. MutiMediaCard Interface Signal Description

Signal Name	Type	Description	Alternate Function
MCLK	O	**MMC Clock output** Data or command clock transfer.	-
MCMD	I/O	**MMC Command line** bi-directional command channel used for card initialization and data transfer commands. To avoid any parasitic current consumption, unused MCMD input must be polarized to V_{DD} or V_{SS}.	-
MDAT	I/O	**MMC Data line** bi-directional data channel. To avoid any parasitic current consumption, unused MDAT input must be polarized to V_{DD} or V_{SS}.	-

Table 7. UART Signal Description

Signal Name	Type	Description	Alternate Function
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1

Table 8. SPI Controller Signal Description

Signal Name	Type	Description	Alternate Function
MISO	I/O	**SPI Master Input Slave Output Data Line** When in master mode, MISO receives data from the slave peripheral. When in slave mode, MISO outputs data to the master controller.	P4.0
MOSI	I/O	**SPI Master Output Slave Input Data Line** When in master mode, MOSI outputs data to the slave peripheral. When in slave mode, MOSI receives data from the master controller.	P4.1
SCK	I/O	**SPI Clock Line** When in master mode, SCK outputs clock to the slave peripheral. When in slave mode, SCK receives clock from the master controller.	P4.2
$\overline{SS}$	I	**SPI Slave Select Line** When in controlled slave mode, $\overline{SS}$ enables the slave mode.	P4.3

Table 9. TWI Controller Signal Description

Signal Name	Type	Description	Alternate Function
SCL	I/O	**TWI Serial Clock** When TWI controller is in master mode, SCL outputs the serial clock to the slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller.	P1.6
SDA	I/O	**TWI Serial Data** SDA is the bi-directional TWI data line.	P1.7

Table 10. A/D Converter Signal Description

Signal Name	Type	Description	Alternate Function
AIN1:0	I	**A/D Converter Analog Inputs**	-
AREFP	I	**Analog Positive Voltage Reference Input**	-
AREFN	I	**Analog Negative Voltage Reference Input** This pin is internally connected to AVSS.	-

Table 11. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN3:0	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt.	P1.3:0

Table 12. External Access Signal Description

Signal Name	Type	Description	Alternate Function
A15:8	I/O	**Address Lines** Upper address lines for the external bus. Multiplexed higher address and data lines for the IDE interface.	P2.7:0
AD7:0	I/O	**Address/Data Lines** Multiplexed lower address and data lines for the external memory or the IDE interface.	P0.7:0
ALE	O	**Address Latch Enable Output** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A7:0. An external latch is used to demultiplex the address from address/data bus.	-
$\overline{ISP}$	I/O	**ISP Enable Input** This signal must be held to GND through a pull-down resistor at the falling reset to force execution of the internal bootloader.	-
$\overline{RD}$	O	**Read Signal** Read signal asserted during external data memory read operation.	P3.7
$\overline{WR}$	O	**Write Signal** Write signal asserted during external data memory write operation.	P3.6

Table 13. System Signal Description

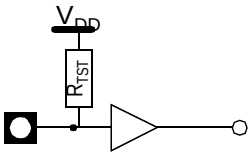
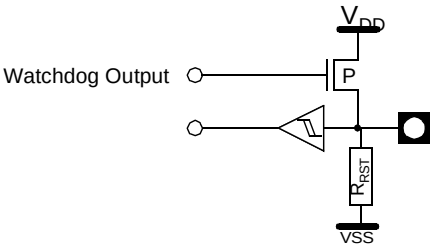
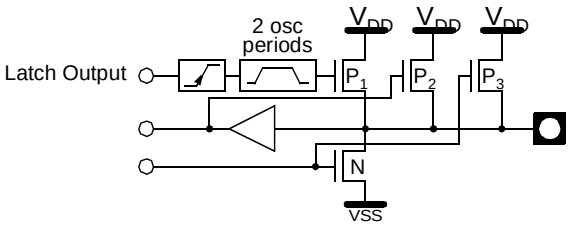
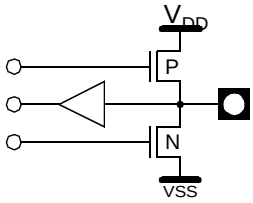
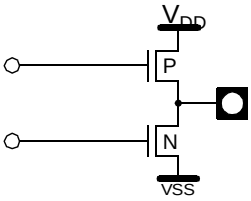
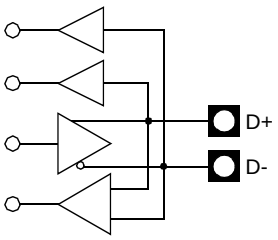
Signal Name	Type	Description	Alternate Function
RST	I	**Reset Input** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and V_{DD}. Asserting RST when the chip is in Idle mode or Power-down mode returns the chip to normal operation.	-
$\overline{TST}$	I	**Test Input** Test mode entry signal. This pin must be set to V_{DD}.	-

Table 14. Power Signal Description

Signal Name	Type	Description	Alternate Function
V_{DD}	PWR	**Digital Supply Voltage** Connect these pins to +3V supply voltage.	-
VSS	GND	**Circuit Ground** Connect these pins to ground.	-
AV_{DD}	PWR	**Analog Supply Voltage** Connect this pin to +3V supply voltage.	-
AVSS	GND	**Analog Ground** Connect this pin to ground.	-
PV_{DD}	PWR	**PLL Supply voltage** Connect this pin to +3V supply voltage.	-
PVSS	GND	**PLL Circuit Ground** Connect this pin to ground.	-
UV_{DD}	PWR	**USB Supply Voltage** Connect this pin to +3V supply voltage.	-
UVSS	GND	**USB Ground** Connect this pin to ground.	-

Internal Pin Structure

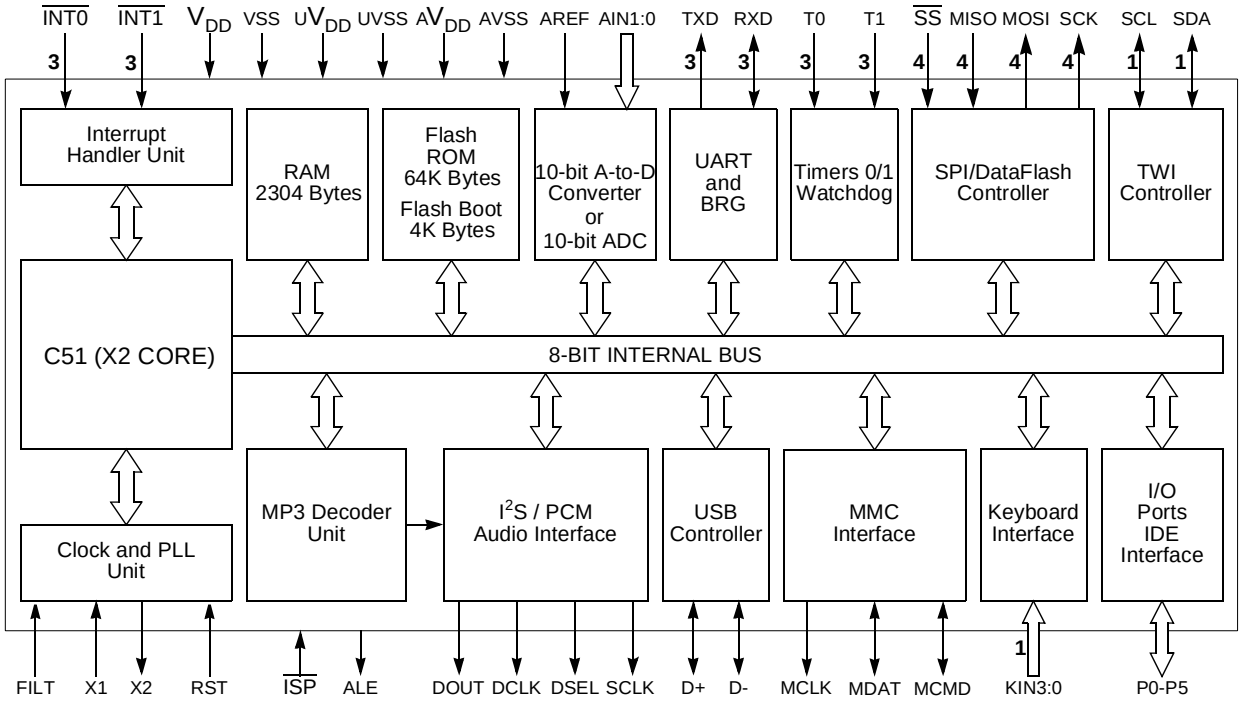
Table 15. Detailed Internal Pin Structure

Circuit[1]	Type	Pins
	Input	$\overline{TST}$
	Input/Output	RST
	Input/Output	P1[2] P2[3] P3 P4 P53:0
	Input/Output	P0 MCMD MDAT $\overline{ISP}$
	Output	ALE SCLK DCLK DOUT DSEL MCLK
	Input/Output	D+ D-

Notes:
1. For information on resistors value, input/output levels, and drive capability, refer to the Section “DC Characteristics”, page 24.
2. When the TWI controller is enabled, P_1, P_2, and P_3 transistors are disabled allowing pseudo open-drain structure.
3. In Port 2, P_1 transistor is continuously driven when outputting a high level bit address (A15:8).

Block Diagram

Figure 3. AT8xC51SND1C Block Diagram



Note: 1 Alternate function of Port 1
3 Alternate function of Port 3
4 Alternate function of Port 4

Application Information

Figure 4. AT8xC51SND1C Typical Application with On-board Atmel DataFlash and TWI LCD

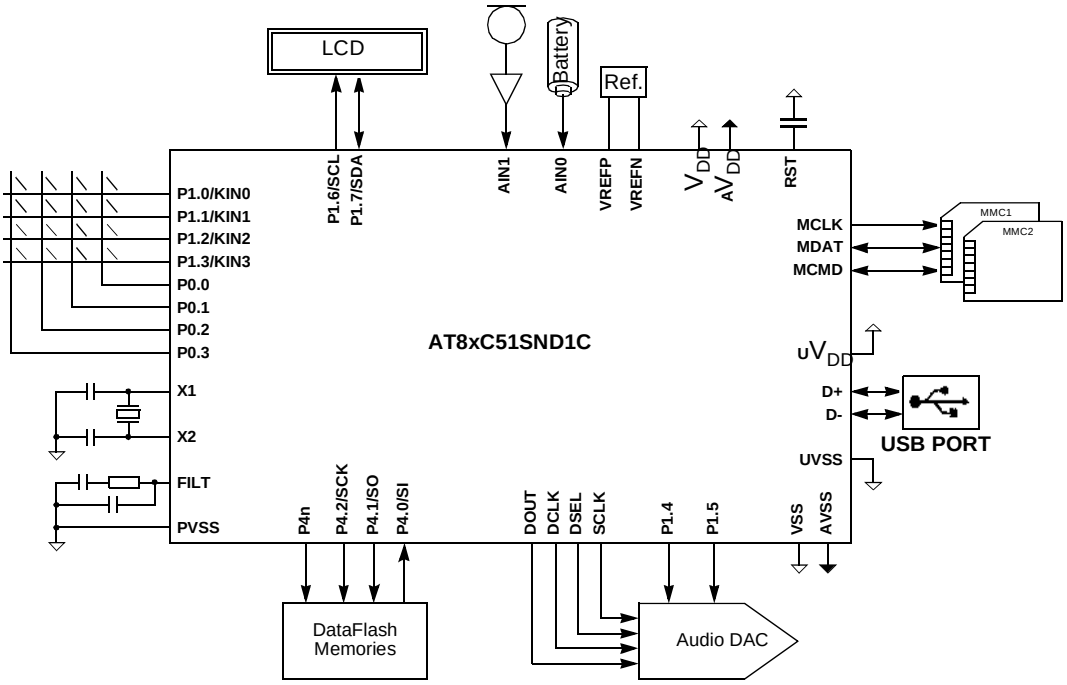


Figure 5. AT8xC51SND1C Typical Application with On-board Atmel DataFlash and LCD

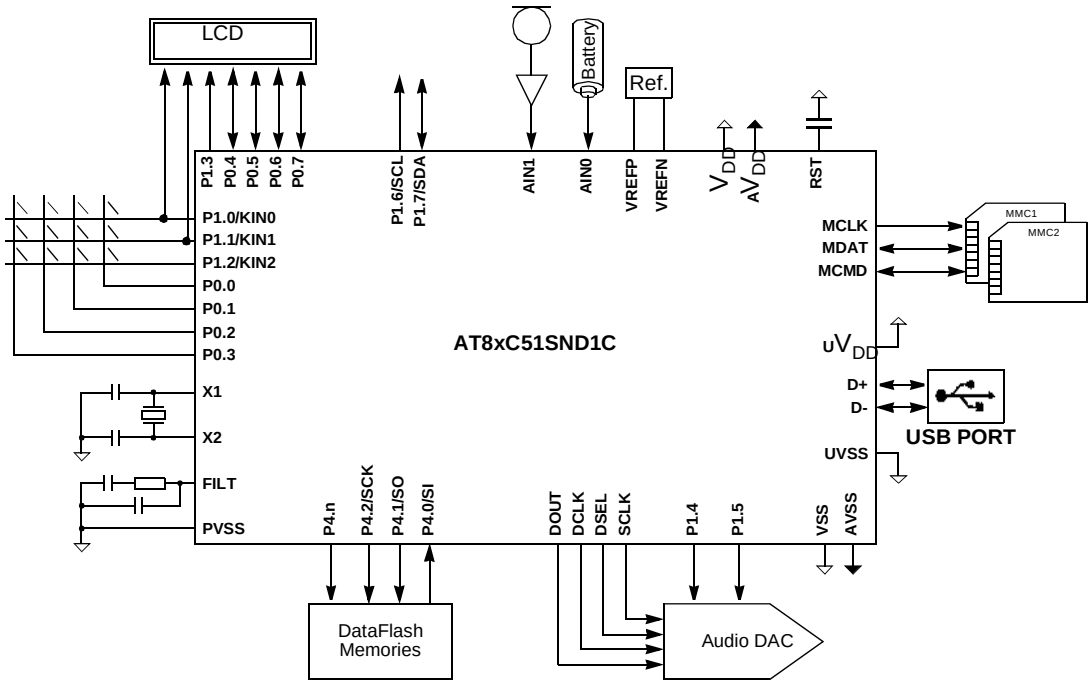


Figure 6. AT8xC51SND1C Typical Application with On-board SSFDC Flash

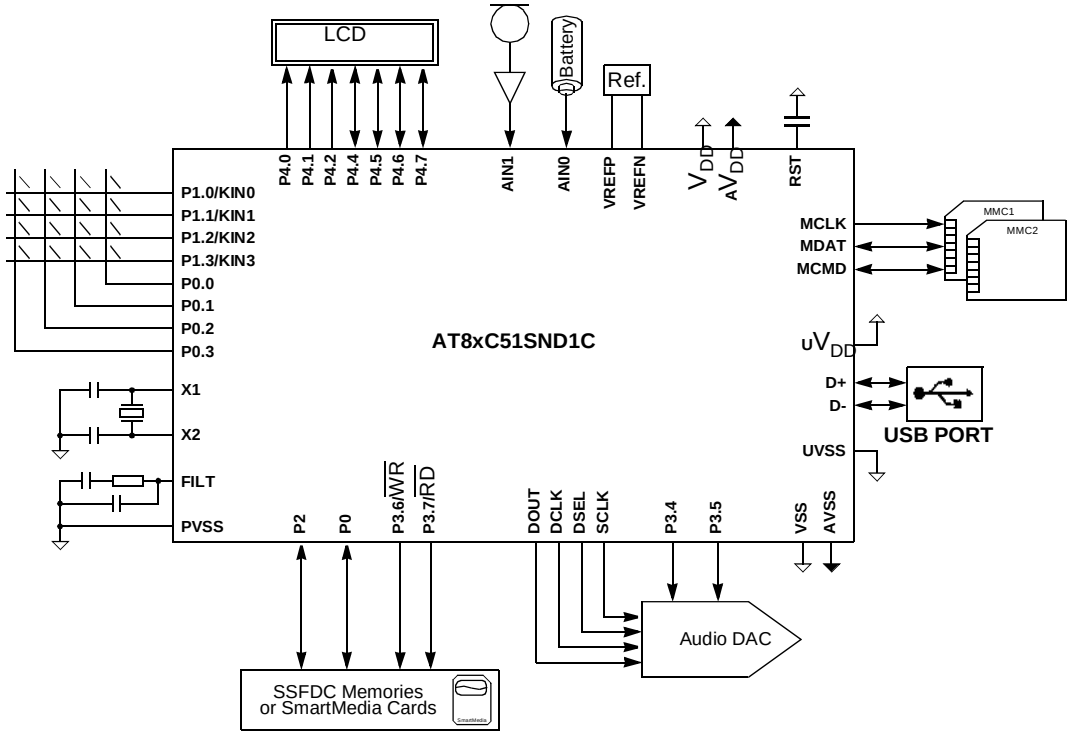
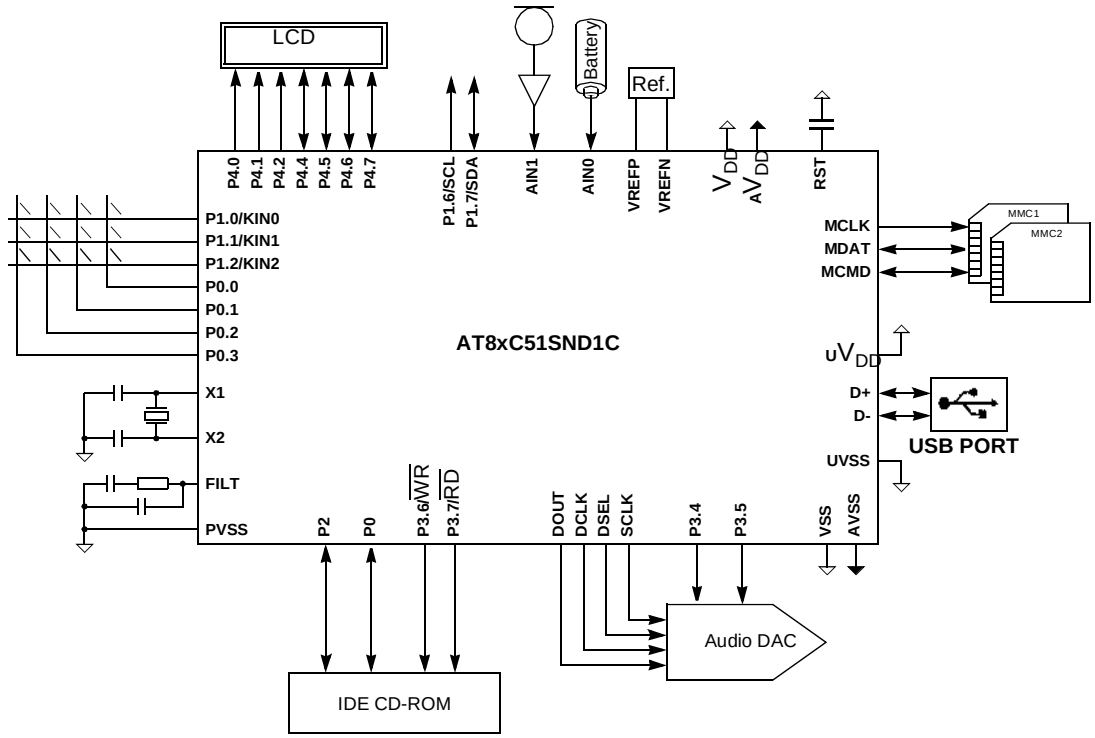


Figure 7. AT8xC51SND1C Typical Application with IDE CD-ROM Drive



Address Spaces

The AT8xC51SND1C derivatives implement four different address spaces:

- Program/Code Memory
- Boot Memory
- Data Memory
- Special Function Registers (SFRs)

Code Memory

The AT89C51SND1C and AT83C51SND1C implement 64K Bytes of on-chip program/code memory. The AT83C51SND1C product provides the internal program/code memory in ROM technology while the AT89C51SND1C product provides it in Flash technology.

The Flash memory increases ROM functionality by enabling in-circuit electrical erasure and programming. Thanks to the internal charge pump, the high voltage needed for programming or erasing Flash cells is generated on-chip using the standard V_{DD} voltage. Thus, the AT89C51SND1C can be programmed using only one voltage and allows in application software programming commonly known as IAP. Hardware programming mode is also available using specific programming tools.

Boot Memory

The AT89C51SND1C implements 4K Bytes of on-chip boot memory provided in Flash technology. This boot memory is delivered programmed with a standard bootloader software allowing In-system Programming commonly known as ISP. It also contains some Application Programming Interfaces routines commonly known as API allowing user to develop his own bootloader.

Data Memory

The AT8xC51SND1 derivatives implement 2304 Bytes of on-chip data RAM. This memory is divided in two separate areas:

- 256 Bytes of on-chip RAM memory (standard C51 memory).
- 2048 Bytes of on-chip expanded RAM memory (ERAM accessible via MOVX instructions).

Special Function Registers

The Special Function Registers (SFRs) of the AT8xC51SND1 derivatives fall into the categories detailed in Table 16 through Table 32. The relative addresses of these SFRs are provided together with their reset values in Table 33. In this table, the bit-addressable registers are identified by Note 1.

Table 16. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator	–	–	–	–	–	–	–	–
B	F0h	B Register	–	–	–	–	–	–	–	–
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer	–	–	–	–	–	–	–	–
DPL	82h	Data Pointer Low byte	–	–	–	–	–	–	–	–
DPH	83h	Data Pointer High byte	–	–	–	–	–	–	–	–

Table 17. System Management SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1	SMOD0	–	–	GF1	GF0	PD	IDL
AUXR	8Eh	Auxiliary Register 0	–	EXT16	M0	DPHDIS	XRS1	XRS0	EXTRAM	AO
AUXR1	A2h	Auxiliary Register 1	–	–	ENBOOT	–	GF3	0	–	DPS
NVERS	FBh	Version Number	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0

Table 18. PLL and System Clock SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CKCON	8Fh	Clock Control	–	–	–	–	–	–	–	X2
PLLCON	E9h	PLL Control	R1	R0	–	–	PLLRES	–	PLLEN	PLOCK
PLLNDIV	EEh	PLL N Divider	–	N6	N5	N4	N3	N2	N1	N0
PLLRDIV	EFh	PLL R Divider	R9	R8	R7	R6	R5	R4	R3	R2

Table 19. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EAUD	EMP3	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	–	EUSB	–	EKB	EADC	ESPI	EI2C	EMMC
IPH0	B7h	Interrupt Priority Control High 0	–	IPHAUD	IPHMP3	IPHS	IPHT1	IPHX1	IPHT0	IPHX0
IPL0	B8h	Interrupt Priority Control Low 0	–	IPLAUD	IPLMP3	IPLS	IPLT1	IPLX1	IPLT0	IPLX0
IPH1	B3h	Interrupt Priority Control High 1	–	IPHUSB	–	IPHKB	IPHADC	IPHSPI	IPHI2C	IPHMMC
IPL1	B2h	Interrupt Priority Control Low 1	–	IPLUSB	–	IPLKB	IPLADC	IPLSPI	IPLI2C	IPLMMC

Table 20. Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	8-bit Port 0	–	–	–	–	–	–	–	–
P1	90h	8-bit Port 1	–	–	–	–	–	–	–	–
P2	A0h	8-bit Port 2	–	–	–	–	–	–	–	–
P3	B0h	8-bit Port 3	–	–	–	–	–	–	–	–
P4	C0h	8-bit Port 4	–	–	–	–	–	–	–	–
P5	D8h	4-bit Port 5	–	–	–	–	–	–	–	–

Table 21. Flash Memory SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
FCON	D1h	Flash Control	FPL3	FPL2	FPL1	FPL0	FPS	FMOD1	FMOD0	FBUSY

Table 22. Timer SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TCON	88h	Timer/Counter 0 and 1 Control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
TL0	8Ah	Timer/Counter 0 Low Byte	–	–	–	–	–	–	–	–
TH0	8Ch	Timer/Counter 0 High Byte	–	–	–	–	–	–	–	–
TL1	8Bh	Timer/Counter 1 Low Byte	–	–	–	–	–	–	–	–

Table 22. Timer SFRs (Continued)

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TH1	8Dh	Timer/Counter 1 High Byte	–	–	–	–	–	–	–	–
WDTRST	A6h	WatchDog Timer Reset	–	–	–	–	–	–	–	–
WDTPRG	A7h	WatchDog Timer Program	–	–	–	–	–	WTO2	WTO1	WTO0

Table 23. MP3 Decoder SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
MP3CON	AAh	MP3 Control	MPEN	MPBBST	CRCEN	MSKANC	MSKREQ	MSKLAY	MSKSYN	MSKCRC
MP3STA	C8h	MP3 Status	MPANC	MPREQ	ERRLAY	ERRSYN	ERRCRC	MPFS1	MPFS0	MPVER
MP3STA1	AFh	MP3 Status 1	–	–	–	MPFREQ	MPBREQ	–	–	–
MP3DAT	ACh	MP3 Data	MPD7	MPD6	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0
MP3ANC	ADh	MP3 Ancillary Data	AND7	AND6	AND5	AND4	AND3	AND2	AND1	AND0
MP3VOL	9Eh	MP3 Audio Volume Control Left	–	–	–	VOL4	VOL3	VOL2	VOL1	VOL0
MP3VOR	9Fh	MP3 Audio Volume Control Right	–	–	–	VOR4	VOR3	VOR2	VOR1	VOR0
MP3BAS	B4h	MP3 Audio Bass Control	–	–	–	BAS4	BAS3	BAS2	BAS1	BAS0
MP3MED	B5h	MP3 Audio Medium Control	–	–	–	MED4	MED3	MED2	MED1	MED0
MP3TRE	B6h	MP3 Audio Treble Control	–	–	–	TRE4	TRE3	TRE2	TRE1	TRE0
MP3CLK	EBh	MP3 Clock Divider	–	–	–	MPCD4	MPCD3	MPCD2	MPCD1	MPCD0

Table 24. Audio Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
AUDCON0	9Ah	Audio Control 0	JUST4	JUST3	JUST2	JUST1	JUST0	POL	DSIZ	HLR
AUDCON1	9Bh	Audio Control 1	SRC	DRQEN	MSREQ	MUDRN	–	DUP1	DUP0	AUDEN
AUDSTA	9Ch	Audio Status	SREQ	UDRN	AUBUSY	–	–	–	–	–
AUDDAT	9Dh	Audio Data	AUD7	AUD6	AUD5	AUD4	AUD3	AUD2	AUD1	AUD0
AUDCLK	ECh	Audio Clock Divider	–	–	–	AUCD4	AUCD3	AUCD2	AUCD1	AUCD0

Table 25. USB Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
USBCON	BCh	USB Global Control	USBE	SUSPCLK	SDRMWUP	–	UPRSM	RMWUPE	CONFG	FADDEN
USBADDR	C6h	USB Address	FEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0
USBINT	BDh	USB Global Interrupt	–	–	WUPCPU	EORINT	SOFINT	–	–	SPINT
USBIEN	BEh	USB Global Interrupt Enable	–	–	EWUPCPU	EEORINT	ESOFINT	–	–	ESPINT
UEPNUM	C7h	USB Endpoint Number	–	–	–	–	–	–	EPNUM1	EPNUM0
UEPCONX	D4h	USB Endpoint X Control	EPEN	–	–	–	DTGL	EPDIR	EPTYPE1	EPTYPE0
UEPSTAX	CEh	USB Endpoint X Status	DIR	–	STALLRQ	TXRDY	STLCRC	RXSETUP	RXOUT	TXCMP
UEPRST	D5h	USB Endpoint Reset	–	–	–	–	EP3RST	EP2RST	EP1RST	EP0RST
UEPINT	F8h	USB Endpoint Interrupt	–	–	–	–	EP3INT	EP2INT	EP1INT	EP0INT
UEPIEN	C2h	USB Endpoint Interrupt Enable	–	–	–	–	EP3INTE	EP2INTE	EP1INTE	EP0INTE
UEPDATX	CFh	USB Endpoint X FIFO Data	FDAT7	FDAT6	FDAT5	FDAT4	FDAT3	FDAT2	FDAT1	FDAT0
UBYCTX	E2h	USB Endpoint X Byte Counter	-	BYCT6	BYCT5	BYCT4	BYCT3	BYCT2	BYCT1	BYCT0
UFNUML	BAh	USB Frame Number Low	FNUM7	FNUM6	FNUM5	FNUM4	FNUM3	FNUM2	FNUM1	FNUM0
UFNUMH	BBh	USB Frame Number High	–	–	CRCOK	CRCERR	–	FNUM10	FNUM9	FNUM8
USBCLK	EAh	USB Clock Divider	–	–	–	–	–	–	USBCD1	USBCD0

Table 26. MMC Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
MMCON0	E4h	MMC Control 0	DRPTR	DTPTR	CRPTR	CTPTR	MBLOCK	DFMT	RFMT	CRCDIS
MMCON1	E5h	MMC Control 1	BLEN3	BLEN2	BLEN1	BLEN0	DATDIR	DATEN	RESPEN	CMDEN
MMCON2	E6h	MMC Control 2	MMCEN	DCR	CCR	–	–	DATD1	DATD0	FLOWC
MMSTA	DEh	MMC Control and Status	–	–	CBUSY	CRC16S	DATFS	CRC7S	RESPFS	CFLCK
MMINT	E7h	MMC Interrupt	MCBI	EORI	EOCI	EOFI	F2FI	F1FI	F2EI	F1EI
MMMSK	DFh	MMC Interrupt Mask	MCBM	EORM	EOCM	EOFM	F2FM	F1FM	F2EM	F1EM
MMCMD	DDh	MMC Command	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
MMDAT	DCh	MMC Data	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
MMCLK	EDh	MMC Clock Divider	MMCD7	MMCD6	MMCD5	MMCD4	MMCD3	MMCD2	MMCD1	MMCD0

Table 27. IDE Interface SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
DAT16H	F9h	High Order Data Byte	D15	D14	D13	D12	D11	D10	D9	D8

Table 28. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer	–	–	–	–	–	–	–	–
SADEN	B9h	Slave Address Mask	–	–	–	–	–	–	–	–
SADDR	A9h	Slave Address	–	–	–	–	–	–	–	–
BDRCON	92h	Baud Rate Control	–	–	–	BRR	TBCK	RBCK	SPD	SRC
BRL	91h	Baud Rate Reload	–	–	–	–	–	–	–	–

Table 29. SPI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SPCON	C3h	SPI Control	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
SPSTA	C4h	SPI Status	SPIF	WCOL	–	MODF	–	–	–	–
SPDAT	C5h	SPI Data	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Table 30. TWI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SSCON	93h	Synchronous Serial Control	SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
SSSTA	94h	Synchronous Serial Status	SSC4	SSC3	SSC2	SSC1	SSC0	0	0	0
SSDAT	95h	Synchronous Serial Data	SSD7	SSD6	SSD5	SSD4	SSD3	SSD2	SSD1	SSD0
SSADR	96h	Synchronous Serial Address	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSGC

Table 31. Keyboard Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBCON	A3h	Keyboard Control	KINL3	KINL2	KINL1	KINL0	KINM3	KINM2	KINM1	KINM0
KBSTA	A4h	Keyboard Status	KPDE	–	–	–	KINF3	KINF2	KINF1	KINF0

Table 32. A/D Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ADCON	F3h	ADC Control	–	ADIDL	ADEN	ADEOC	ADSST	–	–	ADCS
ADCLK	F2h	ADC Clock Divider	–	–	–	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
ADDL	F4h	ADC Data Low Byte	–	–	–	–	–	–	ADAT1	ADAT0
ADDH	F5h	ADC Data High Byte	ADAT9	ADAT8	ADAT7	ADAT6	ADAT5	ADAT4	ADAT3	ADAT2

Table 33. SFR Addresses and Reset Values

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	UEPINT 0000 0000	DAT16H XXXX XXXX		NVERS[2] 1000 0100					FFh
F0h	B[1] 0000 0000		ADCLK 0000 0000	ADCON 0000 0000	ADDL 0000 0000	ADDH 0000 0000			F7h
E8h		PLLCON 0000 1000	USBCLK 0000 0000	MP3CLK 0000 0000	AUDCLK 0000 0000	MMCLK 0000 0000	PLLNDIV 0000 0000	PLLRDIV 0000 0000	EFh
E0h	ACC[1] 0000 0000		UBYCTLX 0000 0000		MMCON0 0000 0000	MMCON1 0000 0000	MMCON2 0000 0000	MMINT 0000 0011	E7h
D8h	P5[1] XXXX 1111				MMDAT 1111 1111	MMCMD 1111 1111	MMSTA 0000 0000	MMMSK 1111 1111	DFh
D0h	PSW[1] 0000 0000	FCON[3] 1111 0000[4]			UEPCONX 0000 0000	UEPRST 0000 0000			D7h
C8h	MP3STA[1] 0000 0001						UEPSTAX 0000 0000	UEPDATX 0000 0000	CFh
C0h	P4[1] 1111 1111		UEPIEN 0000 0000	SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX	USBADDR 1000 0000	UEPNUM 0000 0000	C7h
B8h	IPL0[1] X000 0000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0001 0000		BFh
B0h	P3[1] 1111 1111	IEN1 0000 0000	IPL1 0000 0000	IPH1 0000 0000	MP3BAS 0000 0000	MP3MED 0000 0000	MP3TRE 0000 0000	IPH0 X000 0000	B7h
A8h	IEN0[1] 0000 0000	SADDR 0000 0000	MP3CON 0011 1111		MP3DAT 0000 0000	MP3ANC 0000 0000		MP3STA1 0100 0001	AFh
A0h	P2[1] 1111 1111		AUXR1 XXXX 00X0	KBCON 0000 1111	KBSTA 0000 0000		WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	AUDCON0 0000 1000	AUDCON1 1011 0010	AUDSTA 1100 0000	AUDDAT 1111 1111	MP3VOL 0000 0000	MP3VOR 0000 0000	9Fh
90h	P1[1] 1111 1111	BRL 0000 0000	BDRCON XXX0 0000	SSCON 0000 0000	SSSTA 1111 1000	SSDAT 1111 1111	SSADR 1111 1110		97h
88h	TCON[1] 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR X000 1101	CKCON 0000 000X[5]	8Fh
80h	P0[1] 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON XXXX 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Notes:
1. SFR registers with least significant nibble address equal to 0 or 8 are bit-addressable.
2. NVERS reset value depends on the silicon version.
3. FCON register is only available in AT89C51SND1C product.
4. FCON reset value is 00h in case of reset with hardware condition.
5. CKCON reset value depends on the X2B bit (programmed or unprogrammed) in the Hardware Byte.

Peripherals

Clock Generator System

The AT8xC51SND1C internal clocks are extracted from an on-chip PLL fed by an on-chip oscillator. Four clocks are generated respectively for the C51 core, the MP3 decoder, the audio interface, and the other peripherals. The C51 and peripheral clocks are derived from the oscillator clock. The MP3 decoder clock is generated by dividing the PLL output clock. The audio interface sample rates are also obtained by dividing the PLL output clock.

Ports

The AT8xC51SND1C implement five 8-bit ports (P0 - P4) and one 4-bit port (P5). In addition to performing general-purpose I/Os, some ports are capable of external data memory operations; others allow for alternate functions. All I/O Ports are bi-directional. Each Port contains a latch, an output driver and an input buffer. Port 0 and Port 2 output drivers and input buffers facilitate external memory operations. Some Port 1, Port 3 and Port 4 pins serve for both general-purpose I/Os and alternate functions.

Timers/Counters

The AT8xC51SND1C implement the two general-purpose, 16-bit Timers/Counters of a standard C51. They are identified as Timer 0, Timer 1, and can independently be configured each to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, a Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

Watchdog Timer

The AT8xC51SND1C implement a hardware Watchdog Timer that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

MP3 Decoder

The AT8xC51SND1C implements a MPEG I/II audio layer 3 decoder (MP3 decoder).

In MPEG I (ISO 11172-3) three layers of compression have been standardized supporting three sampling frequencies: 48, 44.1, and 32 kHz. Among these layers, layer 3 allows highest compression rate of about 12:1 while still maintaining CD audio quality. For example, 3 minutes of CD audio (16-bit PCM, 44.1 kHz) data, which needs about 32M bytes of storage, can be encoded into only 2.7 MBytes of MPEG I audio layer 3 data.

In MPEG II (ISO 13818-3), three additional sampling frequencies: 24, 22.05, and 16 kHz are supported for low bit rates applications.

The AT8xC51SND1C can decode in real-time the MPEG I audio layer 3 encoded data into a PCM audio data, and also supports MPEG II audio layer 3 additional frequencies.

Additional features are supported by the AT8xC51SND1C MP3 decoder such as volume, bass, medium, and treble controls, bass boost effect and ancillary data extraction.

Audio Output Interface

The AT8xC51SND1C implements an audio output interface allowing the decoded audio bitstream to be output in various formats. It is compatible with right and left justification PCM and I^2S formats and the on-chip PLL (see Section “Clock Generator System”) allows connection of almost all of the commercial audio DAC families available on the market.

Universal Serial Bus Interface

The AT8xC51SND1C implement a full-speed USB Interface. It can be used for the following purposes:

- Download of MP3 encoded audio files by supporting the USB mass storage class.
- In-System Programming by supporting the USB firmware upgrade class.

MultiMedia Card Interface

The AT8xC51SND1C implement a MultiMedia Card (MMC) interface compliant to the V2.2 specification in MultiMedia Card mode. The MMC allows storage of MP3 encoded audio files in removable Flash memory cards that can be easily plugged to, or removed from the application. It can also be used for In-System Programming.

IDE/ATAPI Interface

The AT8xC51SND1C provide an IDE/ATAPI interface allowing connection of devices such as CD-ROM reader, CompactFlash™ cards, Hard Disk Drive, etc. It consists of a 16-bit bi-directional bus part of the low-level ANSI ATA/ATAPI specification. It is provided for mass storage interfaces but could be used for In-System Programming using CD-ROM.

Serial I/O Interface

The AT8xC51SND1C implement a serial port with its own baud rate generator providing one single synchronous communication mode and three full-duplex Universal Asynchronous Receiver Transmitter (UART) communication modes. It is provided for the following purposes:

- In-System Programming.
- Remote control of the AT8xC51SND1C by a host.

Serial Peripheral Interface

The AT8xC51SND1C implement a Serial Peripheral Interface (SPI) supporting master and slave modes. It is provided for the following purposes:

- Interfacing DataFlash memory and DataFlash cards for MP3 encoded audio files storage
- Remote control of the AT8xC51SND1C by a host
- In-System Programming

TWI Controller

The AT8xC51SND1C implements a TWI controller supporting the four standard master and slave modes with multimaster capability. It is provided for the following purposes:

- Connection of slave devices like LCD controller, audio DAC…
- Remote control of the AT8xC51SND1C by a host
- In-System Programming

A/D Controller

The AT8xC51SND1C implements a 2-channel 10-bit (8 true bits) analog-to-digital converter (ADC). It is provided for the following purposes:

- Battery monitoring
- Voice recording
- Corded remote control

Keyboard Interface

The AT8xC51SND1C implement a keyboard interface allowing connection of 4 x n matrix keyboard. It is based on 4 inputs with programmable interrupt capability on both high or low level. These inputs are available as an alternate function of P1.3:0 and allow exit from idle and power-down modes.

Electrical Characteristics

Absolute Maximum Rating

Storage Temperature	-65 to +150°C
Voltage on any other Pin to V_{SS}	-0.3 to +4.0V
I_{OL} per I/O Pin	5 mA
Power Dissipation	1 W
Ambient Temperature Under Bias	-40 to +85°C
V_{DD}	2.7 to 3.3V

NOTE: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

DC Characteristics

Digital Logic

Table 34. Digital DC Characteristics V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

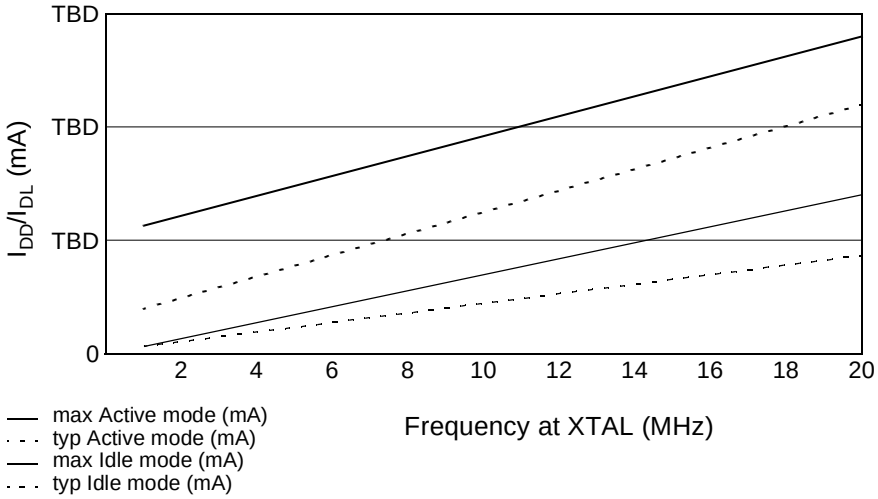
Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 \cdot V_{DD} - 0.1$	V	
V_{IH1}	Input High Voltage (except RST)	$0.2 \cdot V_{DD} + 0.9$		V_{DD}	V	
V_{IH2}	Input High Voltage (RST)	$0.7 \cdot V_{DD}$		$V_{DD} + 0.5$	V	
V_{OL1}	Output Low Voltage (except P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			0.45	V	I_{OL} = 1.6 mA
V_{OL2}	Output Low Voltage (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			0.45	V	I_{OL} = 3.2 mA
V_{OH1}	Output High Voltage (P1, P2, P3, P4 and P5)	$V_{DD} - 0.7$			V	I_{OH} = -30 µA
V_{OH2}	Output High Voltage (P0, P2 address mode, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT, D+, D-)	$V_{DD} - 0.7$			V	I_{OH} = -3.2 mA
I_{IL}	Logical 0 Input Current (P1, P2, P3, P4 and P5)			-50	µA	V_{IN} = 0.45V

Table 34. Digital DC Characteristics V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
I_{LI}	Input Leakage Current (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			10	µA	$0.45 < V_{IN} < V_{DD}$
I_{TL}	Logic1 to 0 Transition Current (P1, P2, P3, P4 and P5)			-650	µA	Vin = 2.0V
R_{RST}	Pull-down Resistor	50	90	200	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
V_{RET}	V_{DD} Data Retention Limit			1.8	V	
I_{DD}	Operating Current		TBD	TBD	mA	12 MHz, V_{DD} < 3.3V 16 MHz, V_{DD} < 3.3V 20 MHz, V_{DD} < 3.3V
I_{DL}	Idle Mode Current		TBD	TBD	mA	12 MHz, V_{DD} < 3.3V 16 MHz, V_{DD} < 3.3V 20 MHz, V_{DD} < 3.3V
I_{PD}	Power-down Current		TBD	TBD	µA	$V_{RET} < V_{DD} < 3.3V$

Note: 1. Typical values are obtained using V_{DD} = 3V and T_A = 25°C. They are not tested and there is no guarantee on these values.

Figure 8. I_{DD}/I_{DL} Versus X_{TAL} Frequency; V_{DD} = 2.7 to 3.3V



I_{DD}, I_{DL} and I_{PD} Test Conditions

Figure 9. I_{DD} Test Condition, Active Mode

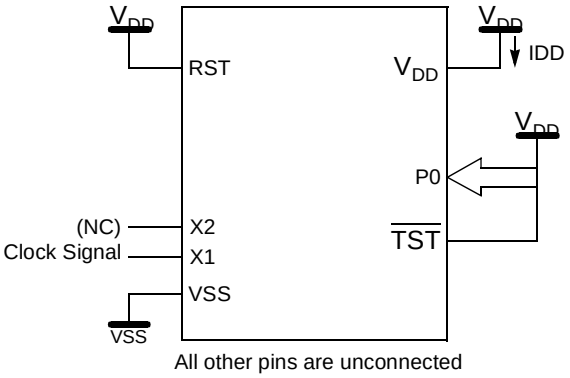


Figure 10. I_{DL} Test Condition, Idle Mode

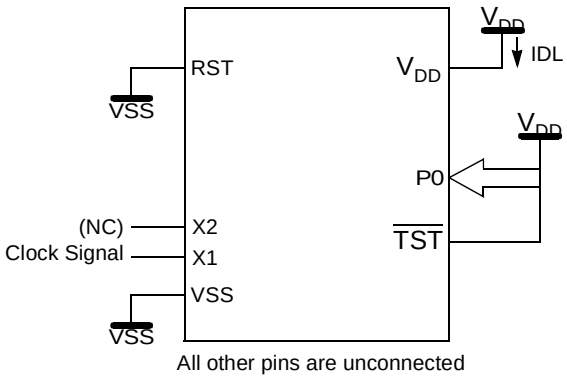
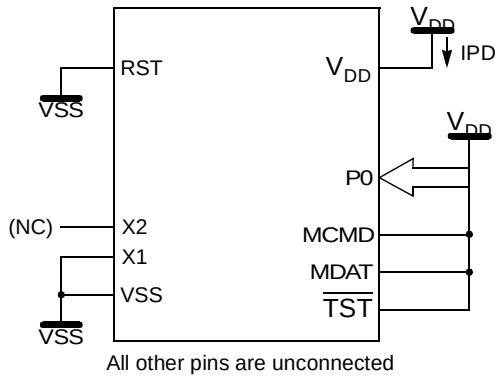


Figure 11. I_{PD} Test Condition, Power-Down Mode



A-to-D Converter

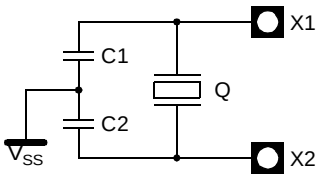
Table 35. A-to-D Converter DC Characteristics V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
AV_{DD}	Analog Supply Voltage	2.7		3.3	V	
AI_{DD}	Analog Operating Supply Current			600	µA	A V_{DD} = 3.3V AIN1:0 = 0 to AV_{DD}
AI_{PD}	Analog Standby Current			2	µA	A V_{DD} = 3.3V ADEN = 0 or PD = 1
AV_{IN}	Analog Input Voltage	AV_{SS}		AV_{DD}	V	
AV_{REF}	Reference Voltage A_{REFN} A_{REFP}	 AV_{SS} 2.4		 AV_{DD}	 V V	
R_{REF}	AREF Input Resistance	10		30	kΩ	T_A = 25°C
C_{IA}	Analog Input capacitance			10	pF	T_A = 25°C

Oscillator and Crystal

Schematic

Figure 12. Crystal Connection



Note: For operation with most standard crystals, no external components are needed on X1 and X2. It may be necessary to add external capacitors on X1 and X2 to ground in special cases (max 10 pF). X1 and X2 may not be used to drive other circuits.

Parameters

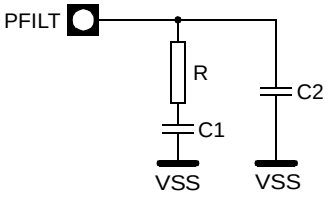
Table 36. Oscillator and Crystal Characteristics V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
C_{X1}	Internal Capacitance (X1 - VSS)		10		pF
C_{X2}	Internal Capacitance (X2 - VSS)		10		pF
C_L	Equivalent Load Capacitance (X1 - X2)		5		pF
DL	Drive Level			50	µW
F	Crystal Frequency			20	MHz
RS	Crystal Series Resistance			40	Ω
CS	Crystal Shunt Capacitance			6	pF

Phase Lock Loop

Schematic

Figure 13. PLL Filter Connection



Parameters

Table 37. PLL Filter Characteristics

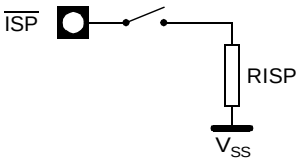
V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R	Filter Resistor		100		Ω
C1	Filter Capacitance 1		10		nF
C2	Filter Capacitance 2		2.2		nF

In-System Programming

Schematic

Figure 14. ISP Pull-down Connection



Parameters

Table 38. ISP Pull-Down Characteristics V_{DD} = 2.7 to 3.3V , T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R_{ISP}	ISP Pull-down Resistor		2.2		kΩ

AC Characteristics

External 8-bit Bus Cycles

Definition of Symbols

Table 39. External 8-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	$\overline{RD}$
W	$\overline{WR}$

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Test conditions: capacitive load on all pins = 50 pF.

Table 40. External 8-bit Bus Cycle – Data Read AC Timings

V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

		Variable Clock Standard Mode		Variable Clock X2 Mode		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}-15$		$T_{CLCL}-15$		ns
T_{AVLL}	Address Valid to ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLAX}	Address Hold after ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLRL}	ALE Low to $\overline{RD}$ Low	$3 \cdot T_{CLCL}-30$		$1.5 \cdot T_{CLCL}-30$		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{RHLH}	$\overline{RD}$ High to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}-65$		$4.5 \cdot T_{CLCL}-65$	ns
T_{AVRL}	Address Valid to $\overline{RD}$ Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data		$5 \cdot T_{CLCL}-30$		$2.5 \cdot T_{CLCL}-30$	ns
T_{RLAZ}	$\overline{RD}$ Low to address Float		0		0	ns
T_{RHDX}	Data Hold After $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Instruction Float after $\overline{RD}$ High		$2 \cdot T_{CLCL}-25$		$T_{CLCL}-25$	ns

Table 41. External 8-bit Bus Cycle – Data Write AC Timings

V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address Hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}$-20		$3.5 \cdot T_{CLCL}$-20		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{CLCL}-15		$0.5 \cdot T_{CLCL}$-15		ns

Waveforms

Figure 15. External 8-bit Bus Cycle – Data Read Waveforms

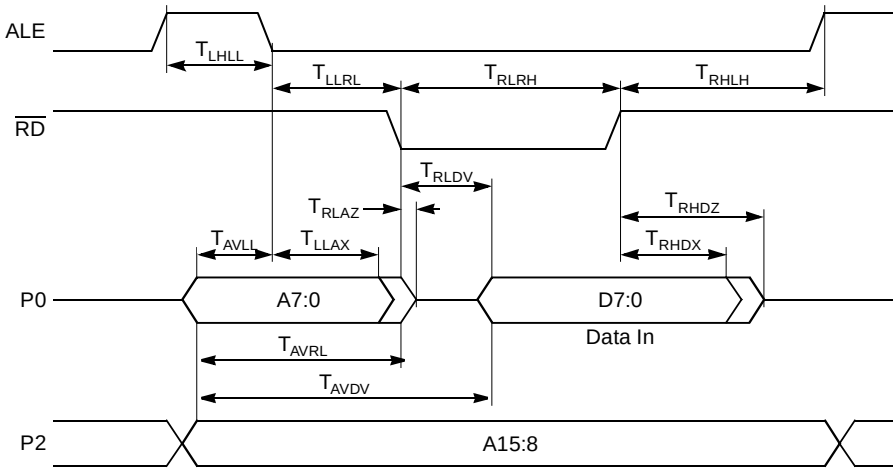
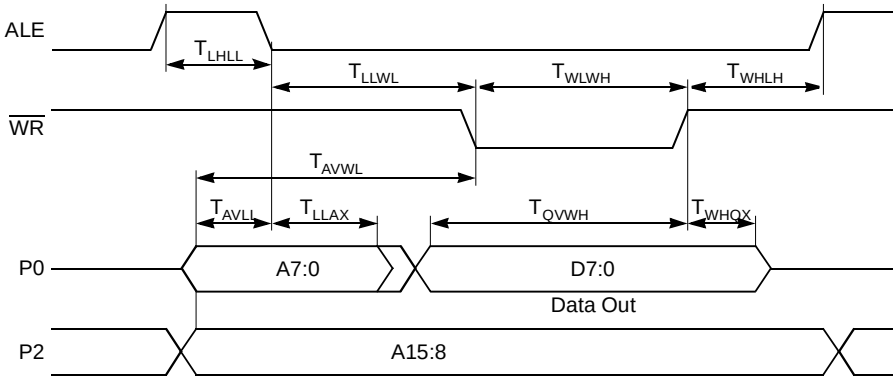


Figure 16. External 8-bit Bus Cycle – Data Write Waveforms



External IDE 16-bit Bus Cycles

Definition of Symbols

Table 42. External IDE 16-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	$\overline{RD}$
W	$\overline{WR}$

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Test conditions: capacitive load on all pins = 50 pF.

Table 43. External IDE 16-bit Bus Cycle – Data Read AC Timings

V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address Hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLRL}	ALE Low to $\overline{RD}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{RHLH}	$\overline{RD}$ High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}$-65		$4.5 \cdot T_{CLCL}$-65	ns
T_{AVRL}	Address Valid to $\overline{RD}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data		$5 \cdot T_{CLCL}$-30		$2.5 \cdot T_{CLCL}$-30	ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Instruction Float after $\overline{RD}$ High		$2 \cdot T_{CLCL}$-25		T_{CLCL}-25	ns

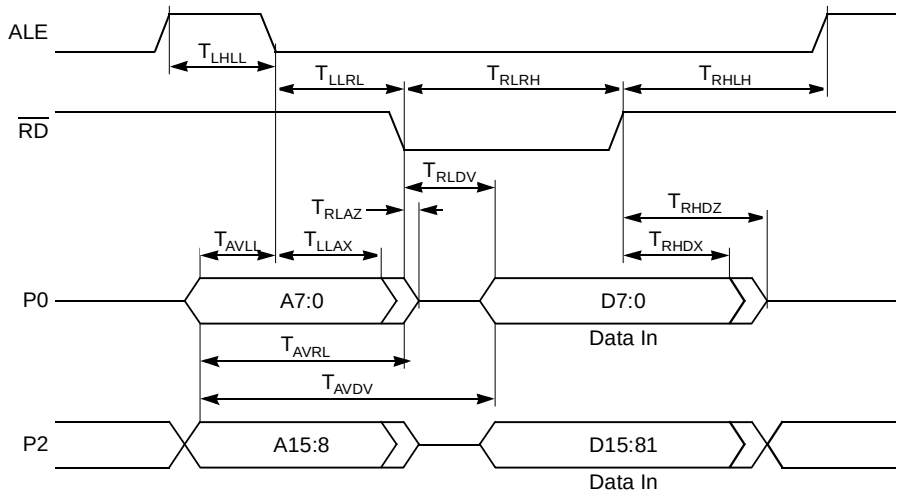
Table 44. External IDE 16-bit Bus Cycle – Data Write AC Timings

V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address Hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}$-20		$3.5 \cdot T_{CLCL}$-20		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{CLCL}-15		$0.5 \cdot T_{CLCL}$-15		ns

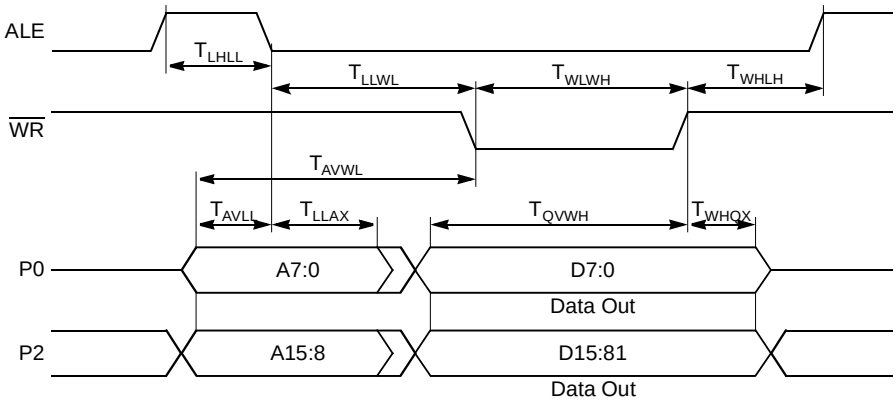
Waveforms

Figure 17. External IDE 16-bit Bus Cycle – Data Read Waveforms



Note: D15:8 is written in DAT16H SFR.

Figure 18. External IDE 16-bit Bus Cycle – Data Write Waveforms



Note: D15:8 is the content of DAT16H SFR.

SPI Interface

Definition of Symbols

Table 45. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Table 46. SPI Interface Master AC Timing[2]

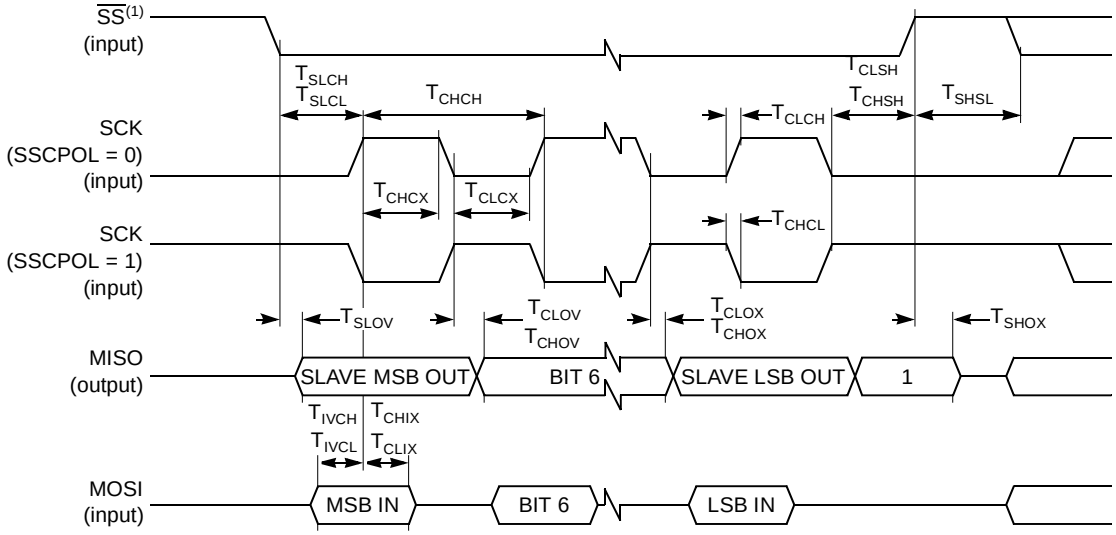
V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	$\overline{SS}$ Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	$\overline{SS}$ High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	$\overline{SS}$ Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after $\overline{SS}$ High		130	ns
T_{SHSL}	$\overline{SS}$ High to $\overline{SS}$ Low	Note[1]		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise Time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise Time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

Notes: 1. Value of this parameter depends on software.
2. Test conditions: capacitive load on all pins = 100 pF

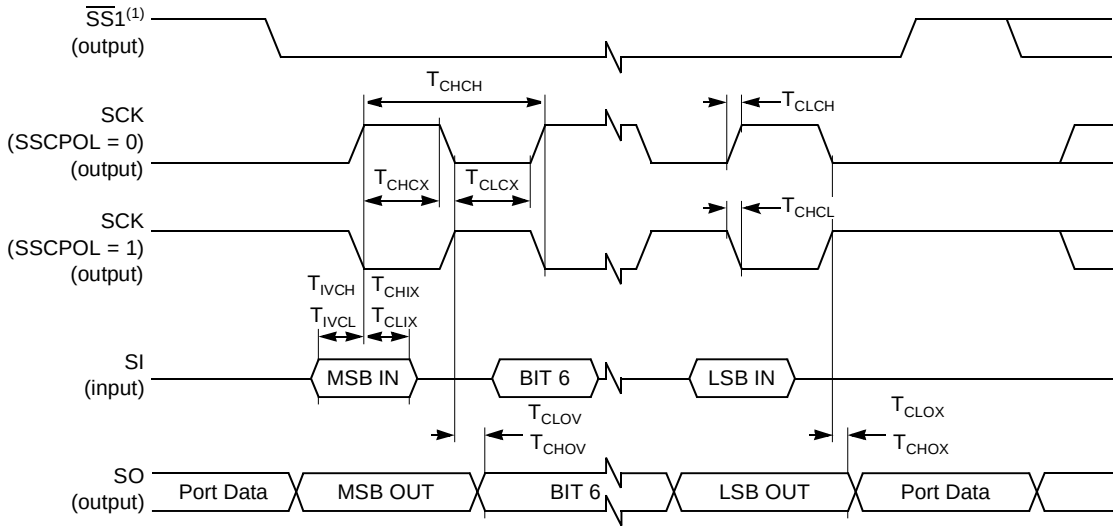
Waveforms

Figure 19. SPI Slave Waveforms (SSCPHA = 0)



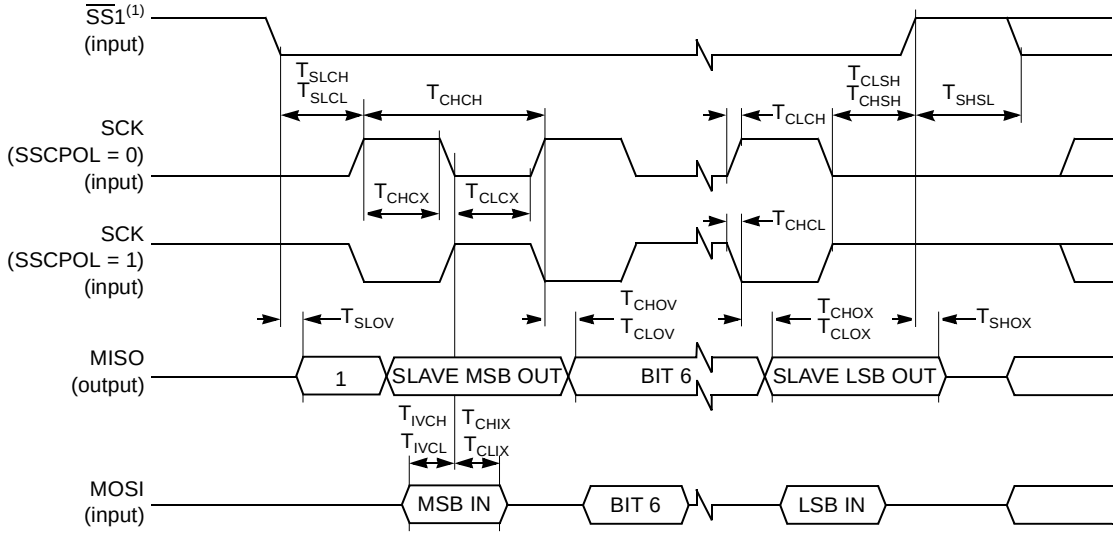
Note: 1. Not Defined but generally the MSB of the character, which has just been received.

Figure 20. SPI Slave Waveforms (SSCPHA = 1)



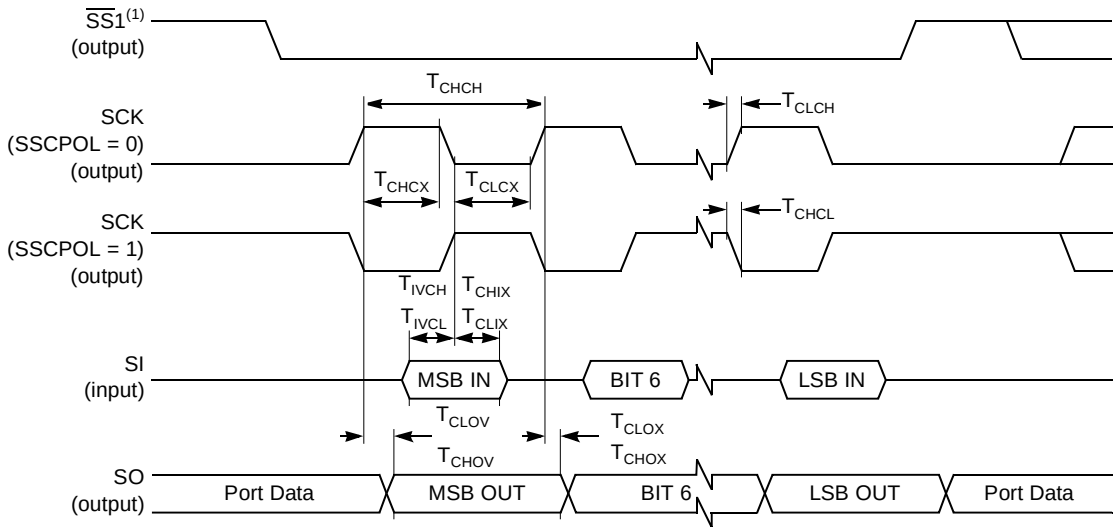
Note: 1. Not Defined but generally the LSB of the character, which has just been received.

Figure 21. SPI Master Waveforms (SSCPHA = 0)



Note: $\overline{SS}$ handled by software using general purpose port pin.

Figure 22. SPI Master Waveforms (SSCPHA = 1)



Note: $\overline{SS}$ handled by software using general purpose port pin.

Two-wire Interface

Timings

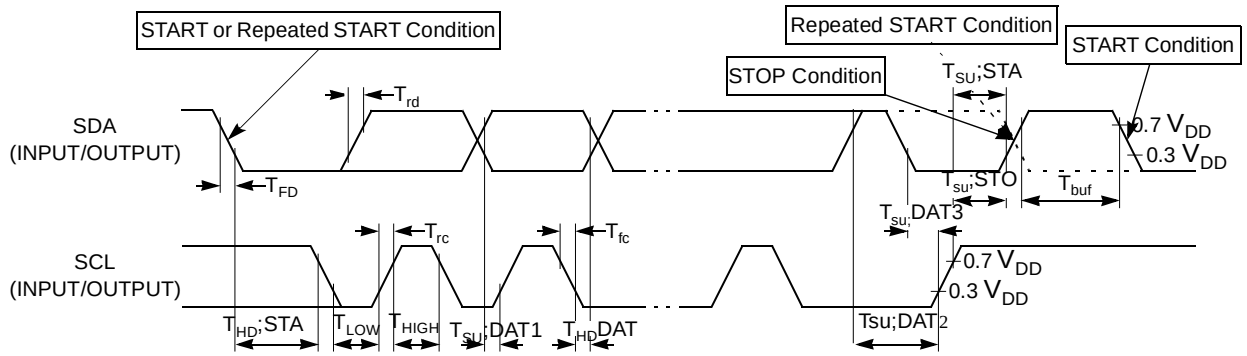
Table 47. TWI Interface AC Timing
zV_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	INPUT Min Max	OUTPUT Min Max
T_{HD}; STA	Start condition hold time	$14 \cdot T_{CLCL}$ (4)	4.0 µs(1)
T_{LOW}	SCL Low Time	$16 \cdot T_{CLCL}$ (4)	4.7 µs(1)
T_{HIGH}	SCL High Time	$14 \cdot T_{CLCL}$ (4)	4.0 µs(1)
T_{RC}	SCL Rise Time	1 µs	Note(2)
T_{FC}	SCL Fall Time	0.3 µs	0.3 µs(3)
T_{SU}; DAT1	Data Set-up Time	250 ns	$20 \cdot T_{CLCL}$ (4)- T_{RD}
T_{SU}; DAT2	SDA Set-up Time (before repeated START condition)	250 ns	1 µs(1)
T_{SU}; DAT3	SDA Set-up Time (before STOP condition)	250 ns	$8 \cdot T_{CLCL}$ (4)
T_{HD}; DAT	Data Hold Time	0 ns	$8 \cdot T_{CLCL}$ (4) - T_{FC}
T_{SU}; STA	Repeated START Set-up Time	$14 \cdot T_{CLCL}$ (4)	4.7 µs(1)
T_{SU}; STO	STOP condition Set-up Time	$14 \cdot T_{CLCL}$ (4)	4.0 µs(1)
T_{BUF}	Bus Free Time	$14 \cdot T_{CLCL}$ (4)	4.7 µs(1)
T_{RD}	SDA Rise Time	1 µs	-(2)
T_{FD}	SDA Fall Time	0.3 µs	0.3 µs(3)

Notes:
1. At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-up resistor, this must be < 1 µs.
3. Spikes on the SDA and SCL lines with a duration of less than $3 \cdot T_{CLCL}$ will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400 pF.
4. $T_{CLCL} = T_{OSC}$ = one oscillator clock period.

Waveforms

Figure 23. TWI Waveforms



MMC Interface

Definition of Symbols

Table 48. MMC Interface Timing Symbol Definitions

Signals	
C	Clock
D	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

Timings

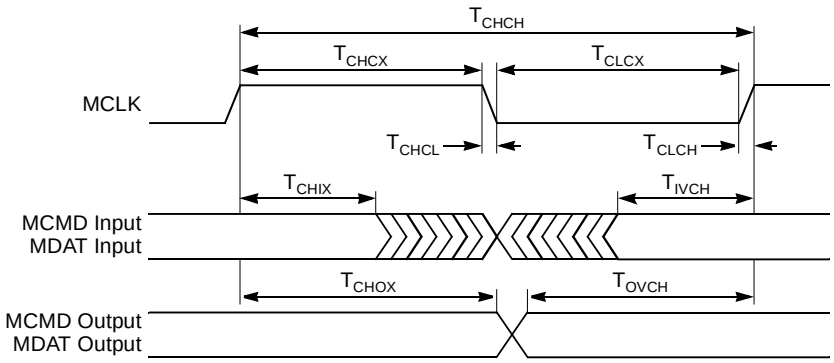
Table 49. MMC Interface AC Timings

V_{DD} = 2.7 to 3.3V, T_A = 0 to 70°C, CL ≤ 100 pF (10 Cards)

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period	50		ns
T_{CHCX}	Clock High Time	10		ns
T_{CLCX}	Clock Low Time	10		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{DVCH}	Input Data Valid to Clock High	3		ns
T_{CHDX}	Input Data Hold after Clock High	3		ns
T_{CHOX}	Output Data Hold after Clock High	5		ns
T_{OVCH}	Output Data Valid to Clock High	5		ns

Waveforms

Figure 24. MMC Input-Output Waveforms



Audio Interface

Definition of Symbols

Table 50. Audio Interface Timing Symbol Definitions

Signals	
C	Clock
O	Data Out
S	Data Select

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

Timings

Table 51. Audio Interface AC Timings

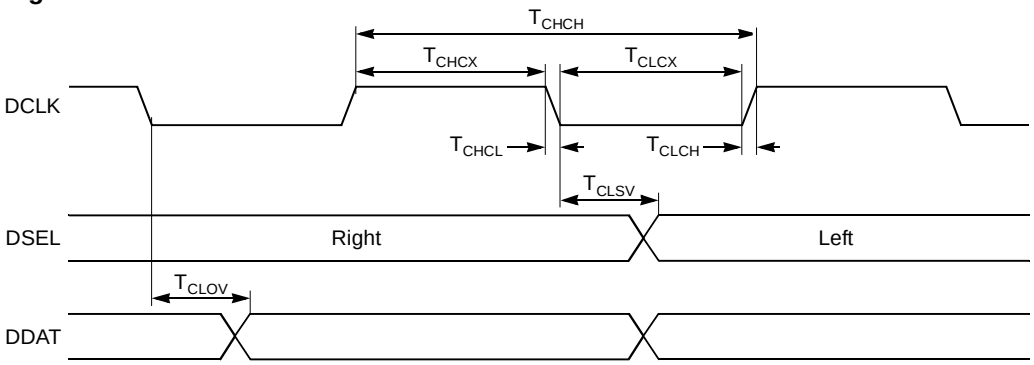
V_{DD} = 2.7 to 3.3V, T_A = 0 to 70°C, CL ≤ 30pF

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period		325.5(1)	ns
T_{CHCX}	Clock High Time	30		ns
T_{CLCX}	Clock Low Time	30		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{CLSV}	Clock Low to Select Valid		10	ns
T_{CLOV}	Clock Low to Data Valid		10	ns

Note: 32-bit format with Fs = 48 kHz.

Waveforms

Figure 25. Audio Interface Waveforms



Analog to Digital Converter

Definition of Symbols

Table 52. Analog to Digital Converter Timing Symbol Definitions

Signals	
C	Clock
E	Enable (ADEN bit)
S	Start Conversion (ADSST bit)

Conditions	
H	High
L	Low

Characteristics

Table 53. Analog-to-Digital Converter AC Characteristics

V_{DD} = 2.7 to 3.3V, T_A = 0 to 70°C

Symbol	Parameter	Min	Max	Unit
T_{CLCL}	Clock Period	1.43		µs
T_{EHSH}	Start-up Time		4	µs
T_{SHSL}	Conversion Time		$11 \cdot T_{CLCL}$	µs
D_{LE}	Differential non-linearity error(1)(2)		TBD	LSB
I_{LE}	Integral non-linearity error(1)(3)		TBD	LSB
O_{SE}	Offset error(1)(4)		TBD	LSB
G_E	Gain error(1)(5)		TBD	%

Notes:
1. AV_{DD} = AV_{REFP} = 3.0 V, AV_{SS} = AV_{REFN} = 0 V. ADC is monotonic with no missing code.
2. The differential non-linearity is the difference between the actual step width and the ideal step width (see Figure 27).
3. The integral non-linearity is the peak difference between the center of the actual step and the ideal transfer curve after appropriate adjustment of gain and offset errors (see Figure 27).
4. The offset error is the absolute difference between the straight line, which fits the actual transfer curve (after removing of gain error); and the straight line, which fits the ideal transfer curve (see Figure 27).
5. The gain error is the relative difference in percent between the straight line which fits the actual transfer curve (after removing of offset error); and the straight line, which fits the ideal transfer curve (see Figure 27).

Waveforms

Figure 26. Analog-to-Digital Converter Internal Waveforms

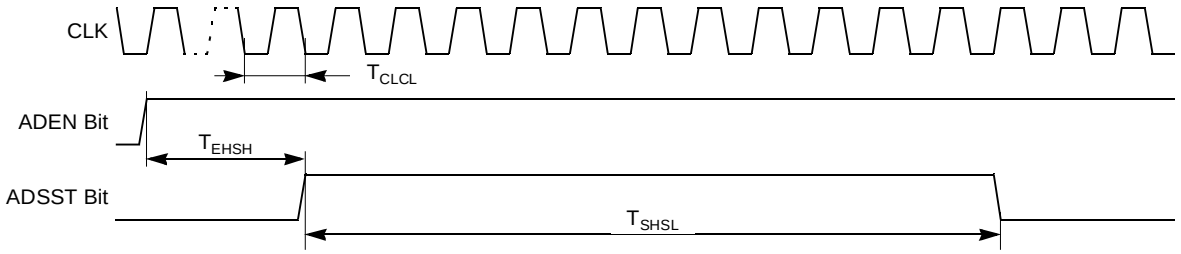
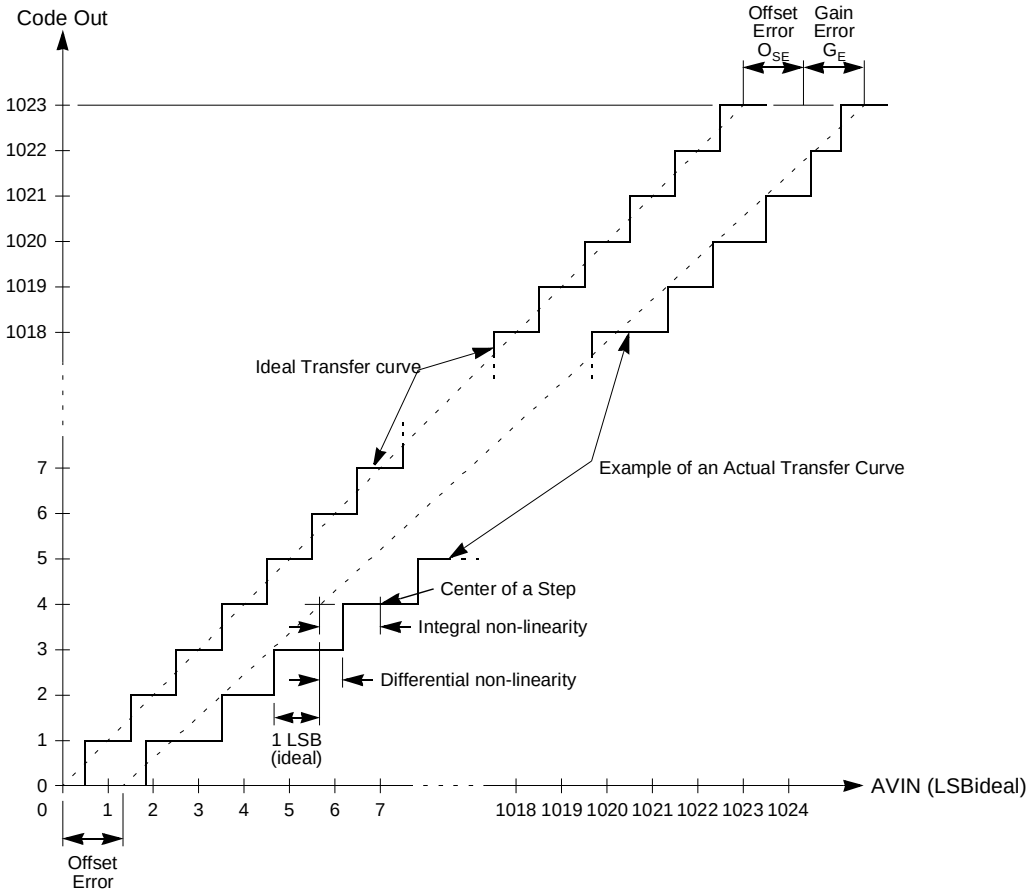


Figure 27. Analog to Digital Converter Characteristics



Flash Memory

Definition of Symbols

Table 54. Flash Memory Timing Symbol Definitions

Signals	
S	$\overline{ISP}$
R	RST
B	FBUSY flag

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

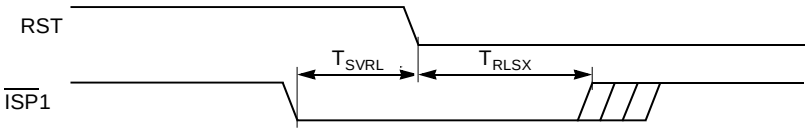
Table 55. Flash Memory AC Timing

V_{DD} = 2.7 to 3.3V, T_A = -40° to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
T_{SVRL}	Input $\overline{ISP}$ Valid to RST Edge	50			ns
T_{RLSX}	Input $\overline{ISP}$ Hold after RST Edge	50			ns
T_{BHBL}	Flash Internal Busy (Programming) Time		10		ms

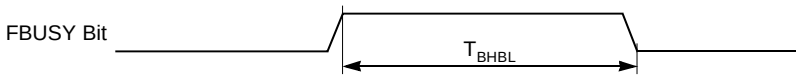
Waveforms

Figure 28. Flash Memory – ISP Waveforms



Note: $\overline{ISP}$ must be driven through a pull-down resistor (see Section “In-System Programming”, page 28).

Figure 29. Flash Memory – Internal Busy Waveforms



External Clock Drive and Logic Level References

Definition of Symbols

Table 56. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

Timings

Table 57. External Clock AC Timings

V_{DD} = 2.7 to 3.3V, T_A= 0 to 70°C

Symbol	Parameter	Min	Max	Unit
T_{CLCL}	Clock Period	50		ns
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns
T_{CR}	Cyclic Ratio in X2 mode	40	60	%

Waveforms

Figure 30. External Clock Waveform

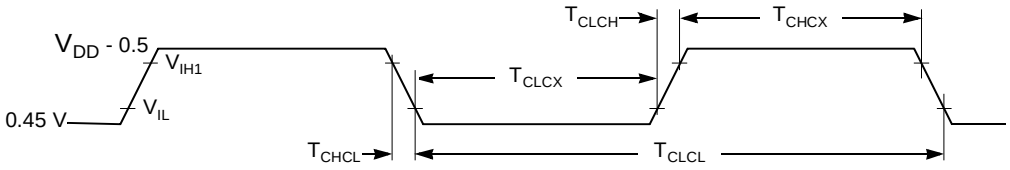
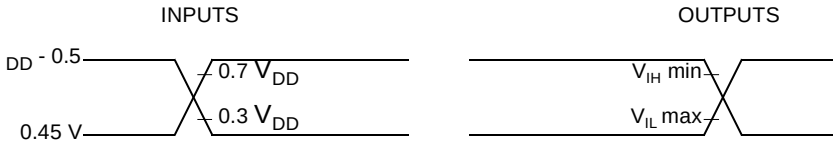
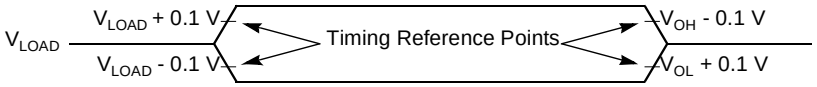


Figure 31. AC Testing Input/Output Waveforms



Notes: 1. During AC testing, all inputs are driven at V_{DD} -0.5V for a logic 1 and 0.45V for a logic 0.
2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 32. Float Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm 20$ mA.

Ordering Information

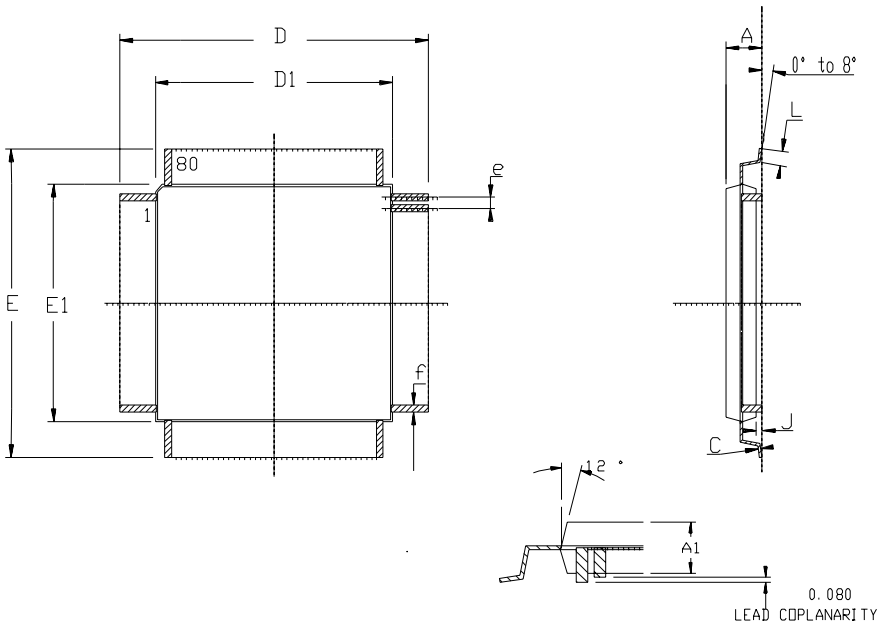
Table 58. Ordering Information

Part Number	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package[2]	Packing
AT89C51SND1C-ROTIL	64K Flash	3V	Industrial	40 MHz	TQFP80	Tray
AT83SND1Axxx[1]-ROTIL	64K ROM	3V	Industrial	40 MHz	TQFP80	Tray

Notes: 1. Refers to ROM code.
2. PLCC84 package only available for development board.

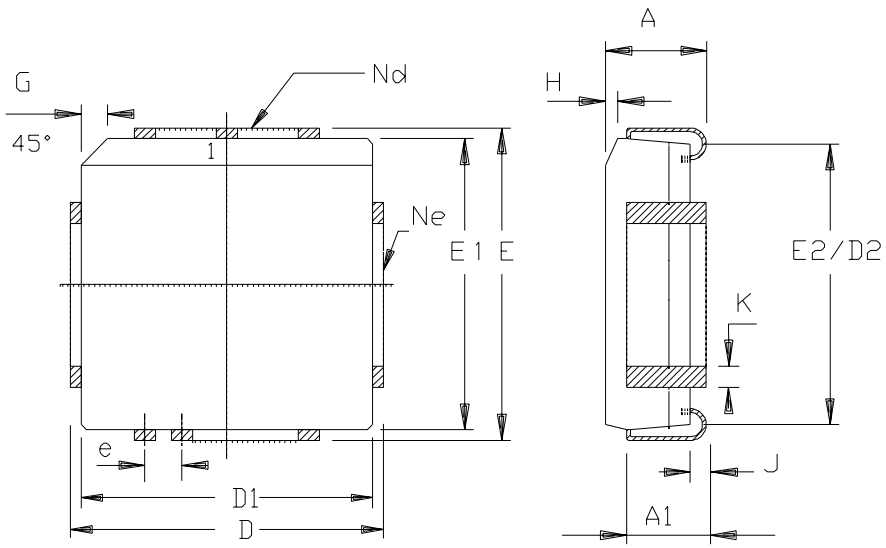
Package Information

TQFP80



	MM		INCH	
	Min	Max	Min	Max
A	1.40	1.60	.055	.063
A1	1.35	1.45	.053	.057
C	0.17 BSC		.007 BSC	
D	15.80	16.20	.622	.638
D1	13.90	14.10	.547	.555
E	15.80	16.20	.622	.638
E1	13.90	14.10	.547	.555
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.65 BSC		.0256 BSC	
f	0.30 BSC		.012 BSC	

PLCC84



	MM		INCH	
A	4.20	5.08	.165	.200
A1	2.29	3.30	.090	.130
D	30.10	30.35	1.185	1.195
D1	29.21	29.41	1.150	1.158
D2	27.69	28.70	1.090	1.130
E	30.10	30.35	1.185	1.195
E1	29.21	29.41	1.150	1.158
E2	27.69	28.70	1.090	1.130
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	–	.020	–
K	0.33	0.53	.013	.021
Nd	21		21	
Ne	21		21	
PKG STD	00			

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