



Lower Power 3.3V CMOS Fast SRAM 256K (32K x 8-Bit)

IDT71V256SA

Features

- ♦ Ideal for high-performance processor secondary cache
- ♦ Commercial (0°C to +70°C) and Industrial (-40°C to +85°C) temperature range options
- ♦ Fast access times:
 - Commercial and Industrial: 10/12/15/20ns
- ♦ Low standby current (maximum):
 - 2mA full standby
- ♦ Small packages for space-efficient layouts:
 - 28-pin 300 mil SOJ
 - 28-pin TSOP Type I
- ♦ Produced with advanced high-performance CMOS technology
- ♦ Inputs and outputs are LVTTL-compatible
- ♦ Single 3.3V(±0.3V) power supply

Description

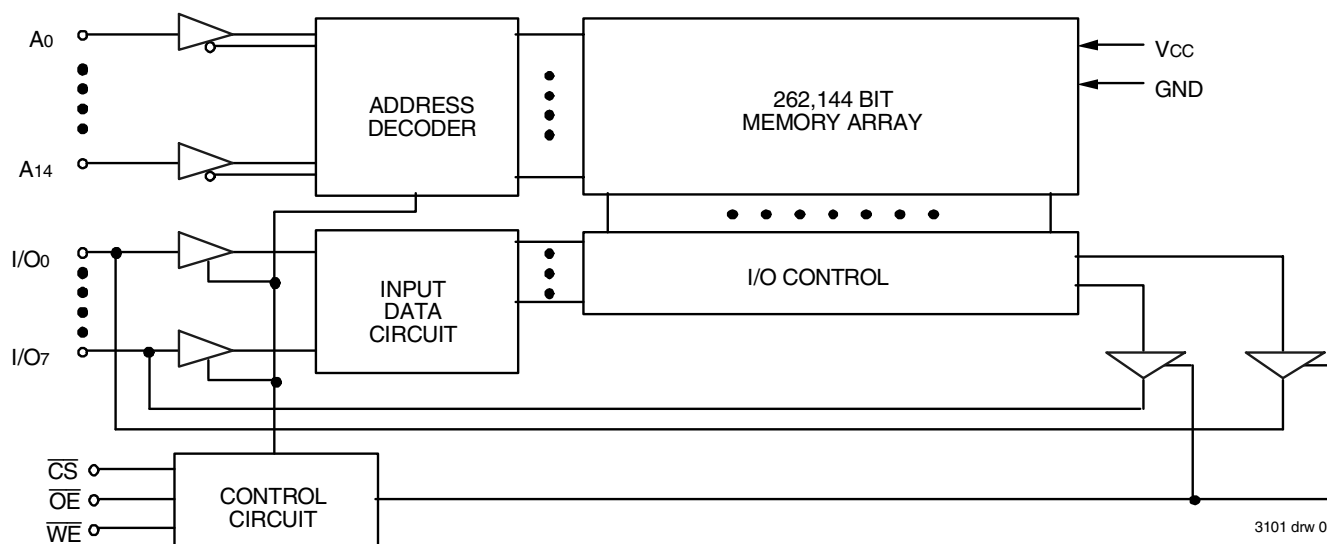
The IDT71V256SA is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

The IDT71V256SA has outstanding low power characteristics while at the same time maintaining very high performance. Address access times of as fast as 10ns are ideal for 3.3V secondary cache in 3.3V desktop designs.

When power management logic puts the IDT71V256SA in standby mode, its very low power characteristics contribute to extended battery life. By taking $\overline{CS}$ HIGH, the SRAM will automatically go to a low power standby mode and will remain in standby as long as $\overline{CS}$ remains HIGH. Furthermore, under full standby mode ($\overline{CS}$ at CMOS level, $f=0$), power consumption is guaranteed to always be less than 6.6mW and typically will be much smaller.

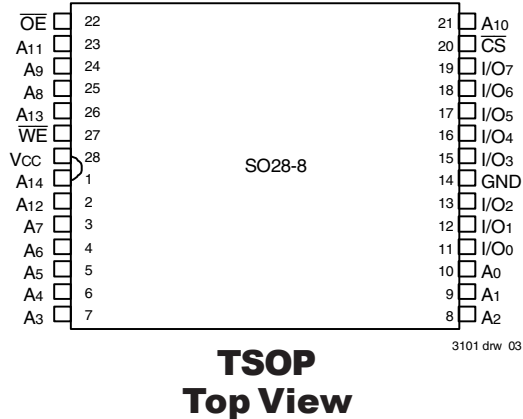
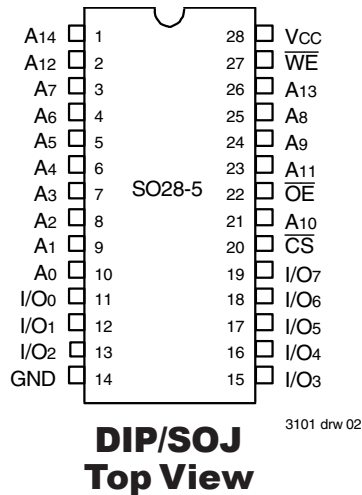
The IDT71V256SA is packaged in a 28-pin 300 mil SOJ and a 28-pin 300 mil TSOP Type I.

Functional Block Diagram



JANUARY 2004

Pin Configurations



Pin Descriptions

Name	Description
A ₀ - A ₁₄	Addresses
I/O ₀ - I/O ₇	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V _{CC}	Power

3101 tbl 01

Truth Table⁽¹⁾

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (Isb)
X	V _{HC}	X	High-Z	Standby (Isb1)
H	L	H	High-Z	Output Disable
H	L	L	DOUT	Read
L	L	X	DIN	Write

3101 tbl 02

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't Care

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l.	Unit
V _{CC}	Supply Voltage Relative to GND	-0.5 to +4.6	V
V _{TERM} ⁽²⁾	Terminal Voltage Relative to GND	-0.5 to V _{CC} +0.5	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	50	mA

3101 tbl 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input, Output, and I/O terminals; 4.6V maximum.

Capacitance

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 3dV	7	pF

3101 tbl 04

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	V _{CC}
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

3101 tbl 05

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage - Inputs	2.0	—	5.0	V
V _{IH}	Input High Voltage - I/O	2.0	—	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

3101 tbl 06

NOTE:

1. V_{IL} (min.) = -2.0V for pulse width less than 5ns, once per cycle.

DC Electrical Characteristics⁽¹⁾

(V_{CC} = 3.3V ± 0.3V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V, Commercial and Industrial Temperture Ranges)

Symbol	Parameter	71V256SA10	71V256SA12	71V256SA15	71V256SA20	Unit
I _{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	100	90	85	85	mA
I _{SB}	Standby Power Supply Current (TTL Level) CS = V _{IH} , V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽²⁾	20	20	20	20	mA
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , V _{CC} = Max., Outputs Open, f = 0 ⁽²⁾ , V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC}	2	2	2	2	mA

3101 tbl 07

NOTES:

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/trc, only address inputs cycling at f_{MAX}; f = 0 means that no inputs are cycling.

DC Electrical Characteristics

(V_{CC} = 3.3V ± 0.3V)

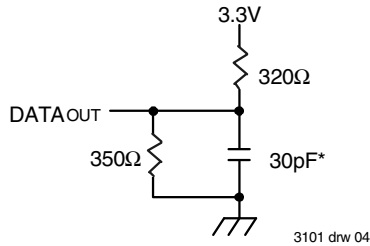
Symbol	Parameter	Test Conditions	IDT71V256SA			Unit
			Min.	Typ.	Max.	
I _{IL}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	—	2	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., $\overline{CS}$ = V _{IH} , V _{OUT} = GND to V _{CC}	—	—	2	μA
V _{OL}	Output Low Voltage	I _{OL} = 8mA, V _{CC} = Min.	—	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA, V _{CC} = Min.	2.4	—	—	V

3101 tbl 08

AC Test Conditions

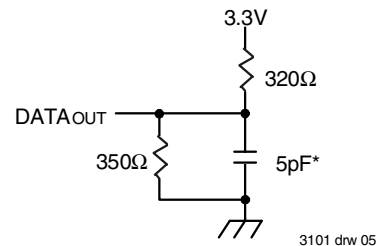
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3101 tbl 09



3101 drw 04

Figure 1. AC Test Load



3101 drw 05

Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

*Includes scope and jig capacitances

AC Electrical Characteristics

(Vcc = 3.3V ± 0.3V, Commercial and Industrial Temperature Ranges)

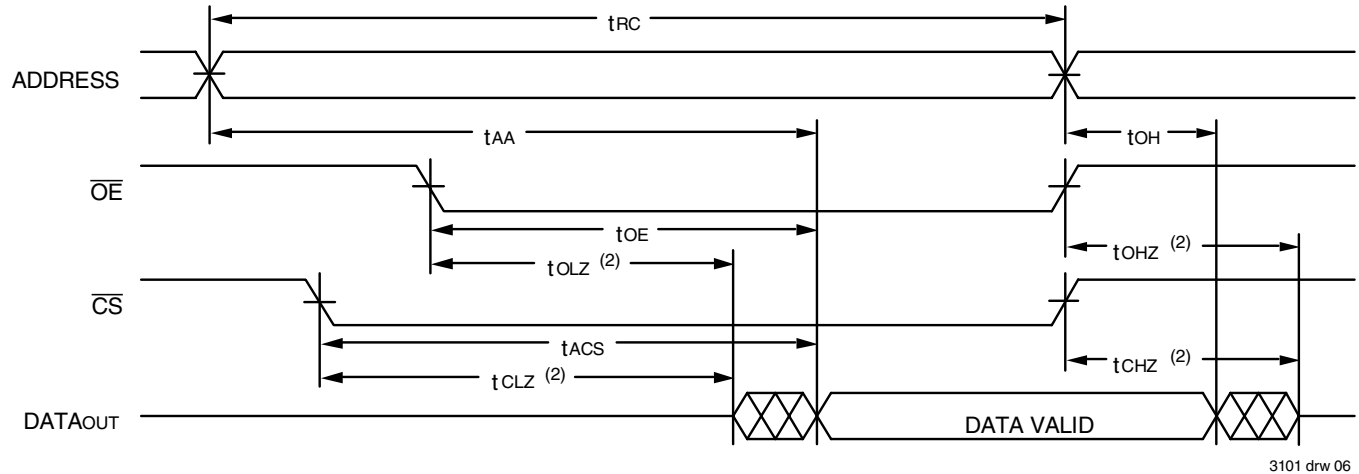
Symbol	Parameter	71V256SA10		71V256SA12		71V256SA15		71V256SA20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t _{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t _{AA}	Address Access Time	—	10	—	12	—	15	—	20	ns
t _{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	20	ns
t _{CLZ} ⁽¹⁾	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t _{CHZ} ⁽¹⁾	Chip Select to Output in High-Z	0	8	0	8	0	9	0	10	ns
t _{OE}	Output Enable to Output Valid	—	6	—	6	—	7	—	8	ns
t _{OLZ} ⁽¹⁾	Output Enable to Output in Low-Z	3	—	3	—	0	—	0	—	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output in High-Z	2	6	2	6	0	7	0	8	ns
t _{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
t _{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t _{AW}	Address Valid to End-of-Write	9	—	9	—	10	—	15	—	ns
t _{CW}	Chip Select to End-of-Write	9	—	9	—	10	—	15	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	9	—	9	—	10	—	15	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t _{DW}	Data to Write Time Overlap	6	—	6	—	7	—	8	—	ns
t _{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t _{OW} ⁽¹⁾	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns
t _{WHZ} ⁽¹⁾	Write Enable to Output in High-Z	1	8	1	8	1	9	1	10	ns

3101 tbl 10

NOTE:

1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1⁽¹⁾

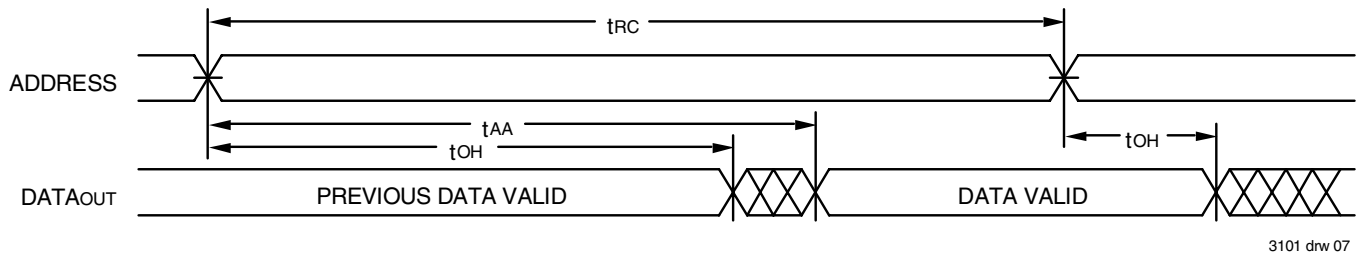


3101 drw 06

NOTES:

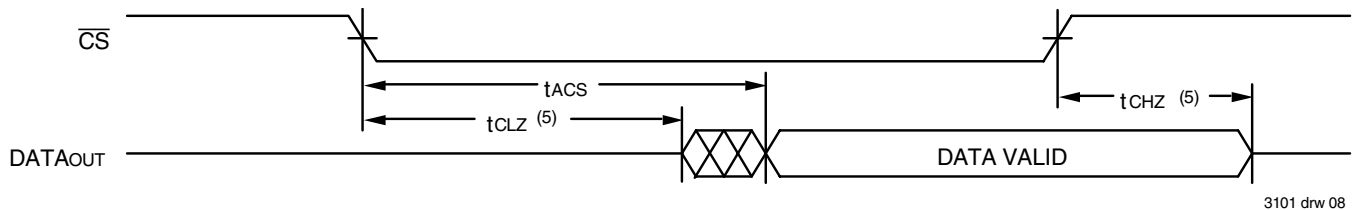
1. $\overline{WE}$ is HIGH for Read cycle.
2. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Read Cycle No. 2^(1,2,4)



3101 drw 07

Timing Waveform of Read Cycle No. 3^(1,3,4)



3101 drw 08

NOTES:

1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

The timing diagram illustrates the sequence of signals for a memory access. The ADDRESS bus is active during the write cycle (tWC). The output enable ($\overline{OE}$) is active during the read cycle (tAW). The chip select ($\overline{CS}$) is active during the write cycle (tAS) and the read cycle (tWP⁽⁶⁾). The write enable ($\overline{WE}$) is active during the write cycle (tWR). The data output (DATAOUT) is valid during the read cycle (tOW⁽⁵⁾) and the data input (DATAIN) is valid during the write cycle (tDW, tDH). The output hold time (tOHZ⁽⁵⁾) is the time after $\overline{OE}$ is deasserted. The output delay (tOW⁽⁵⁾) is the time from the end of the write cycle to the output becoming high-impedance. The data output delay (tOW⁽⁵⁾) is the time from the end of the write cycle to the output becoming high-impedance. The data output delay (tOW⁽⁵⁾) is the time from the end of the write cycle to the output becoming high-impedance.

1. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals must not be applied.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.
6. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{OW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

The diagram illustrates the timing relationships for a memory access. The signals shown are ADDRESS, CS (Chip Select), WE (Write Enable), and DATAIN. The timing parameters are defined as follows:

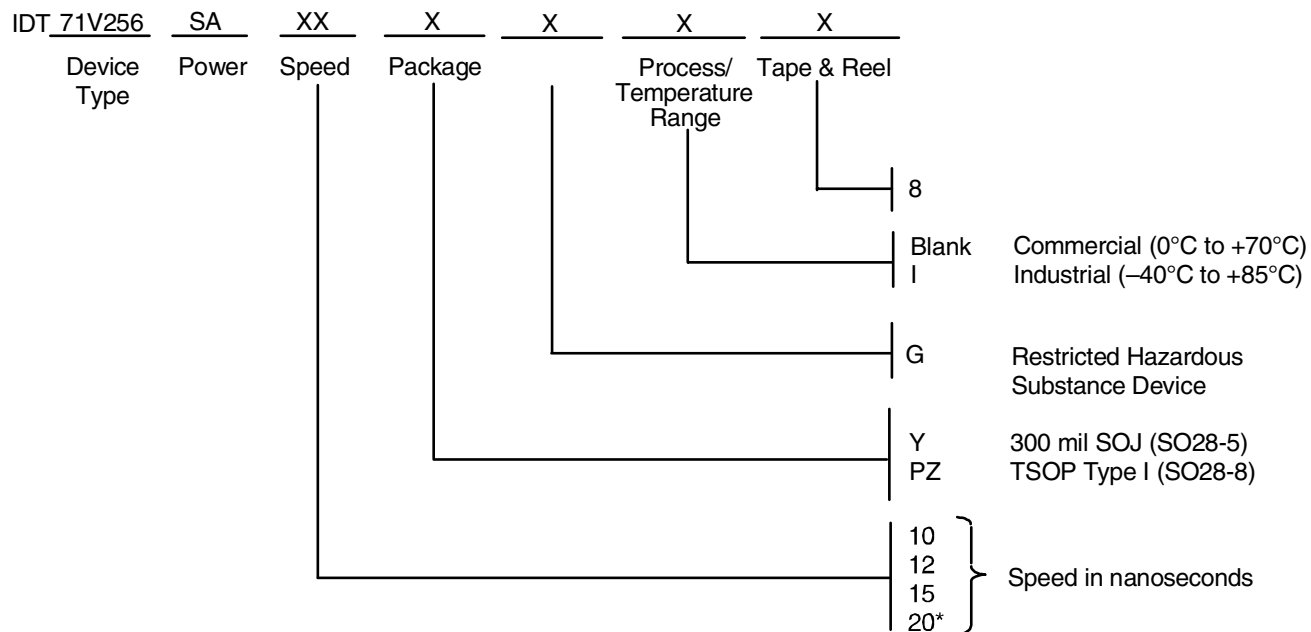
- t_{WC} : Write Cycle time, from the start of the ADDRESS signal to the end of the ADDRESS signal.
- t_{AW} : Address to Write Enable time, from the start of the ADDRESS signal to the start of the WE signal.
- t_{AS} : Address Setup time, from the start of the ADDRESS signal to the start of the CS signal.
- $t_{CW}^{(5)}$: Chip Select to Write Enable time, from the start of the CS signal to the start of the WE signal.
- t_{WR} : Write Enable to Write Cycle time, from the start of the WE signal to the end of the ADDRESS signal.
- t_{DW} : Data Valid time, from the start of the DATAIN signal to the start of the WE signal.
- t_{DH} : Data Hold time, from the end of the WE signal to the end of the DATAIN signal.

The DATAIN signal is shown as a horizontal line with a trapezoidal pulse labeled "DATA VALID" during the t_{DW} and t_{DH} intervals.

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1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{OW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

Ordering Information — Commercial and Industrial



* Available in SOJ package only.

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Datasheet Document History

1/7/00		Updated to new format
	Pg. 1, 3, 4, 7	Expanded Industrial Temperature offerings
	Pg. 1, 2, 7	Removed 28-pin 300 mil plastic DIP package offering
	Pg. 6	Removed Note No. 1 from Write Cycle No. 1 diagram; renumbered notes and footnotes
	Pg. 7	Revised Ordering Information
	Pg. 8	Added Datasheet Document History
08/09/00		Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"
06/21/02	Pg. 7	Added tape and reel option to the ordering information
01/30/04	Pg. 7	Added "restricted hazardous substance device" to order information.



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