DESCRIPTION

The Hynix HY57V641620HG is a 67,108,864-bit CMOS Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY57V641620HG is organized as 4banks of 1,048,576x16.

HY57V641620HG is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or Full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

FEATURES

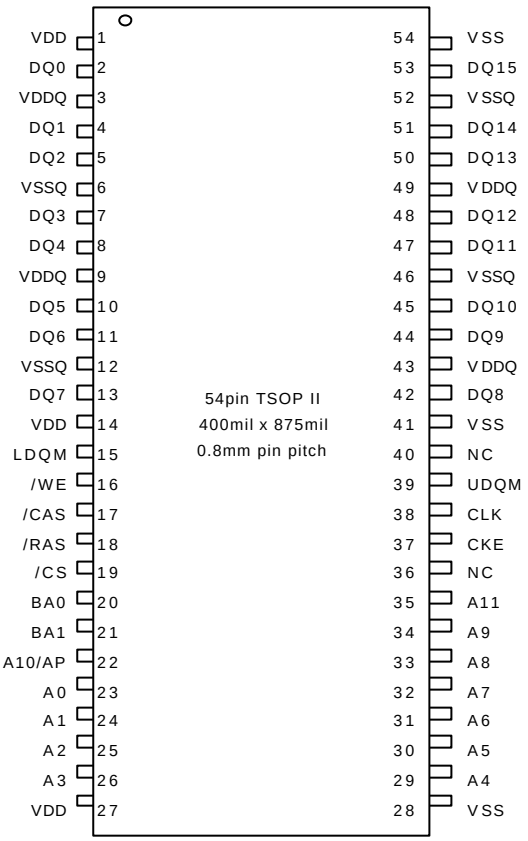
- Single 3.3±0.3V power supply Note)
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 54pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM or LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks

ORDERING INFORMATION

Part No.	Clock Frequency	Power	Organization	Interface	Package
HY57V641620HGT-5/55/6/7	200/183/166/143MHz	Normal	4Banks x 1Mbits x16	LVTTL	400mil 54pin TSOP II
HY57V641620HGT-K	133MHz				
HY57V641620HGT-H	133MHz				
HY57V641620HGT-8	125MHz				
HY57V641620HGT-P	100MHz				
HY57V641620HGT-S	100MHz				
HY57V641620HGLT-5/55/6/7	200/183/166/143MHz	Low power			
HY57V641620HGLT-K	133MHz				
HY57V641620HGLT-H	133MHz				
HY57V641620HGLT-8	125MHz				
HY57V641620HGLT-P	100MHz				
HY57V641620HGLT-S	100MHz				

Note : VDD(Min) of HY57V641620HG(L)T-5/55/6 is 3.135V

PIN CONFIGURATION

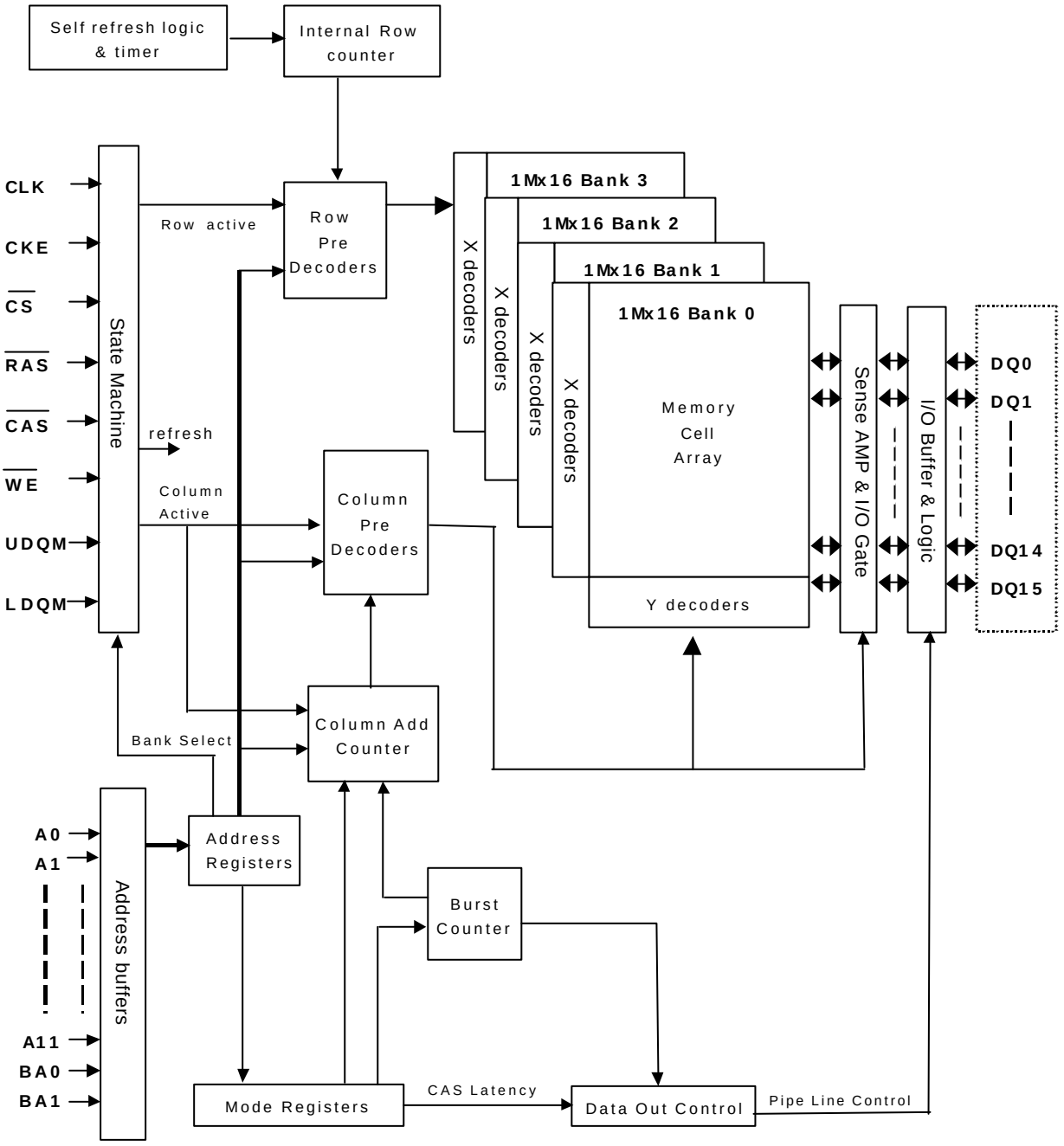


PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0,BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
V_{DD}/V_{SS}	Power Supply/Ground	Power supply for internal circuits and input buffers
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mbit x 4banks x 16 I/O Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITION (T_A=0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	1,2
Input High Voltage	V_{IH}	2.0	3.0	V_{DDQ} + 2.0	V	1,3
Input Low Voltage	V_{IL}	V_{SSQ} - 2.0	0	0.8	V	1,4

Note :

1.All voltages are referenced to V_{SS} = 0V

2.VDD(min) of HY57V641620HG(L)T-5/55/6 is 3.135V

3.V_{IH} (max) is acceptable 5.6V AC pulse width with ≤3ns of duration

4.V_{IL} (min) is acceptable -2.0V AC pulse width with ≤3ns of duration

AC OPERATING CONDITION (T_A=0 to 70°C, V_{DD}=3.3 ± 0.3V[Note2], V_{SS}=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	V_{IH} / V_{IL}	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note :

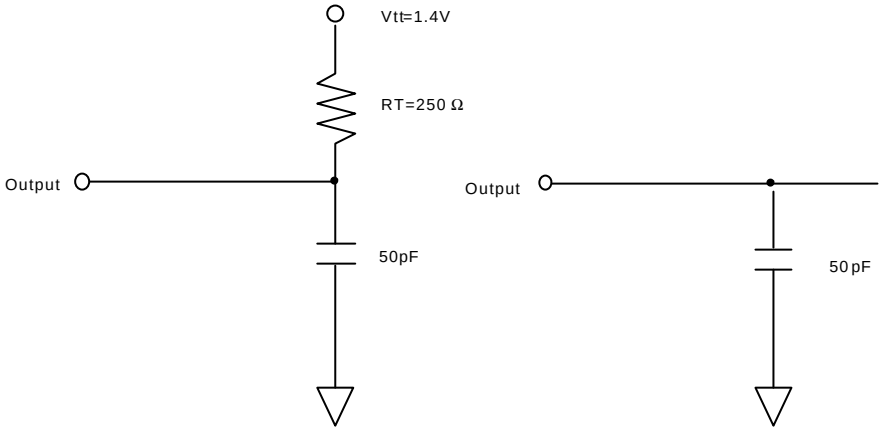
1. Output load to measure access time is equivalent to two TTL gates and one capacitor (50pF)
   For details, refer to AC/DC output circuit

2.VDD(min) of HY57V641620HG(L)T-5/55/6 is 3.135V

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	C_{I1}	2	4	pF
	A0 ~ A11, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, UDQM, LDQM	C_{I2}	2.5	5	pF
Data input / output capacitance	DQ0 ~ DQ15	$C_{I/O}$	2	6.5	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit

AC Output Load Circuit

DC CHARACTERISTICS I (TA=0 to 70°C, V_{DD}=3.3±0.3V[Note3])

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	I_{LI}	-1	1	uA	1
Output Leakage Current	I_{LO}	-1	1	uA	2
Output High Voltage	V_{OH}	2.4	-	V	I_{OH} = -4mA
Output Low Voltage	V_{OL}	-	0.4	V	I_{OL} = +4mA

Note:

1. V_{IN} = 0 to 3.6V, All other pins are not tested under V_{IN} =0V
2. D_{OUT} is disabled, V_{OUT}=0 to 3.6

DC CHARACTERISTICS II (TA=0 to 70°C, VDD=3.3±0.3V[Note5], VSS=0V)

Parameter	Symbol	Test Condition		Speed									Unit	Note
				-5	-55	-6	-7	-K	-H	-8	-P	-S		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA		100	95	90	85	85	85	80	80	80	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = min		2									mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		2									mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		15									mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		12									mA	
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = min		6									mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		5									mA	
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		30									mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		20									mA	
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	CL=3	170	160	150	150	150	150	120	120	120	mA	1
			CL=2	NA	NA	NA	NA	120					mA	
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active		160									mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V		1									mA	3
				400									uA	4

Note :

1.IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open

2.Min. of tRRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II

3.HY57V641620HGT-6/7/K/H/P/S

4.HY57V641620HGLT-6/7/K/H/P/S

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-55		-6		-7		-K		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	CAS Latency = 3	tCK3	55	1000	55	1000	6	1000	7	1000	7.5	1000	7.5	1000	8	1000	10	1000	10	1000	ns	
	CAS Latency = 2	tCK2	10		10		10		10		7.5		10		10		10		12		ns	
Clock high pulse width		tCHW	2.5	-	2.75	-	2.5	-	2.5	-	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
Clock low pulse width		tCLW	2.5	-	2.75	-	2.5	-	2.5	-	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
Access time from clock	CAS Latency = 3	tAC3	-	5.4	-	5.4	-	5.4	-	5.4	-	5.4		5.4	-	6		6	-	6	ns	2
	CAS Latency = 2	tAC2	-	6	-	6	-	6	-	6	-	5.4		6	-	6	-	6	-	8	ns	
Data-out hold time		tOH	2.5	-	2.5	-	2.7	-	2.7	-	2.7	-	2.7	-	3	-	3	-	3	-	ns	
Data-Input setup time		tDS	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Data-Input hold time		tDH	0.8	-	0.8	-	0.8	-	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Address setup time		tAS	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Address hold time		tAH	0.8	-	0.8	-	0.8	-	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
CKE setup time		tCKS	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
CKE hold time		tCKH	0.8	-	0.8	-	0.8	-	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Command setup time		tCS	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Command hold time		tCH	0.8	-	0.8	-	0.8	-	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
CLK to data output in low Z-time		tOLZ	1	-	1	-	1	-	1.5	-	1.5	-	1.5	-	1	-	1	-	2	-	ns	
CLK to data output in high Z-time	CAS Latency = 3	tOHZ3		5.4		5.4		5.4		5.4		5.4		5.4	3	6		6		6	ns	
	CAS Latency = 2	tOHZ2													3	6					ns	

Note :

1. Assume tR / tF (input rise and fall time) is 1ns
2. Access times to be measured with input signals of 1v/ns edge rate

AC CHARACTERISTICS I

Parameter		Symbol	-5		-55		-6		-7		-K		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Mn	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	55	-	55	-	60	-	62	-	65	-	65	-	68	-	70	-	70	-	ns	
	Auto Refresh	tRRC	60	-	60	-	60	-	62	-	65	-	65	-	68	-	70	-	70	-	ns	
$\overline{RAS}$ to$\overline{CAS}$ Delay		tRCD	15	-	16.5	-	18	-	20	-	15	-	20	-	20	-	20	-	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	38.5	100K	38.5	100K	42	100K	42	120K	45	120K	45	120K	48	100K	50	120K	50	120K	ns	
$\overline{RAS}$ Precharge Time		tRP	15	-	16.5	-	18	-	20	-	15	-	20	-	20	-	20	-	20	-	ns	
$\overline{RAS}$ to$\overline{RAS}$ Bank Active Delay		tRRD	10	-	11	-	12	-	14	-	15	-	15	-	16	-	20	-	20	-	ns	
$\overline{CAS}$ to$\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
Data-In to Precharge Command		tDPL	2	-	2	-	2	-	1	-	1	-	1	-	2	-	1	-	1	-	CLK	
Data-In to Active Command		tDAL	5	-	5	-	5	-	4	-	4	-	4	-	5	-	3	-	3	-	CLK	
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	1	-	1	-	1	-	2	-	1	-	1	-	CLK	
Precharge to Data Output Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ 3	3	-	3	-	3	-	3	-	3	-	3	-	3	-	3	-	3	-	CLK	
	$\overline{CAS}$ Latency = 2	tPROZ 2	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Power Down Exit Time		tPDE	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	-	64	-	64	-	64	-	64	-	64	ms	

Note:

1. A new command can be given tRRC after self refresh exit

DEVICE OPERATING OPTION TABLE

HY57V641620HG(L)T-5

	CAS Latency	t RCD	t RAS	t RC	t RP	t AC	tOH
200MHz(5ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.4ns	2.5ns
183MHz(5.5ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.4ns	2.5ns
166MHz(6ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.4ns	2.7ns

HY57V641620HG(L)T-55

	CAS Latency	t RCD	t RAS	t RC	t RP	t AC	tOH
183MHz(5.5ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.4ns	2.5ns
166MHz(6ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.4ns	2.7ns
143MHz(7ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.4ns	2.7ns

HY57V641620HG(L)T-6

	CAS Latency	t RCD	t RAS	t RC	t RP	t AC	tOH
166MHz(6ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.4ns	2.7ns
143MHz(7ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
133MHz(7.5ns)	2CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns

HY57V641620HG(L)T-7

	CAS Latency	t RCD	t RAS	t RC	t RP	t AC	tOH
143MHz(7ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
133MHz(7.5ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

HY57V641620HG(L)T-K

	CAS Latency	t RCD	t RAS	t RC	t RP	t AC	tOH
133MHz(7.5ns)	2CLKs	2CLKs	6CLKs	8CLKs	2CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

HY57V641620HG(L)T-H

	CAS Latency	t RCD	t RAS	t RC	t RP	t AC	tOH
133MHz(7.5ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

HY57V641620HG(L)T-8

	CAS Latency	t RCD	t RAS	t RC	t RP	t AC	tOH
125MHz(8ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	3CLKs	6ns	3ns
83MHz(12ns)	3CLKs	3CLKs	6CLKs	9CLKs	2CLKs	6ns	3ns

HY57V641620HG(L)T-P

	CAS Latency	t RCD	t RAS	t RC	t RP	t AC	tOH
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HY57V641620HG(L)T-S

	CAS Latency	t RCD	t RAS	t RC	t RP	t AC	tOH
100MHz(10ns)	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note :

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation

PACKAGE INFORMATION

400mil 54pin Thin Small Outline Package