

## DDR 14-Bit Registered Buffer

**Recommended Application:**  
DDR Memory Modules

**Product Features:**

- Differential clock signal
- Meets SSTL\_2 signal data
- Supports SSTL\_2 class I & II specifications
- low-voltage operation  
VDD = 2.3V to 2.7V
- 48 pin TSSOP package

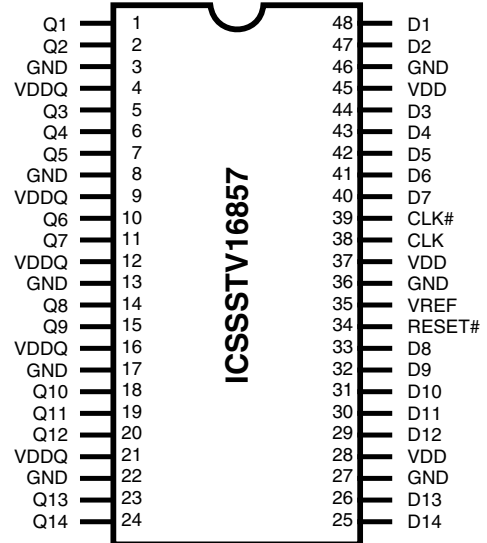
**Truth Table<sup>1</sup>**

Inputs				Q Outputs
RESET#	CLK	CLK#	D	Q
L	X or Floating	X or Floating	X or Floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q <sub>0</sub> <sup>(2)</sup>

**Notes:**

1. H = High Signal Level  
L = Low Signal Level  
↑ = Transition LOW-to-HIGH  
↓ = Transition HIGH -to LOW  
X = Irrelevant
2. Output level before the indicated steady state input conditions were established.

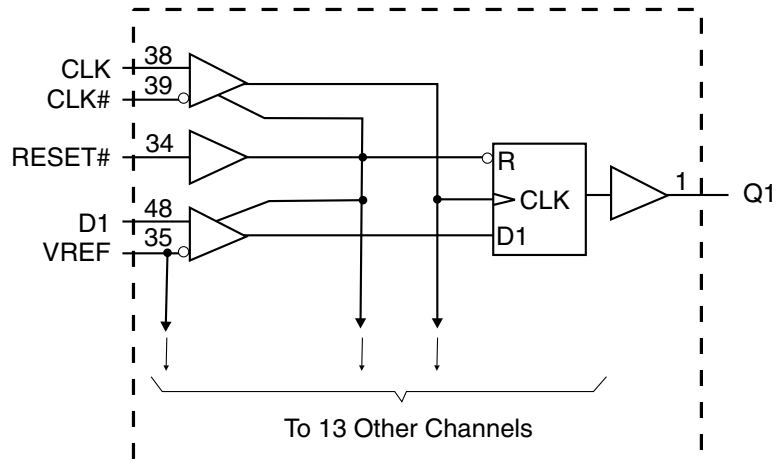
**Pin Configuration**



**48-Pin TSSOP & TVSOP**

6.10 mm. Body, 0.50 mm. pitch = TSSOP  
4.40 mm. Body, 0.40 mm. pitch = TSSOP (TVSOP)

**Block Diagram**





## General Description

The 14-bit ICSSSTV16857 is a universal bus driver designed for 2.3V to 2.7V VDD operation and SSTL\_2 I/O Levels except for the RESET# input which is LVCMOS.

Data flow from D to Q is controlled by the differential clock, CLK, CLK# and RESET#. Data is triggered on the positive edge of CLK. CLK# must be used to maintain noise margins. RESET# must be supported with LVCMOS levels as VREF may not be stable during power-up. RESET# is asynchronous and is intended for power-up only and when low assures that all of the registers reset to the Low State, Q outputs are low, and all input receivers, data and clock are switched off.

## Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
24, 23, 20, 19, 18, 15, 14, 11, 10, 7, 6, 5, 2, 1	Q (14:1)	OUTPUT	Data output
3, 8, 13, 22, 27, 36, 46	GND	PWR	Ground
4, 9, 12, 16, 21	VDDQ	PWR	Output supply voltage
25, 26, 29, 30, 31, 32, 33, 40, 41, 42, 43, 44, 47, 48	D (14:1)	INPUT	Data input
38	CLK	INPUT	Positive clock input
39	CLK#	INPUT	Negative clock input
28, 37, 45	VDD	PWR	Core supply voltage
34	RESET#	INPUT	Reset (active low)
35	VREF	INPUT	Input reference voltage



## Absolute Maximum Ratings

Storage Temperature .....	-65°C to +150°C
Supply Voltage .....	-0.5 to 3.6V
Input Voltage <sup>1</sup> .....	-0.5 to VDD +0.5
Output Voltage <sup>1,2</sup> .....	-0.5 to VDDQ +0.5
Input Clamp Current .....	±50 mA
Output Clamp Current .....	±50mA
Continuous Output Current .....	±50mA
VDD, VDDQ or GND Current/Pin .....	±100mA
Package Thermal Impedance <sup>3</sup> .....	55°C/W

**Notes:**

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level  $V_0 > V_{DDQ}$ .
3. The package thermal impedance is calculated in accordance with JEDEC 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V <sub>DD</sub>	Supply Voltage	2.3	2.5	2.7	V
V <sub>DDQ</sub>	I/O Supply Voltage	2.3	2.5	2.7	
V <sub>REF</sub>	Reference Voltage $V_{REF} = 0.5 \times V_{DDQ}$	1.15	1.25	1.35	
V <sub>TT</sub>	Termination Voltage	V <sub>REF</sub> -0.04	V <sub>REF</sub>	V <sub>REF</sub> -0.04	
V <sub>I</sub>	Input Voltage	0		V <sub>DD</sub>	
V <sub>IH</sub>	DC Input High Voltage	V <sub>REF</sub> +0.15			
V <sub>IH</sub>	AC Input High Voltage				
V <sub>IL</sub>	DC Input Low Voltage				
V <sub>IL</sub>	AC Input Low Voltage				
V <sub>IH</sub>	Input High Voltage Level	1.7		0.7	
V <sub>IL</sub>	Input Low Voltage Level				
V <sub>ICR</sub>	Common mode Input Range	0.97		1.53	
V <sub>ID</sub>	Differential Input Voltage				
V <sub>IX</sub>	Cross Point Voltage of Differential Clock Pair	(V <sub>DDQ</sub> /2) -0.2		(V <sub>DDQ</sub> /2) +0.2	
I <sub>OH</sub>	High-Level Output Current			-20	
I <sub>OL</sub>	Low-Level Output Current			20	
T <sub>A</sub>	Operating Free-Air Temperature	0		70	°C

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - DC

$T_A = 0 - 70^\circ \text{C}$ ;  $V_{DD} = 2.5 \text{ V} \pm 200\text{mV}$ ,  $V_{DDQ} = 2.5\text{V} \pm 200\text{mV}$ ; (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS	VDD	MIN	TYP	MAX	UNITS
$V_{IK}$		$I_I = -18\text{mA}$	2.3V			-1.2	
		$I_{OH} = -100\mu\text{A}$	2.3V-2.7	$V_{DD} - 0.2$	2.5		
$V_{OH}$		$I_{OH} = -16\text{mA}$	2.3V	1.95	2		
		$I_{OL} = 100\mu\text{A}$	2.3-2.7V		0	0.2	V
$V_{OL}$		$I_{OL} = 16\text{mA}$	2.3V		0.16	0.35	
$I_I$	All Inputs	$V_I = V_{DD}$ or GND	2.7V			$\pm 5$	$\mu\text{A}$
$I_{DD}$	Standby (Static)	RESET# = GND	2.7V			0.01	$\mu\text{A}$
	Operating (Static)	$V_I = V_{IH(AC\#)}$ or $V_{IL(AC)}$ , RESET# = $V_{DD}$				TBD	mA
$I_{DDD}$	Dynamic operating clock only	RESET = $V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , CK and CK# switching 50% duty cycle.	2.7V	IO = 0		TBD	$\mu\text{A}/\text{clock MHz}$
	Dynamic Operating per each data input	RESET# = $V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , CK and CK# switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle				TBD	$\mu\text{A}/\text{clock MHz/data}$
$r_{OH}$	Output High	$I_{OH} = -20\text{mA}$	2.3-2.7V	7	15	20	$\Omega$
$r_{OL}$	Output Low	$I_{OL} = 20\text{mA}$	2.3-2.7V	7	10	20	$\Omega$
	[ $r_{OH} - r_{OL}$ ] each						
$r_{O(\Delta)}$	separate bit	$I_O = 20\text{mA}$ , $T_A = 25^\circ \text{C}$	2.5V			4	$\Omega$
	Data Inputs	$V_I = V_{REF} \pm 310\text{mV}$		2.5		3.5	
$C_i$	CK and CK#	$V_{ICR} = 1.25\text{V}$ , $V_{I(PP)} = 360\text{mV}$	2.5V	2.5		3.5	pF

Notes:

1 - Guaranteed by design, not 100% tested in production.



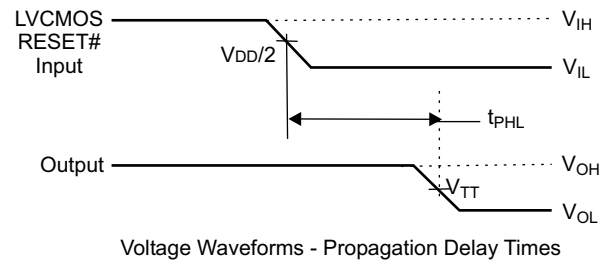
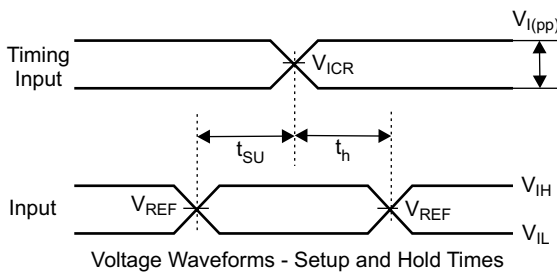
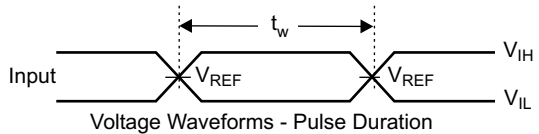
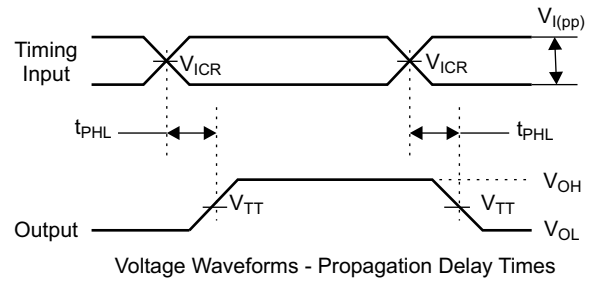
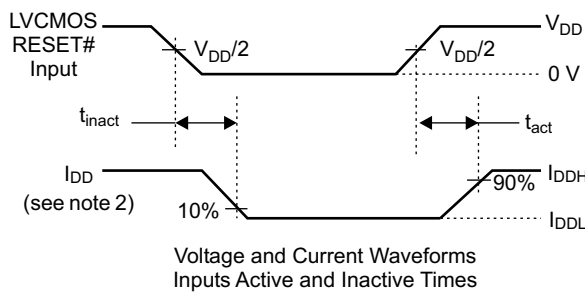
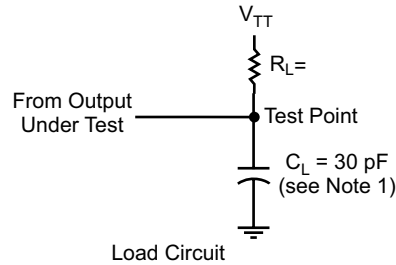
**Timing Requirements**

(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	PARAMETERS		VDD=2.5±0.2V			UNITS
			MIN	TYP	MAX	
f <sub>clock</sub>	Clock frequency			133	200	MHz
t <sub>PD</sub>	Clock to output time		1.1	2.4	2.8	ns
t <sub>RST</sub>	Reset to output time			3.1	5	ns
t <sub>SL</sub>	Output slew rate		1	1.5	4	V/ns
t <sub>SU</sub>	Setup time, fast slew rate <sup>2,4</sup>	Data before CK↑, CK#↓	0.75	0.018		ns
	Setup time, slow slew rate <sup>3,4</sup>		0.9			ns
T <sub>h</sub>	Hold time, fast slew rate <sup>2,4</sup>	Data after CK↑, CK#↓	0.75	0.145		ns
	Hold time, slow slew rate <sup>3,4</sup>		0.9			ns

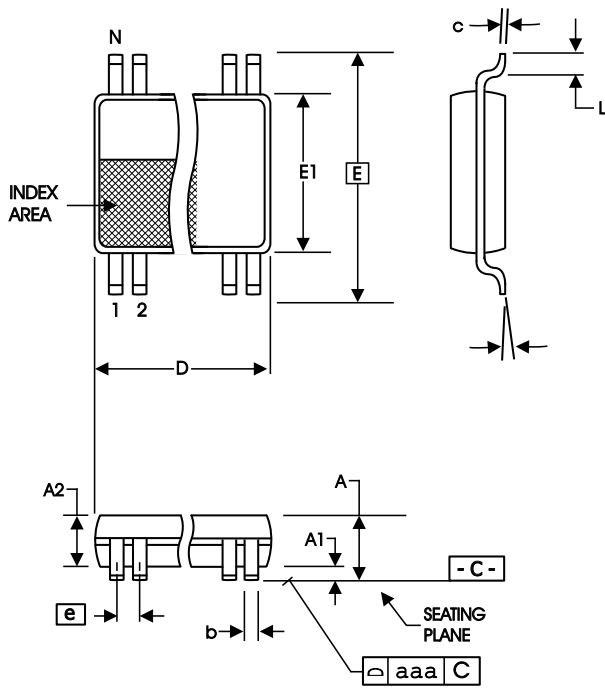
- Notes:
- 1 - Guaranteed by design, not 100% tested in production.
  - 2 - For data signal input slew rate =1V/ns.
  - 4 - CLK, CLK# signals input slew rates are =1V/ns.
  - 3 - For data signal input slew rate =0.5V/ns and < 1V/ns.

<b>Switching Characteristics</b>						
(over recommended operating free-air temperature range, unless otherwise noted)						
SYMBOL	From (Input)	To (Output)	VDD=2.5±0.2V			UNITS
			MIN	TYP	MAX	
f <sub>clock</sub>				133	200	MHz
t <sub>PD</sub>	CLK, CLK#	Q	1.1	2.4	2.8	ns
t <sub>ph1</sub>	RESET#	Q		3.1	5	ns



## Parameter Measurement Information ( $V_{DD} = 2.5V \pm 0.2V$ )

- Notes: 1.  $C_L$  includes probe and jig capacitance.  
 2.  $I_{DD}$  tested with clock and data inputs held at  $V_{DD}$  or GND, and  $I_o = 0 \text{ mA}$ .  
 3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ , input slew rate =  $1 \text{ V/ns} \pm 20\%$  (unless otherwise specified).  
 4. The outputs are measured one at a time with one transition per measurement.  
 5.  $V_{TT} = V_{REF} = V_{DD}/2$   
 6.  $V_{IH} = V_{REF} + 310 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVC MOS input.  
 7.  $V_{IL} = V_{REF} - 310 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVC MOS input.  
 8.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$



SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
$\alpha$	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

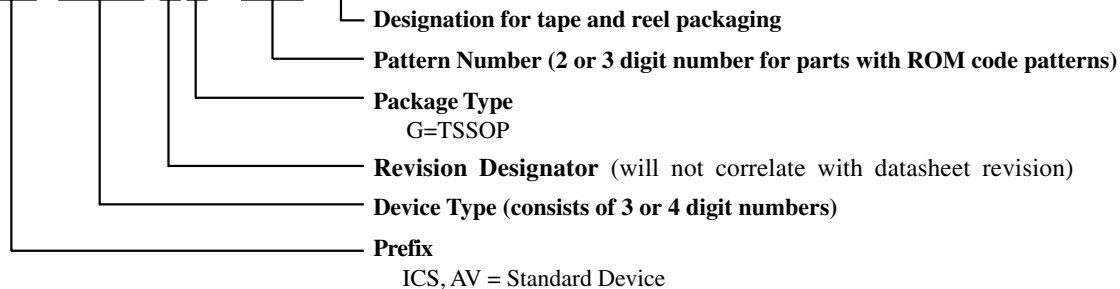
6.10 mm. Body, 0.50 mm. pitch TSSOP  
(240 mil) (0.020 mil)

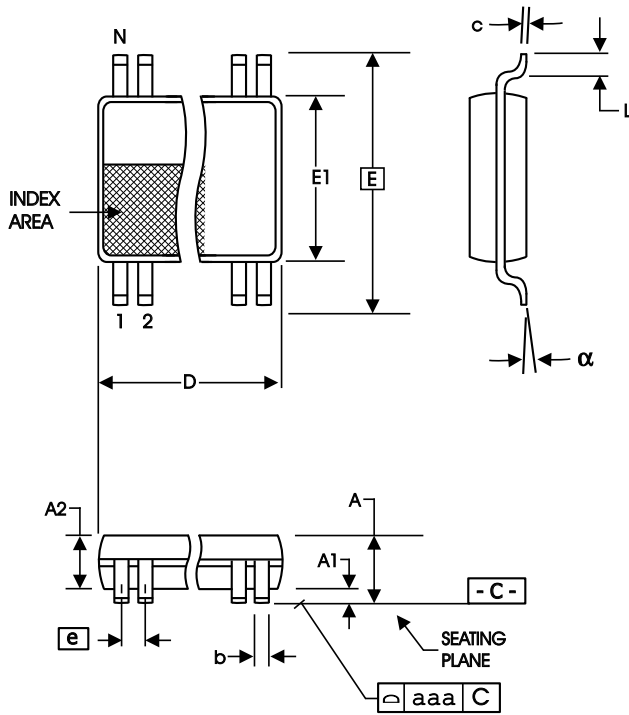
Ordering Information

ICSSSTV16857yG-T

Example:

ICS XXXX y G - PPP - T





SYMBOL	In Millimeters		In Inches		
	COMMON DIMENSIONS	MIN	MAX	MIN	MAX
A	--	1.20	--	.047	
A1	0.05	0.15	.002	.006	
A2	0.80	1.05	.032	.041	
b	0.13	0.23	.005	.009	
c	0.09	0.20	.0035	.008	
D	SEE VARIATIONS		SEE VARIATIONS		
E	6.40 BASIC		0.252 BASIC		
E1	4.30	4.50	.169	.177	
e	0.40 BASIC		0.016 BASIC		
L	0.45	0.75	.018	.030	
N	SEE VARIATIONS		SEE VARIATIONS		
alpha	0°	8°	0°	8°	
aaa	--	0.08	--	.003	

### VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153  
10-0037

**4.40 mm. Body, 0.40 mm. pitch TSSOP**  
(173 mil)      (16 mil)

## Ordering Information

**ICSSSTV16857yL-T**

Example:

**ICS XXXX y L - PPP - T**

