



# STS7PF30L

## P-CHANNEL 30V - 0.016Ω - 7A SO-8 STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS7PF30L	30 V	< 0.021 Ω	7 A

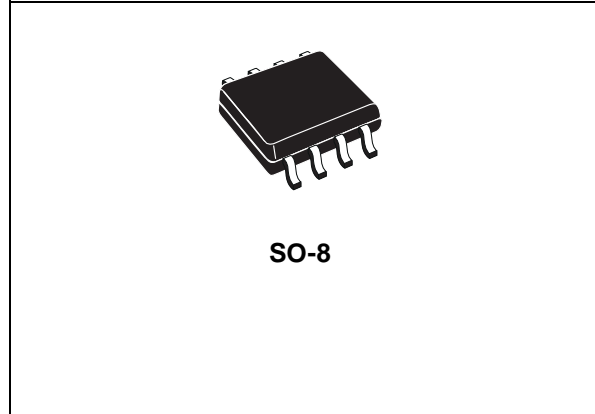
- TYPICAL R<sub>DS(on)</sub> = 0.016Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

### DESCRIPTION

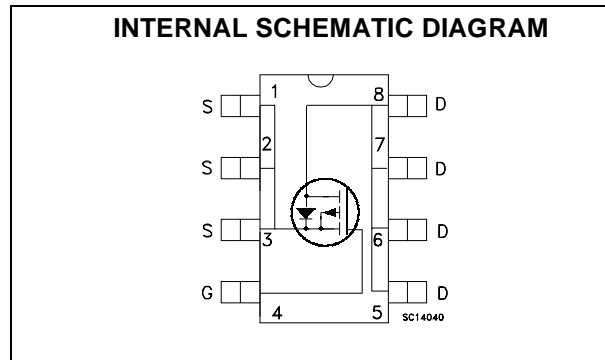
This Power Mosfet is the latest development of ST-Microelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES



SO-8



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	30	V
V <sub>GS</sub>	Gate- source Voltage	±20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	7	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	4.4	A
I <sub>DM</sub>	Drain Current (pulsed)	28	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	2.5	W

(●) Pulse width limited by safe operating area

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

## STS7PF30L

### THERMAL DATA

Rthj-amb(#)	Thermal Resistance Junction-ambient Max	50	°C/W
T <sub>j</sub>	Maximum Lead Temperature For Soldering Purpose Typ	150	°C
T <sub>stg</sub>	Storage Temperature	-55 to 150	°C

(#) When mounted on 1 inch<sup>2</sup> FR4 Board, 2 oz of Cu and t ≤ 10s

### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.6	2.5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.5A V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 3.5A	0.011 0.016	0.016 0.022	0.021 0.028	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> = 10V, I <sub>D</sub> = 3.5A		16		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		2600		pF
C <sub>oss</sub>	Output Capacitance			523		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			174		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**SWITCHING ON(2)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15V, I_D = 3.5A$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (Resistive Load, Figure 3)		68		ns
$t_r$	Rise Time			54		ns
$Q_g$	Total Gate Charge	$V_{DD} = 15V, I_D = 7A,$ $V_{GS} = 4.5V$		28	38	nC
$Q_{gs}$	Gate-Source Charge			8.8		nC
$Q_{gd}$	Gate-Drain Charge			12		nC

**SWITCHING OFF(2)**

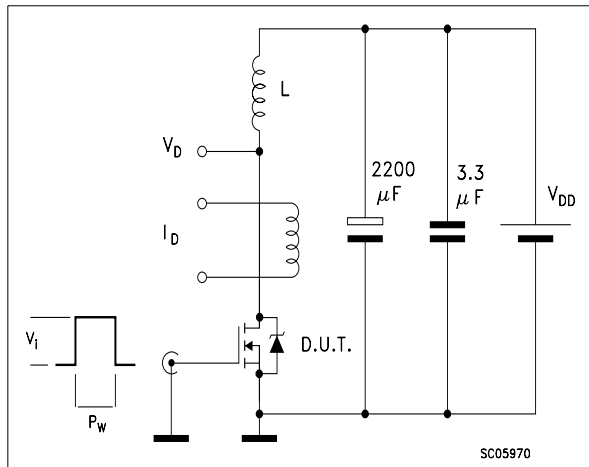
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15V, I_D = 3.5A,$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (Resistive Load, Figure 3)		65		ns
$t_f$	Fall Time			23		ns

**SOURCE DRAIN DIODE (2)**

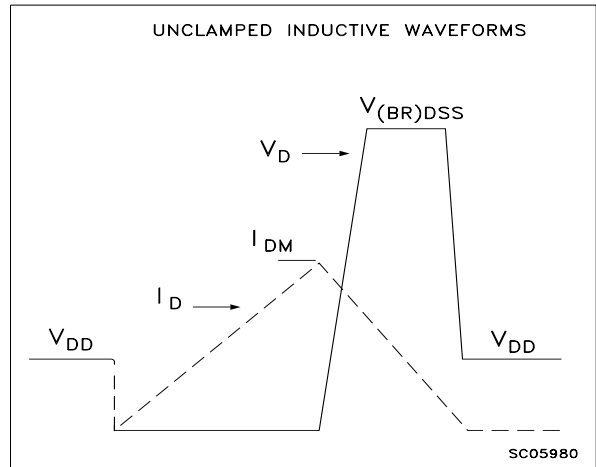
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				7	A
$I_{SDM} (1)$	Source-drain Current (pulsed)				28	A
$V_{SD} (2)$	Forward On Voltage	$I_{SD} = 7A, V_{GS} = 0$			1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 7A, di/dt = 100A/\mu s,$ $V_{DD} = 24V, T_j = 150^\circ C$ (see test circuit, Figure 5)		40		ns
$Q_{rr}$	Reverse Recovery Charge			46		nC
$I_{RRM}$	Reverse Recovery Current			2.3		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

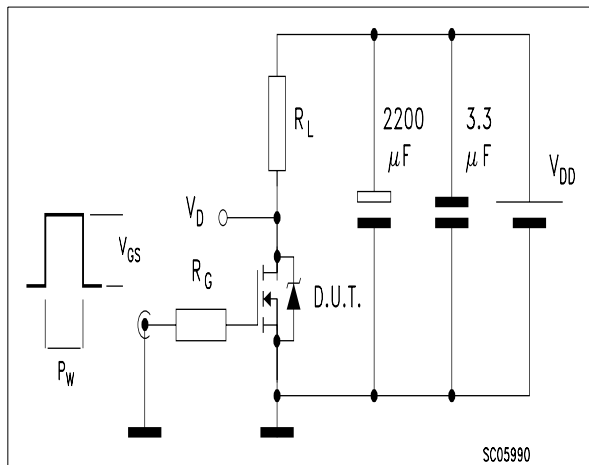
**Fig. 1: Unclamped Inductive Load Test Circuit**



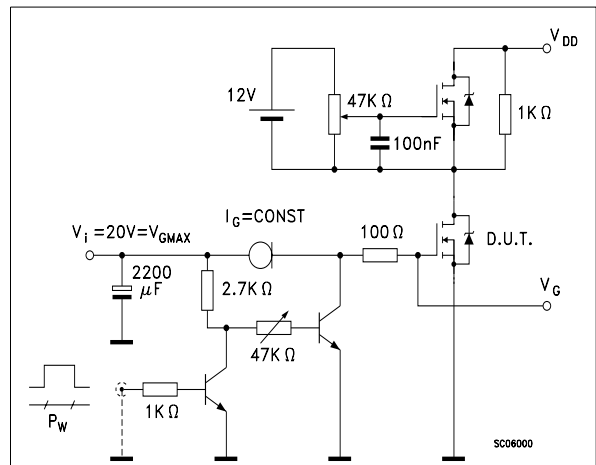
**Fig. 2: Unclamped Inductive Waveform**



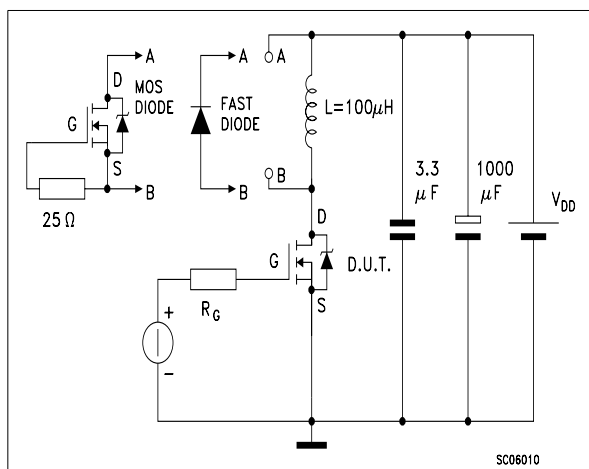
**Fig. 3: Switching Times Test Circuit For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

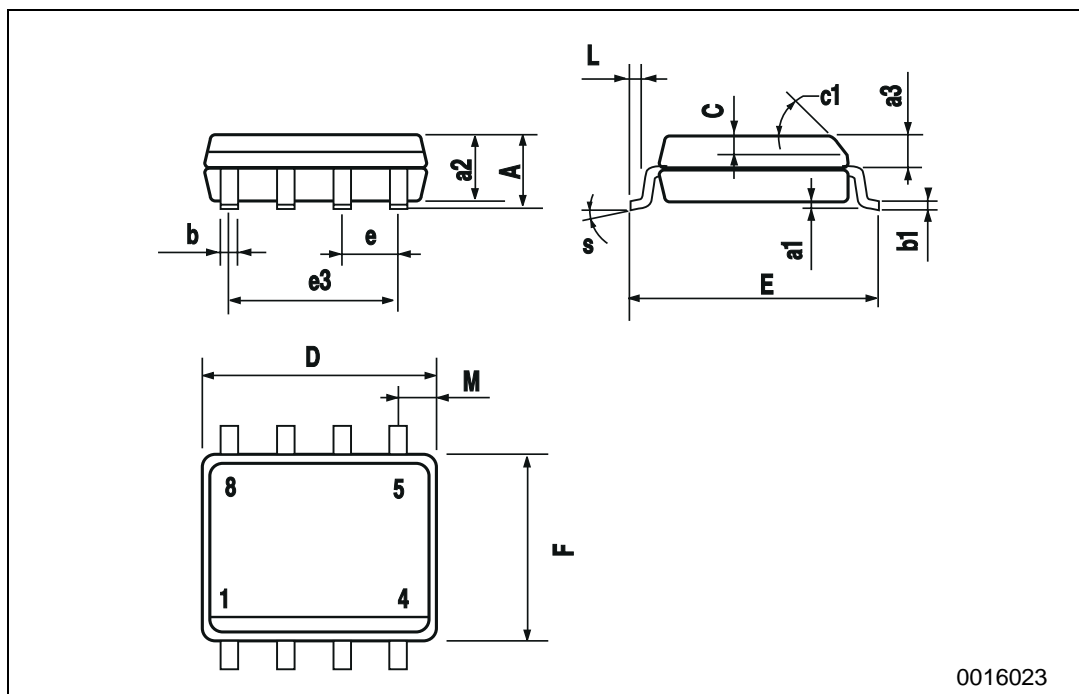


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



**SO-8 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>