DS89C450-K00
DS89C450 Evaluation Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS89C450-K00 Evaluation Kit is a proven platform to conveniently evaluate the capabilities of the Ultra-High-Speed Flash Microcontroller family. The kit contains the DS89C450 in a DIP-40 socket, 128K of SRAM mapped through a preprogrammed CPLD, a power-supply regulator, two DB-9 serial connectors, and switches and LEDs to control and display board operation. With the addition of a power supply and an RS-232 cable connected to a personal computer, the kit provides a completely functional system ideal for application development and debug.

The DS89C450-K00 can also be used as a programming and development platform for the DS5000(T). Quick-start instructions and sample programs can be obtained from the DS5000 directory on the software tool disk, or from Dallas Semiconductor technical support. Email us at micro.support@dalsemi.com.

FEATURES

- Easily Load Code Using Bootstrap Loader and Serial 0 Port (DB-9, J2)
- Two DB-9 RS-232 Serial Connectors
- Two Internal Serial Ports
- On-Board Power Supply Regulator
- 128K of On-Board Program+Data RAM
- Preprogrammed Xilinx CPLD Handles Address Multiplexing and RAM Mapping
- LED Display of Port 0 Levels
- Push-Button Switches for Reset and Interrupt Generation
- Prototyping Area
- Board Schematics Included to Provide a Convenient Reference Design

EVALUATION KIT CONTENTS

Evaluation Kit Board with Processor and 16.384MHz Crystal Installed

8051-Based Microcontroller Software Eval Disk

ORDERING INFORMATION

PART	TEMP RANGE	DIMENSIONS
DS89C450-K00	Room	Approx. 16cm x 10cm

Figure 1. DS89C450 Evaluation Kit Board

COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C6	2	100µF, 25V radial capacitors	Panasonic	ECA-1EM101
C2, C7	2	22µF, 10V tantalum capacitors	Panasonic	ECS-T1AX226R
C3, C4, C5, C8–C15	11	0.1µF capacitors (0805)	Generic	
C16, C17	2	22pF capacitors	Panasonic	ECJ-2VC1H220J
J1	1	2mm male power-barrel connector	CUI Inc.	PJ-002A
J2, J3	2	DB9 RS-232 female connectors	Amp/Tyco	745781-4
J4	1	Micro header pins (unpopulated)		
J5	1	Spare input header pins (unpopulated)		
JP1, JP2	2	Solder pad jumpers (closed)		
R1, R4	2	1.1kΩ resistors (0805)	Generic	
R2, R3	2	10kΩ resistors (0805)	Generic	
R5	1	680Ω resistor (0805)	Generic	
RN1, RN3, RN4	3	Resistor pack (8) – 330Ω	CTS	770101331
RN2	1	Resistor pack (8) – 3.3kΩ	CTS	770101332
SW1, SW4, SW5	3	DIP switch x8	C&K	SDA08H1KD
SW2, SW3	2	SPST pushbutton	Panasonic	EVQ-PAC04M
U1	1	350mA linear regulator (5V)	MAXIM	MAX1659ESA
U2	1	350mA linear regulator (3.3V)	MAXIM	MAX1658ESA
U3	1	DS89C450 microcontroller (40-PDIP)	DALLAS	DS89C450-MNL
U4	1	Quad buffer	Fairchild	74AC125
U5	1	Preprogrammed 44-pin CPLD	Xilinx	XC9536XL-10PC44C
U6	1	128k x 8 asynchronous cache SRAM	Cypress	AS7C1024A-10TJC
U7	—	Unpopulated	—	—
U8	1	RS-232 transceiver (2 Tx, 2 Rx)	MAXIM	MAX233ACWP
U9	1	Inverting octal buffer	Fairchild	74AC540
U10	1	LED x10 display (Port 1 + power)	Lumex	SSA-LXB10IW-GF/LP
Y1	1	16.384MHz crystal (socketed)	Citizen	HC49US16.384MABJ

TYPICAL OPERATING CIRCUIT

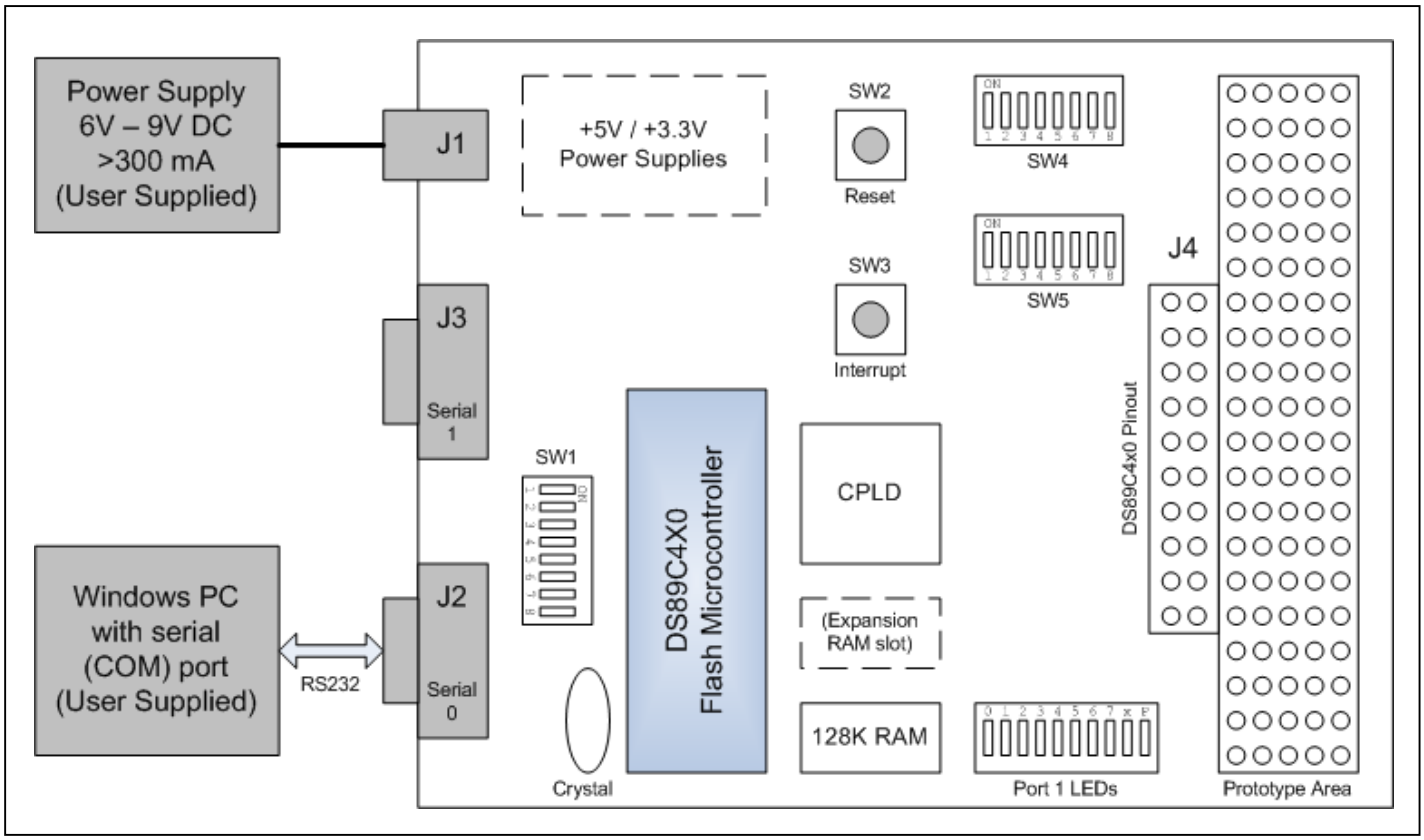


Figure 2. DS89C450 Evaluation Kit Board Layout

DETAILED DESCRIPTION

This evaluation kit must be used with the DS89C430/DS89C440/DS89C450 ultra-high-speed flash microcontrollers data sheet and the *Ultra-High-Speed Flash Microcontroller User's Guide* (www.maxim-ic.com/user_guides). A complete description of the bootstrap loader commands and functions is located in Section 15 of the *Ultra-High-Speed Flash Microcontroller User's Guide*.

The DS89C450 Evaluation Kit Board and all of its connectors are defined in the schematics provided in the accompanying documentation disk. However, a short description of the major components of the board follows.

Power Supplies

The evaluation kit accepts a DC input supply at J1. The supply should be a 6V to 9V DC supply, center post positive, with at least 300mA capacity. The exact DC input value of the supply is not important, as the on-board linear MAX1658 and MAX1659 regulators produce fixed 5V and 3.3V for use by the kit circuitry.

While it is possible to supply up to 16V at J1 (the maximum input voltage of the MAX1658 and MAX1659), this will result in a large amount of heat dissipation from the board. A small heat-sink plane is provided on the backside of the board beneath the linear regulators, but this may be inadequate at input voltages above 9V. If U1 and U2 are hot, lower the DC input voltage at J1. Note that many unregulated DC wall plug-in supplies may provide an output level much higher than their labeled output value if they are lightly loaded.

Serial Ports

Both serial ports of the DS89C450 (Serial Port 0 and Serial Port 1) are translated to RS-232 levels and brought out to DB9 connectors at J2 and J3. Serial Port 0 (J2) must always be used when communicating with the bootloader.

Memory

The external memory of the DS89C450 on this evaluation kit is designed to operate with the address and data bus multiplexed on P0 and P2. A 128K x 8 SRAM is installed, which is accessed as both program and data memory by this multiplexed bus. Note that as the total memory space of the DS89C450 is only 64K of program memory and 64K of data memory, port pin memory banking must be used to access the entire 128K-memory space.

CPLD

The CPLD device on the evaluation kit board is preprogrammed to perform several functions.

- Address latching of the low 8 bits of the external memory address from port P0.
- Mapping together program and data memory.
- Performing port pin memory banking (optional).

The RTL code preprogrammed into the CPLD is as follows.

```
module Eval(AD, nRD, ALE, nPSEN, CFG0, CFG1, SW_IN, P1, A, A16, A17, nOE, SW_OUT);

input  [7:0] AD;     // Multiplexed low-order address and data from micro
input        nRD;    // Data memory read enable from micro
input        ALE;    // Address latch enable from micro
input        nPSEN;  // Program memory read enable from micro
input        CFG0;   // Configuration input zero (from DIP switch)
input        CFG1;   // Configuration input one (from DIP switch)
input        SW_IN;  // Interrupt switch input (from pushbutton)

inout  [7:0] P1;     // Port 1 from micro

output [7:0] A;      // Demultiplexed low-order address to RAM
output       A16;    // Address line to RAM
output       A17;    // Address line to RAM
output       nOE;    // Output enable to RAM
output       SW_OUT; // Interrupt switch output (to micro)

reg    [7:0] A;

always @(negedge ALE) begin
   A <= AD;
end

assign A16    = (CFG0 == 0) ? P1[0] : 1'b0;
assign A17    = (CFG0 == 0) ? P1[1] : 1'b0;
assign P1[0]  = (CFG1 == 0) ?  SW_IN : 1'bz;
assign P1[1]  = (CFG1 == 0) ?  SW_IN : 1'bz;
assign P1[2]  = (CFG1 == 0) ?  SW_IN : 1'bz;
assign P1[3]  = (CFG1 == 0) ?  SW_IN : 1'bz;
assign P1[4]  = (CFG1 == 0) ? ~SW_IN : 1'bz;
assign P1[5]  = (CFG1 == 0) ? ~SW_IN : 1'bz;
assign P1[6]  = (CFG1 == 0) ? ~SW_IN : 1'bz;
assign P1[7]  = (CFG1 == 0) ? ~SW_IN : 1'bz;
assign nOE    = nRD & nPSEN;
assign SW_OUT = SW_IN;

endmodule
```

DIP switches SW4.3 and SW4.4 are used as configuration inputs by the CPLD program. Normally, these switches should be OFF for proper operation. Turning DIP switch SW4.3 ON causes the high address lines A16 and A17 to be set to the values at port pins P1.0 and P1.1. This can be used for address banking, but is not required for normal operation. Turning DIP switch SW4.4 on puts the CPLD into a test mode; press SW3 to toggle the LEDs.

Pushbuttons

Reset and interrupt pushbuttons are provided. The reset button resets the DS89C450, while the interrupt button can be configured to pull down either the INT0 (by setting SW1.4 ON) or T0 (by setting SW1.5 ON) inputs to the microcontroller when pressed.

Header Pins and Prototyping Area

Header J4 provides access to all pins of the DS89C450, including power and ground. This header is adjacent to a 0.100” spaced grid prototyping area for circuit development.

GETTING STARTED

Before using the DS89C450 Evaluation Kit, the Microcontroller Tool Kit (MTK) application should be installed. MTK is included on the CD and is available at www.maxim-ic.com/products/microcontrollers/software/index.cfm.

1) Connect the DC 6V–9V, center post positive power supply to the power plug J1.
2) Connect a DB9 straight-through serial cable between the PC COM1 port and connector J2.
3) Set DIP switches SW1.1, SW1.2, SW1.3, SW4.1, and SW4.2 ON. All other DIP switches should be OFF.
4) Turn power ON. All the LEDs should light except for the second from the right.
5) Open MTK. In the initial dialog box, select the type of processor you are using (DS89C430, DS89C440, or DS89C450).
6) Select **Options -> Configure Serial Port** from the menu. Enter COM1 and 14400 baud.
7) Select **Target -> Open COM1 at 14400 baud**.
8) Select **Target -> Connect to Loader**.
9) A loader banner should appear, as shown in Figure 3.

Refer to the user’s guide for more details on the bootloader commands for the DS89C450. To load an application into the DS89C450 flash memory, first enter “K” at the bootloader prompt to erase the flash, then select **File -> Load Flash** and open the .hex file you wish to load. The **Help** menu in MTK provides additional information.

The bootloader also allows you to write to Port 1 directly by entering “W P1 xx,” where xx is a hex byte value. If you enter a value such as “W P1 55” or “W P1 AA,” the LED display will change to reflect the new outputs at Port 1.

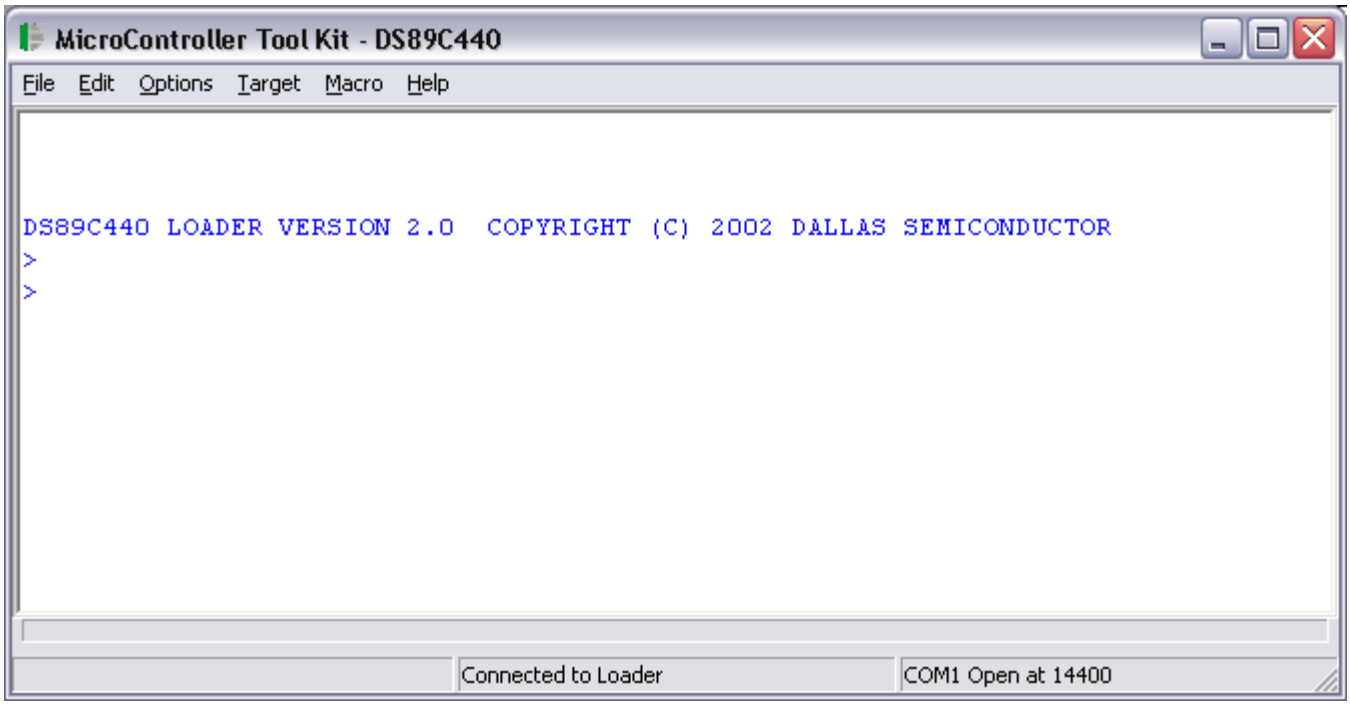


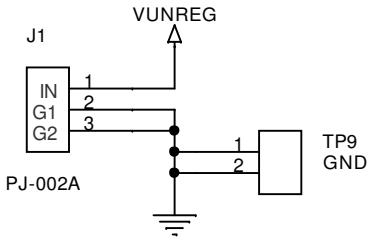
Figure 3. Microcontroller Tool Kit Output

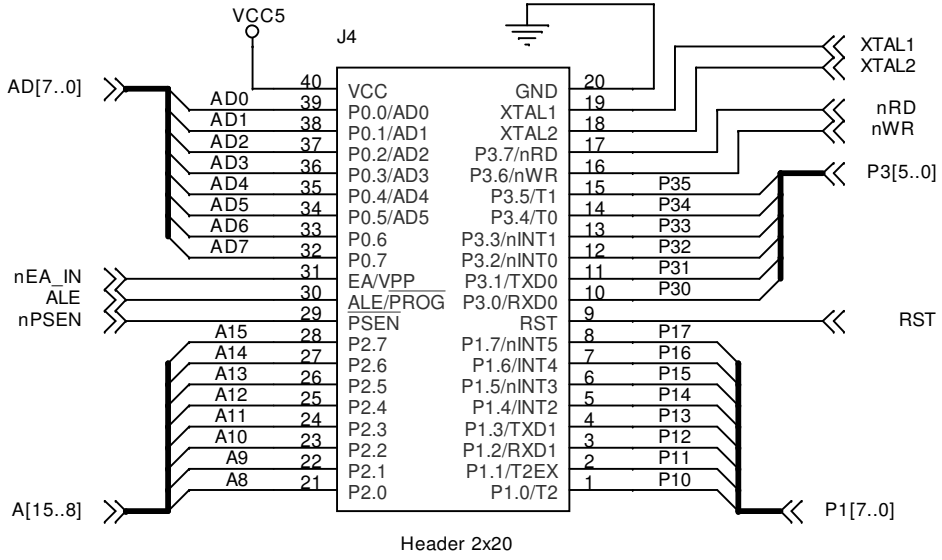
TECHNICAL SUPPORT

For additional technical support, e-mail your questions to micro.support@dalsemi.com.

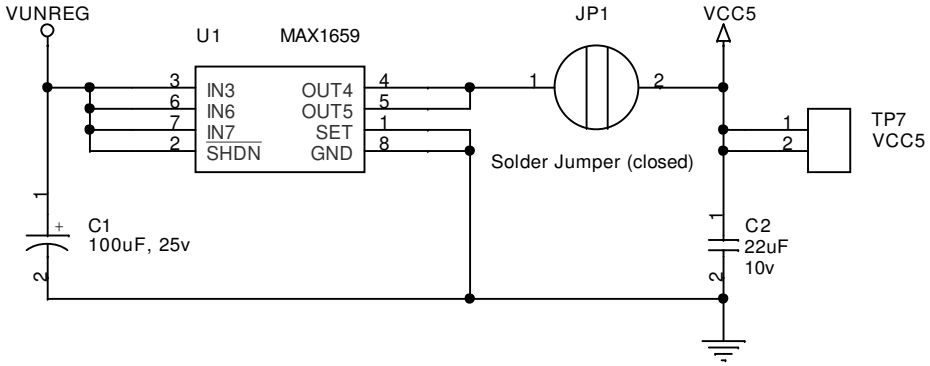
SCHEMATICS

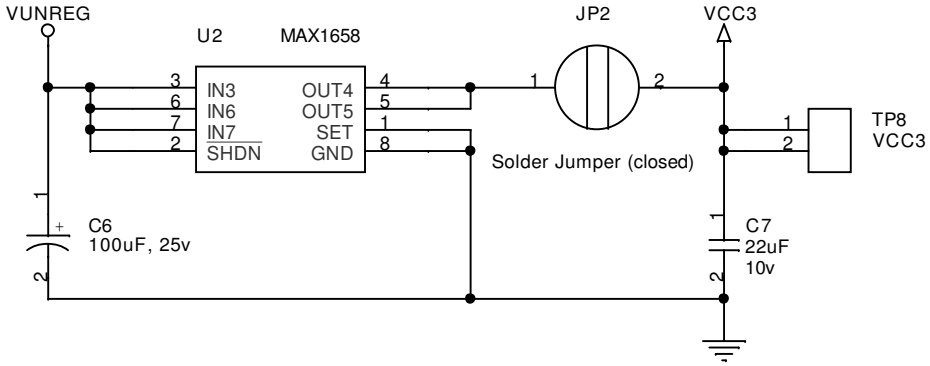
The DS89C450-K00 schematics are featured in the following six pages.

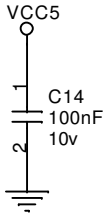




Header 2x20







DS89C4x0 Evaluation Kit - Power and Header	Rev B
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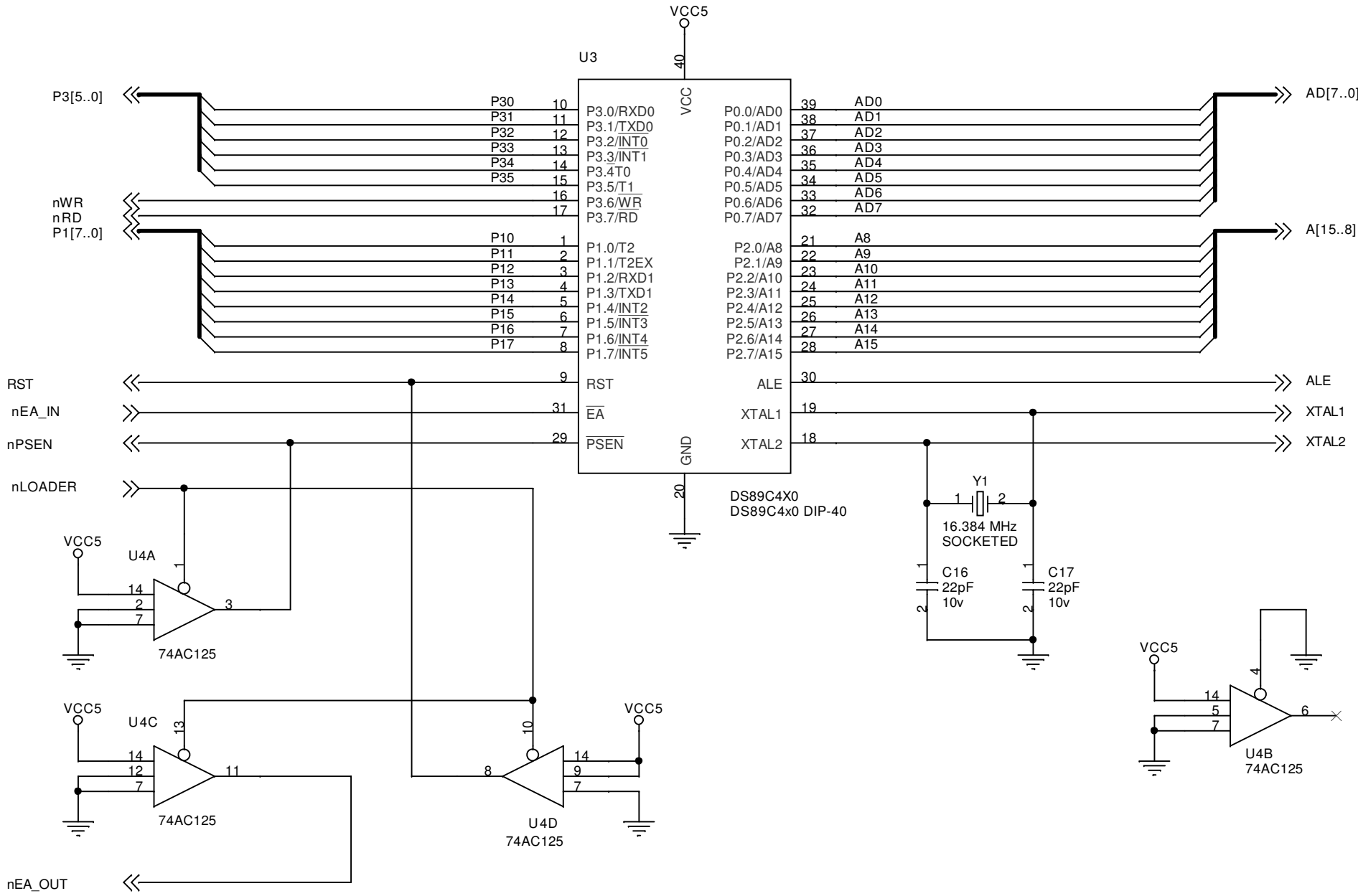
Size A	Document Number 87-2C420-KIT
Wednesday, August 25, 2004	Sheet 1 of 6



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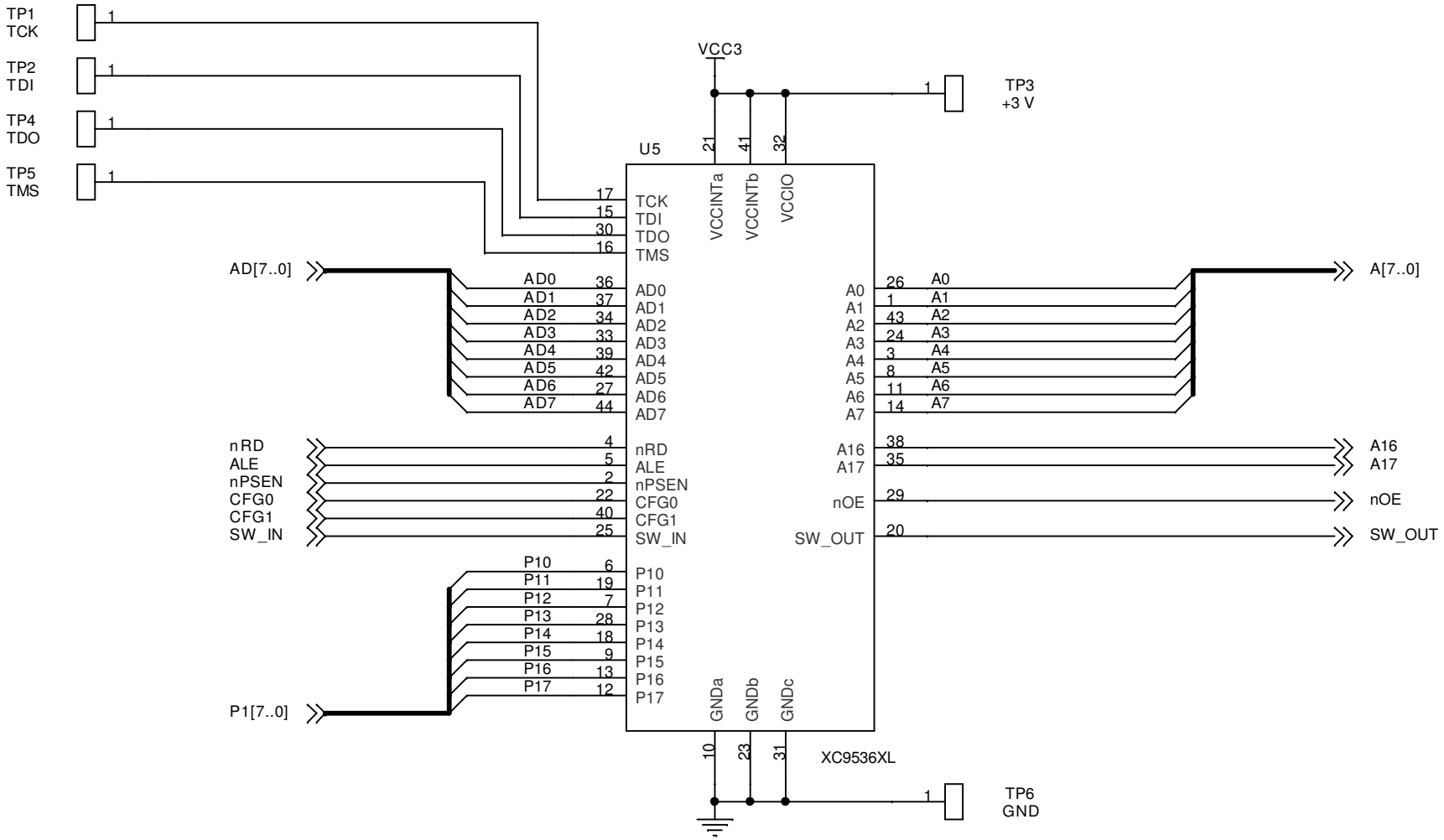

DS89C4x0 Evaluation Kit - CPLD	Rev B
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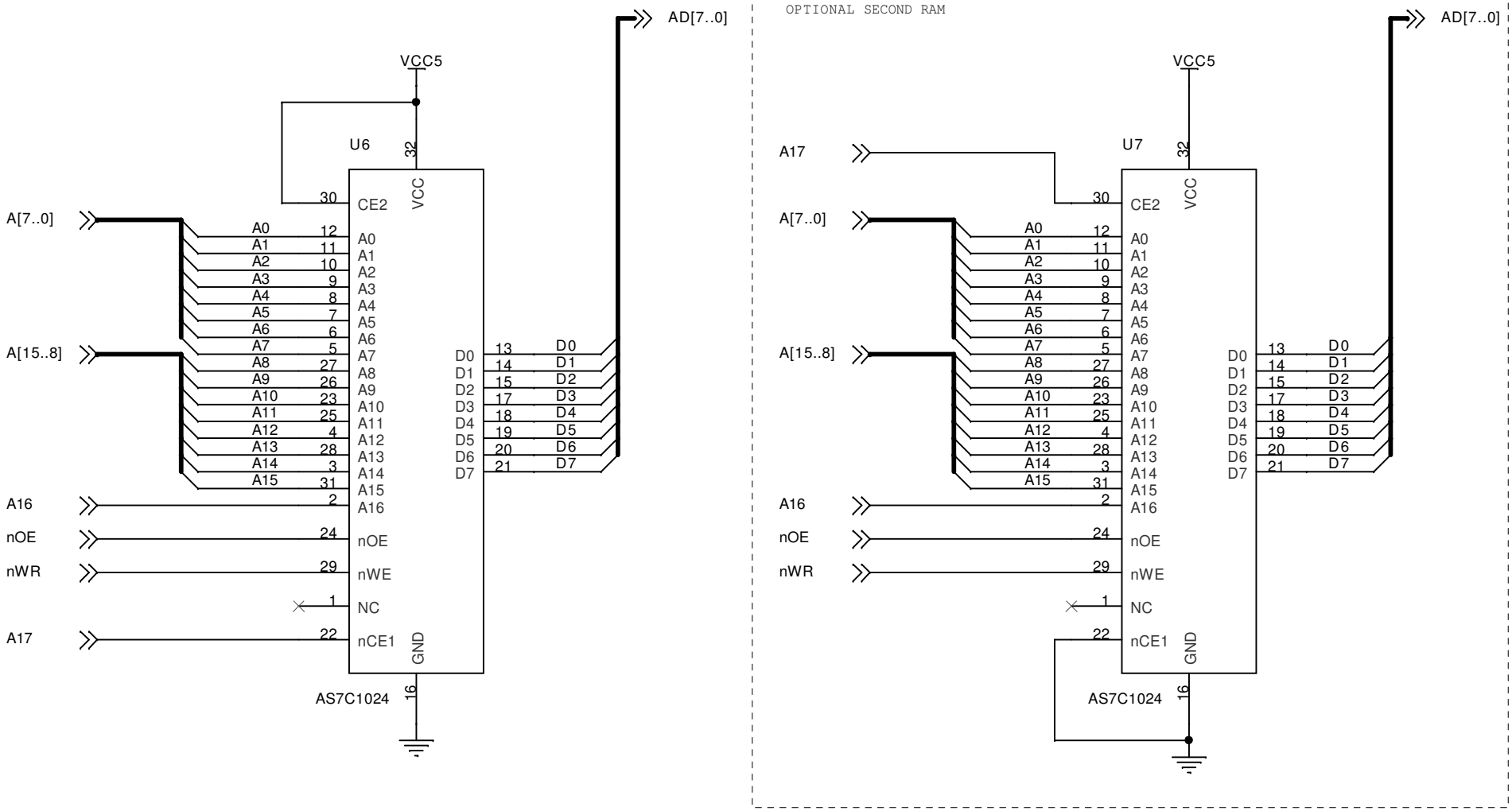
Wednesday, August 25, 2004	Sheet 3 of 6



DS89C4x0 Evaluation Kit - RAM	Rev B
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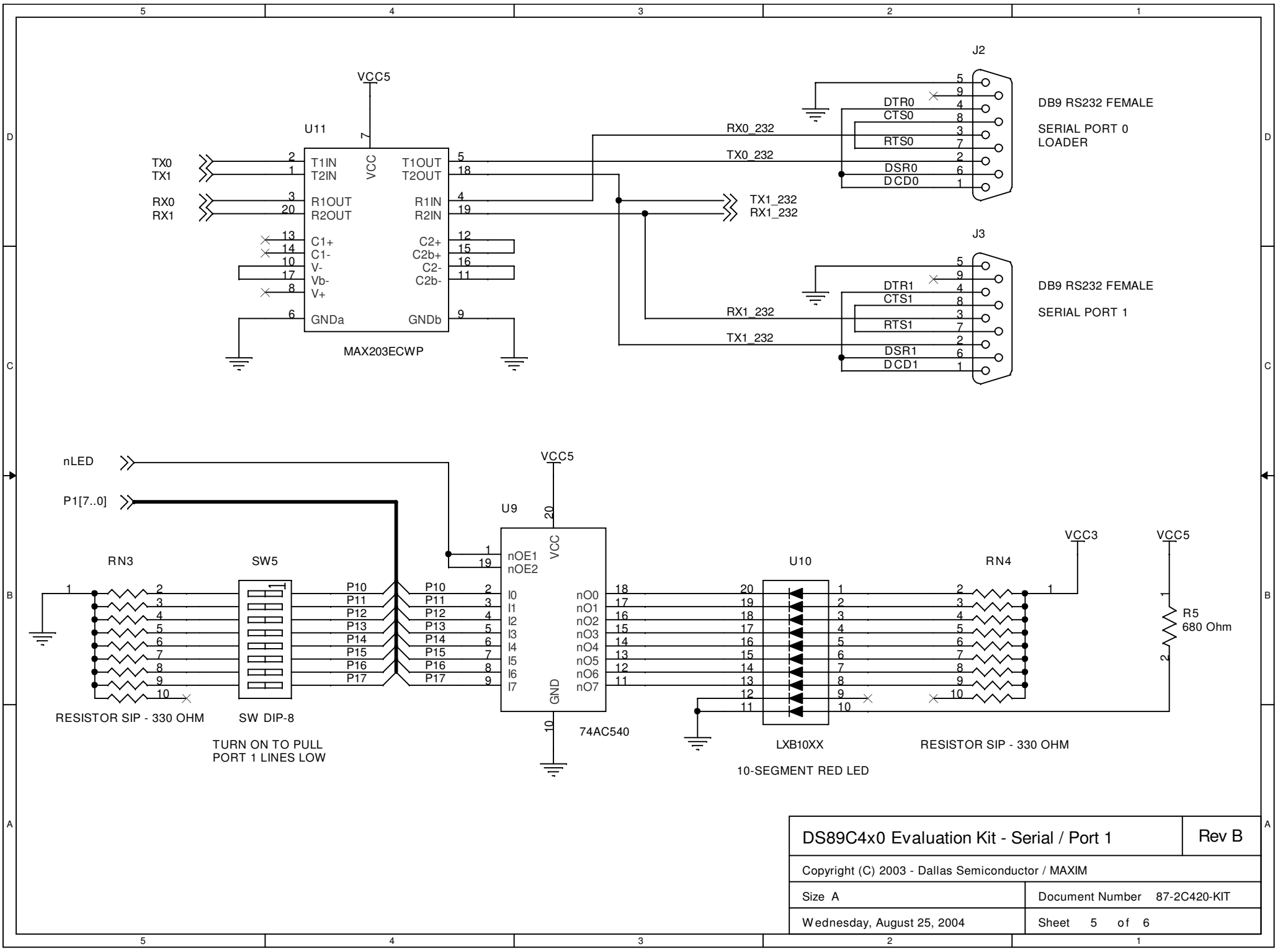
Wednesday, August 25, 2004	Sheet 4 of 6



DS89C4x0 Evaluation Kit - Serial / Port 1	Rev B
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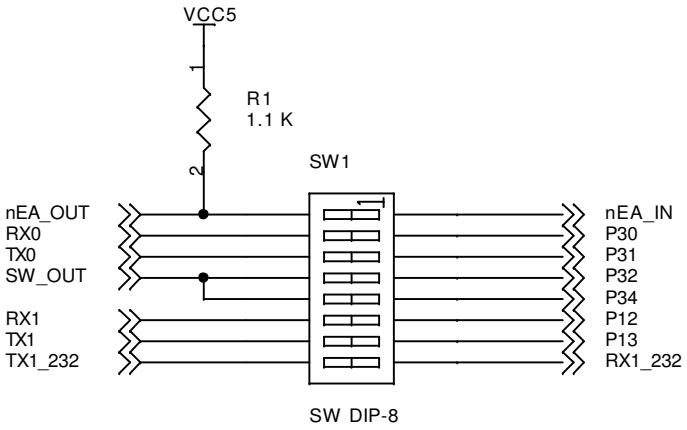
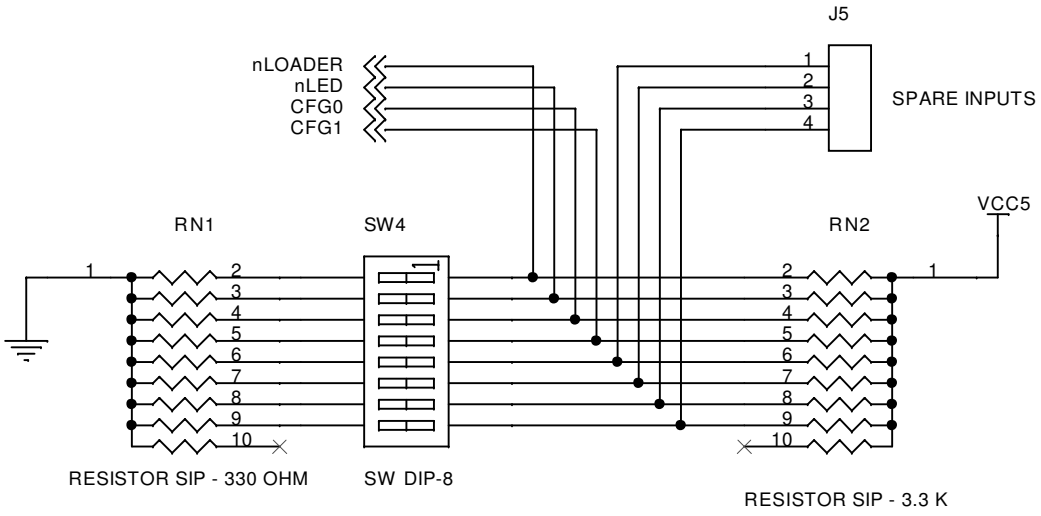
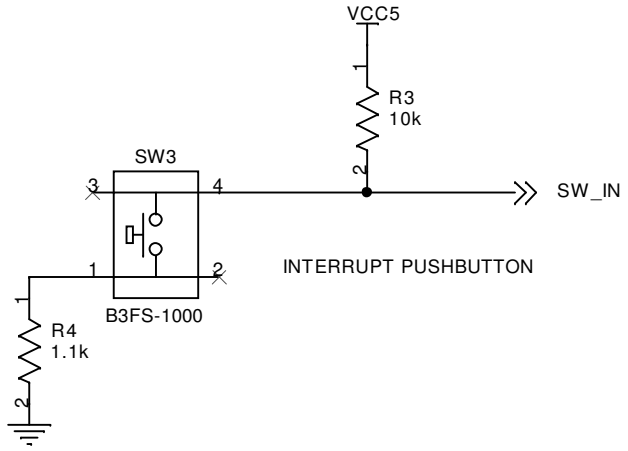
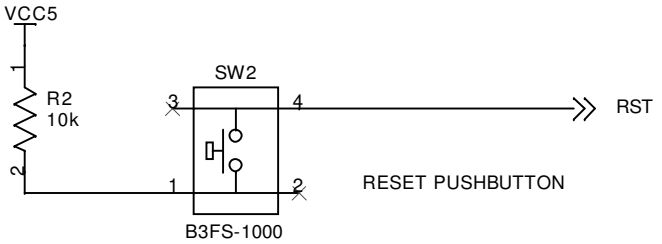




SW1.1 - ON FOR DS89C4x0
SW1.2 - ON TO USE SERIAL PORT 0 / LOADER
SW1.3 - ON TO USE SERIAL PORT 0 / LOADER
SW1.4 - ON TO CONNECT SW3 AND nINT0
SW1.5 - ON TO CONNECT SW3 AND T0
SW1.6 - ON TO USE SERIAL PORT 1
SW1.7 - ON TO USE SERIAL PORT 1
SW1.8 - OFF FOR NORMAL USE

SW1.1 - ON FOR LOADER MODE
SW1.2 - ON TO ENABLE LEDs
SW1.3 - OFF FOR NORMAL USE
SW1.4 - OFF FOR NORMAL USE
SW1.5 - UNUSED
SW1.6 - UNUSED
SW1.7 - UNUSED
SW1.8 - UNUSED





DS89C4x0 Evaluation Kit - Switches/Config	Rev B
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