# RELIABILITY REPORT 

FOR
MAX2531EGI
PLASTIC ENCAPSULATED DEVICES

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## MAXIM INTEGRATED PRODUCTS

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## Conclusion

The MAX2531 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ........Device Description
II. .........Manufacturing Information
III. .......Packaging Information
IV. .......Die Information
V. ........Quality Assurance Information
VI. ........Reliability Evaluation
......Attachments

## I. Device Description

A. General

The MAX2531 multiband LNA/Mixer IC is optimized for CDMA, GSM, and TDMA applications in cellular band. The MAX2531 IC features a GPS LNA/mixer signal path for E911 and Traveler Assistance applications. The cellular signal can be routed to either IF port. For example, one IF port can be connected to an IF filter with 30 kHz band-width, while the other port can drive an IF filter with a wider bandwidth. The GPS band has its own IF port.

To optimize dynamic range at minimum current, the MAX2531 implements multiple LNA and mixer states, including high gain/high linearity, high gain/low linearity, mid gain, low gain, and ultra low gain. In high-gain/highlinearity mode, the high-intercept LNA minimizes desensitization in the presence of a large interfering signal. For the other gain states, the LNA current is reduced to improve standby time. Each band is implemented with a separate mixer to optimize performance for the specific band, and each mixer provides multiple linearity modes to optimize linearity and current consumption. The ultra-low gain mode operates with very little current, which results in significant power savings because the handset typically spends most of its time in this mode.

## B. Absolute Maximum Ratings

| Item |
| :--- |
| $V_{\text {CC }}$ to GND |
| Digital Input Voltage to Gnd |
| LNA Inout (Low-Gain Mode) Level |
| LO Input Level |
| Digital Input Current |
| Junction Temperature |
| Operating Temperature Range |
| Storage Temp. |
| Lead Temp. (soldering 10 sec.) |
| Continuous Power Dissipation $\left(\mathrm{TA}=+70^{\circ} \mathrm{C}\right)$ |
| $\quad 28-\mathrm{Pin}$ QFN |
| Derates above $+70^{\circ} \mathrm{C}$ |
| $28-\mathrm{Pin}$ QFN |

## Rating

-0.3 V to +4.3 V
-0.3 V to (VCC +0.3 V )
15dBm
5dBM
10 mA
$+150^{\circ} \mathrm{C}$
$-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
$+300^{\circ} \mathrm{C}$
1.6W
$21 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$

## II. Manufacturing Information

| A. Description/Function: | Quadruple-Mode PCS/Cellular/GPS LNA/Mixers |
| :--- | :--- |
| B. Process: | MB20 Bi-CMOS Process |
| C. Number of Device Transistors: | 2538 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | Korea |
| F. Date of Initial Production: | April, 2002 |

## III. Packaging Information

A. Package Type:
B. Lead Frame:
C. Lead Finish:
D. Die Attach:
E. Bondwire:
F. Mold Material:
G. Assembly Diagram:
H. Flammability Rating:

Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:

## 28-Pin QFN

Copper
Solder Plate
Silver-Filled Epoxy
Gold (1.3 mil dia.)
Epoxy with silica filler
\# 05-9000-0247

Level 1

## IV. Die Information

A. Dimensions:
$89 \times 87$ mils
B. Passivation:
$\mathrm{Si}_{3} \mathrm{~N}_{4}$ (Silicon nitride)
C. Interconnect:
Au
D. Backside Metallization:
E. Minimum Metal Width:
F. Minimum Metal Spacing:
1.6 microns (as drawn) Metal 1, 2 \& 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:
H. Isolation Dielectric:
$\mathrm{SiO}_{2}$
I. Die Separation Method:
Wafer Saw

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager) Bryan Preeshl (Executive Director of QA) Kenneth Huening (Vice President)
B. Outgoing Inspection Level: $0.1 \%$ for all electrical parameters guaranteed by the Datasheet. $0.1 \%$ For all Visual Defects.
C. Observed Outgoing Defect Rate: < 50 ppm
D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

## A. Accelerated Life Test

The results of the $150^{\circ} \mathrm{C}$ biased (static) life test are shown in Table 1. Using these results, the Failure Rate $(\lambda)$ is calculated as follows:


This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a $60 \%$ confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic \#06-7030 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).
B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a $20 \%$ LTPD for acceptance. Additionally, industry standard $85^{\circ} \mathrm{C} / 85 \% \mathrm{RH}$ or HAST tests are performed quarterly per device/package family.
C. E.S.D. and Latch-Up Testing

The WC19-3 die type has been found to have all pins able to withstand a transient pulse of $\pm 800 \mathrm{~V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

Latch-Up testing has shown that this device withstands a current of $\pm 250 \mathrm{~mA}$.

Table 1
Reliability Evaluation Test Results
MAX2531EGI

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE <br> SIZE | NUMBER OF FAILURES |
| :---: | :---: | :---: | :---: | :---: |
| Static Life Test (Note 1) |  |  |  |  |
|  | $\mathrm{Ta}=150^{\circ} \mathrm{C}$ | DC Parameters | 90 | 0 |
|  | Biased | \& functionality |  |  |
|  |  |  |  |  |
| Moisture Testing (Note 2) |  |  |  |  |
| Pressure Pot | $\mathrm{Ta}=121^{\circ} \mathrm{C}$ | DC Parameters \& functionality | 77 | 0 |
|  | $\mathrm{P}=15 \mathrm{psi}$. |  |  |  |
|  | $\mathrm{RH}=100 \%$ |  |  |  |
|  | Time $=168 \mathrm{hrs}$. |  |  |  |
| 85/85 | $\mathrm{Ta}=85^{\circ} \mathrm{C}$ | DC Parameters \& functionality | 77 | 0 |
|  | RH = 85\% |  |  |  |
|  | Biased |  |  |  |
|  | Time $=1000 \mathrm{hrs}$. |  |  |  |

Mechanical Stress (Note 2)

| Temperature | $-65^{\circ} \mathrm{C} / 150^{\circ} \mathrm{C}$ | DC Parameters | 77 | 0 |
| :--- | :--- | :--- | :--- | :--- |
| Cycle | 1000 Cycles |  |  |  |
|  | Method 1010 |  |  |  |

Note 1: Life Test Data may represent plastic DIP qualification packages.
Note 2: Generic package/process data.

TABLE II. $\underline{\text { Pin combination to be tested. } 1 / 2 / 2}$

|  | Terminal A <br> (Each pin individually <br> connected to terminal A <br> with the other floating) | Terminal B <br> (The common combination <br> of all like-named pins <br> connected to terminal B) |
| :---: | :---: | :---: |
| 1. | All pins except $\mathrm{V}_{\text {PS1 }}$ 3/ | All $\mathrm{V}_{\text {PS } 1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground
(e.g., where $\mathrm{V}_{\mathrm{PS} 1}$ is $\mathrm{V}_{\mathrm{DD}}, \mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{SS}}, \mathrm{V}_{\mathrm{BB}}, G N D,+\mathrm{V}_{\mathrm{S}},-\mathrm{V}_{\mathrm{S}}, \mathrm{V}_{\mathrm{REF}}$, etc).

### 3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{S S 1}$, or $V_{S S 2}$ or $V_{S S 3}$ or $V_{C C 1}$, or $V_{C C 2}$ ) connected to terminal B . All pins except the one being tested and the power supply pin or set of pins shall be open.
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.


Notice 8

$\square / Z \Delta$ bandable area


PKG. BUDY SIZE: $5 \times 5 \mathrm{~mm}$

| PKG. CIDE: ${ }_{\text {G2855-2 }}$ |  | SİNATURES | DATE | /VIAXI/VI |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CAV./PAD SIZE: | PKG. |  |  | BCND DIAGRAM \#: | REV: |
| $130 \times 130$ | DESIGN |  |  | 05-9000-0247 | A |


|  |  |  |
| :---: | :---: | :---: |
|  |  | ONCE PER BOARD $13.6 \mathrm{~V}$ |
| DEVICES: MAX 2530/2531/2538/2539/2351/2358 <br> MAX. EXPECTED CURRENT = 40mA | DRAWN BY: HAK TAN NOTES: |  |

