19-1352; Rev 3; 8/03

EVALUATION KIT AVAILABLE

900MHz Image-Reject Receivers

General Description

The MAX2440/MAX2441/MAX2442 highly integrated front-end receiver ICs provide the lowest cost solution for cordless phones and ISM-band radios operating in the 900MHz band. All devices incorporate receive image-reject mixers to reduce filter cost. They operate with a +2.7V to +4.8V power supply, allowing direct connection to a 3-cell battery stack.

The signal path incorporates an adjustable-gain LNA and an image-reject downconverter with 35dB image suppression. These features yield excellent combined downconverter noise figure (4dB) and high linearity with an input third-order intercept point (IP3) of up to +2dBm.

All devices include an on-chip local oscillator (LO), requiring only an external varactor-tuned LC tank for operation. The integrated divide-by-64/65 dual-modulus prescaler can also be set to a direct mode, in which it acts as an LO buffer amplifier. Three separate power-down inputs can be used for system power management, including a 0.5µA shutdown mode. These parts are compatible with commonly used modulation schemes such as FSK, BPSK, and QPSK, as well as frequency hopping and direct sequence spread-spectrum systems. All devices come in a 28-pin SSOP package.

Evaluation kits are available for the MAX2420/MAX2421/MAX2422. The MAX2420/MAX2421/MAX2422 are transceivers whose receive sections and pinout are identical to the MAX2440/MAX2441/MAX2442.

For complete transceiver devices, refer to the MAX2420/MAX2421/MAX2422/MAX2460/MAX2463 and MAX2424/MAX2426 data sheets.

Applications

Cordless Phones
Wireless Telemetry
Wireless Networks
Spread-Spectrum Communications
Two-Way Paging

Selector Guide

PART	IF FREQ (MHz)	INJECTION TYPE	LO FREQ (MHz)
MAX2440	10.7	High side	f_{RF} + 10.7
MAX2441	46	High side	f_{RF} + 46
MAX2442	70	High side	f_{RF} + 70

Features

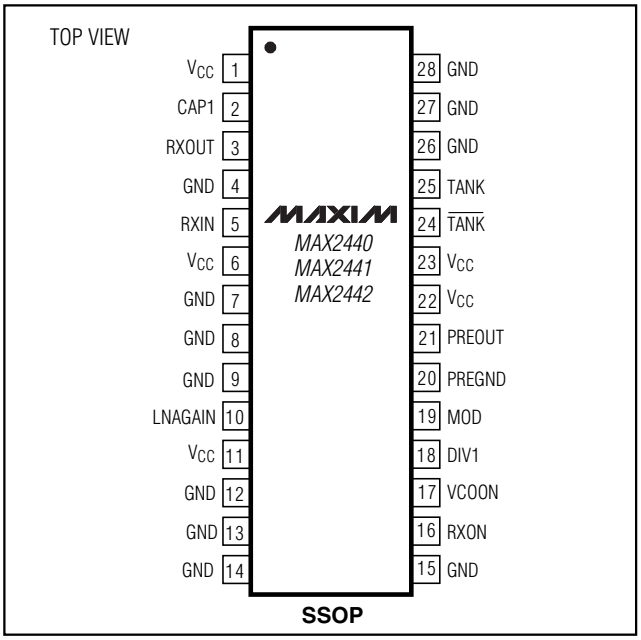
- **Receive Mixer with 35dB Image Rejection**
- **Adjustable-Gain LNA**
- **Up to +2dBm Combined Receiver Input IP3**
- **4dB Combined Receiver Noise Figure**
- **Low Current Consumption:**
  23mA Receive
  9.5mA Oscillator
- **0.5µA Shutdown Mode**
- **Operates from Single +2.7V to +4.8V Supply**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2440EAI	-40°C to +85°C	28 SSOP
MAX2441EAI	-40°C to +85°C	28 SSOP
MAX2442EAI	-40°C to +85°C	28 SSOP

Functional Diagram appears at end of data sheet.

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +5.5V
Voltage on LNAGAIN, RXON, VCOON, DIV1, MOD .....-0.3V to (V_{CC} + 0.3V)
RXIN Input Power.....10dBm
TANK, $\overline{TANK}$ Input Power.....2dBm
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.50mW/°C above +70°C) 762mW
Operating Temperature Range
MAX244_EAI .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +4.8V, no RF signals applied, LNAGAIN = unconnected, V_{VCOON} = 2.4V, V_{RXON} = V_{MOD} = V_{DIV1} = 0.45V, PREGND = GND, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, V_{CC} = +3.3V, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply-Voltage Range			2.7		4.8	V
Oscillator Supply Current	PREGND = unconnected			9.5	14	mA
Prescaler Supply Current (divide-by-64/65 mode)	(Note 2)			4.2	6	mA
Prescaler Supply Current (buffer mode)	V_{DIV1} = 2.4V (Note 3)			5.4	8.5	mA
Receive Supply Current	V_{RXON} = 2.4V, PREGND = unconnected (Note 4)			23	36	mA
Shutdown Supply Current	VCOON = RXON = MOD = DIV1 = GND	T_A = +25°C		0.5		µA
		T_A = T_{MIN} to T_{MAX}			10	
Digital Input Voltage High	RXON, DIV1, VCOON, MOD		2.4			V
Digital Input Voltage Low	RXON, DIV1, VCOON, MOD				0.45	V
Digital Input Current	Voltage on any one digital input = V_{CC} or GND			±1	±10	µA

Note 1: ≥25°C guaranteed by production test, <25°C guaranteed through correlation to worst-case temperature testing.
Note 2: Calculated by measuring the combined oscillator and prescaler supply current and subtracting the oscillator supply current.
Note 3: Calculated by measuring the combined oscillator and LO buffer supply current and subtracting the oscillator supply current.
Note 4: Calculated by measuring the combined receive and oscillator supply current and subtracting the oscillator supply current. With LNAGAIN = GND, the supply current drops by 4.5mA.

AC ELECTRICAL CHARACTERISTICS

(MAX242X/MAX246X EV kit, V_{CC} = +3.3V; f_{LO} = 925.7MHz (MAX2440), f_{LO} = 961MHz (MAX2441), f_{LO} = 985MHz (MAX2442), f_{RXIN} = 915MHz; P_{RXIN} = -35dBm; $V_{LNAGAIN}$ = 2V; V_{VCOON} = V_{RXON} = 2.4V; RXON = MOD = DIV1 = PREGND = GND; T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
RECEIVER							
Input Frequency Range	(Notes 5, 6)			800		1000	MHz
IF Frequency Range	(Notes 5, 6)	MAX2440		8.5	10.7	12.5	MHz
		MAX2441		36	46	55	
		MAX2442		55	70	85	
Image Frequency Rejection				26	35		dB
Conversion Power Gain	(Note 7)	LNAGAIN = V_{CC}, T_A = +25°C	MAX2440/MAX2441	20	22	24.5	dB
			MAX2442	19	21	23.5	
		LNAGAIN = V_{CC}, T_A = T_{MIN} to T_{MAX} (Note 5)	MAX2440/MAX2441	19.5		25	
			MAX2442	18		24	
		$V_{LNAGAIN}$ = 1V			12		
		LNAGAIN = GND			-16		
Noise Figure	DIV1 = V_{CC} (Notes 5, 7)	LNAGAIN = V_{CC}			4	5	dB
		$V_{LNAGAIN}$ = 1V			12		
Input Third-Order Intercept	(Notes 5, 8)	LNAGAIN = V_{CC}		-19	-17		dBm
		$V_{LNAGAIN}$ = 1V			-8		
Input 1dB Compression	LNAGAIN = V_{CC}				-26		dBm
	$V_{LNAGAIN}$ = 1V				-18		
LO to RXIN Leakage	Receiver on or off				-60		dBm
Receiver Turn-On Time	(Note 9)				500		ns

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX242X/MAX246X EV kit, V_{CC} = +3.3V; f_{LO} = 925.7MHz (MAX2440), f_{LO} = 961MHz (MAX2441), f_{LO} = 985MHz (MAX2442), f_{RXIN} = 915MHz; P_{RXIN} = -35dBm; $V_{LNAGAIN}$ = 2V; V_{VCOON} = V_{RXON} = 2.4V; RXON = MOD = DIV1 = PREGND = GND; T_A = +25°C, unless otherwise noted.)

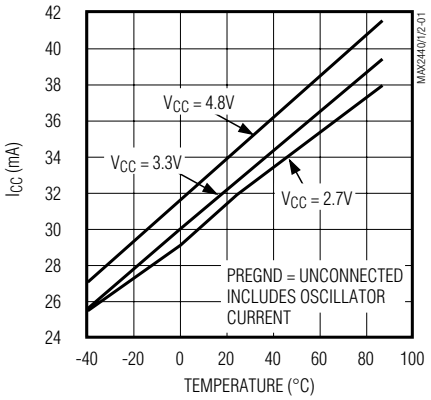
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR AND PRESCALER						
Oscillator Frequency Range	(Notes 5, 10)		690		1100	MHz
Oscillator Phase Noise	10kHz offset (Note 11)			82		dBc/Hz
Oscillator Pulling	Standby to RX			8		kHz
	Standby mode with P_{RXIN} = -45dBm to P_{RXIN} = 0dBm (Note 12)			70		
Prescaler Output Level	Z_L = 100kΩ || 10pF			500		mVp-p
Oscillator Buffer Output Level	DIV1 = 2.4V, Z_L = 50Ω (Note 5)	T_A = +25°C	-11	-8		dBm
		T_A = T_{MIN} to T_{MAX}	-12			
Required Modulus Setup Time	Divide-by-64/65 mode (Notes 5, 13)		10			ns

Note 5: Guaranteed by design and characterization.
Note 6: Image rejection typically falls to 30dBc at the frequency extremes.
Note 7: Refer to the *Typical Operating Characteristics* for plots showing receiver gain versus LNAGAIN voltage, input IP3 versus LNAGAIN voltage, and noise figure versus LNAGAIN voltage.
Note 8: Two tones at P_{RXIN} = -45dBm each, f1 = 915.0MHz and f2 = 915.2MHz.
Note 9: Time delay from RXON = 0.45V to RXON = 2.4V transition to the time the output envelope reaches 90% of its final value.
Note 10: Refers to useable operating range. Tuning range of any given tank circuit design is typically much narrower (refer to Figure 1).
Note 11: Using tank components L3 = 5.0nH (Coilcraft A02T), C2 = C3 = C26 = 3.3pF, R6 = R7 = 10Ω.
Note 12: This approximates a typical application in which a transmitter is followed by an external PA and a T/R switch with finite isolation.
Note 13: Relative to the rising edge of PREOUT.

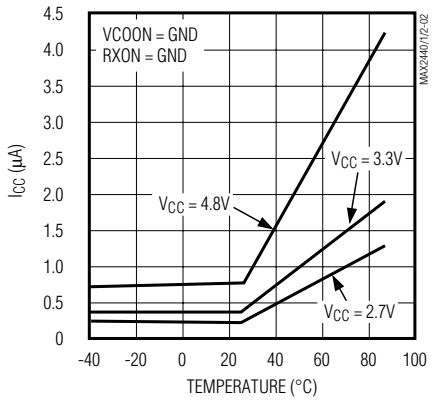
Typical Operating Characteristics

(MAX242X/MAX246X EV kit, V_{CC} = +3.3V; f_{LO} = 925.7MHz (MAX2440), f_{LO} = 961MHz (MAX2441), f_{LO} = 985MHz (MAX2442), f_{RXIN} = 915MHz; P_{RXIN} = -35dBm; $V_{LNAGAIN}$ = 2V; V_{VCOON} = 2.4V; RXON = V_{CC}; MOD = DIV1 = PREGND = GND; T_A = +25°C, unless otherwise noted.)

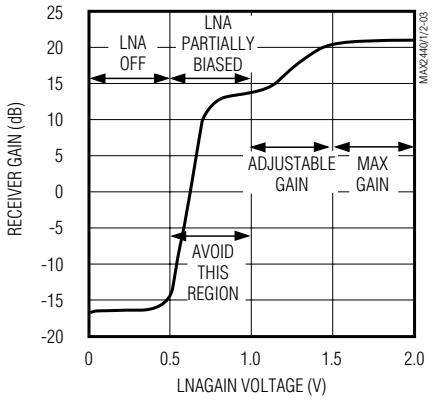
RECEIVER SUPPLY CURRENT vs. TEMPERATURE



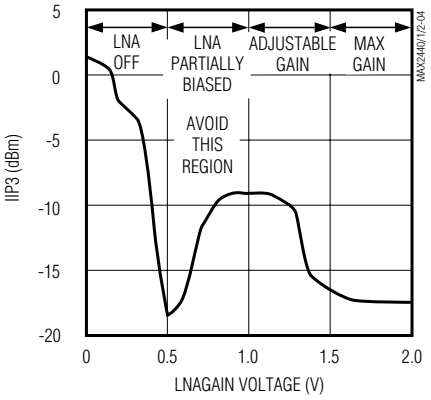
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



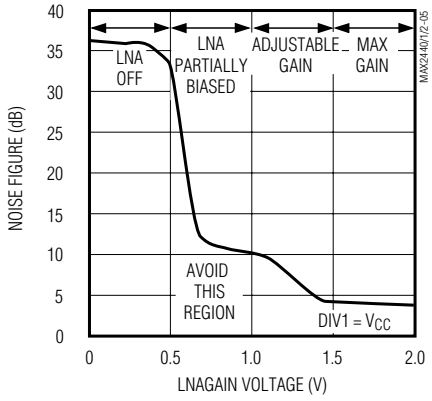
RECEIVER GAIN vs. LNAGAIN



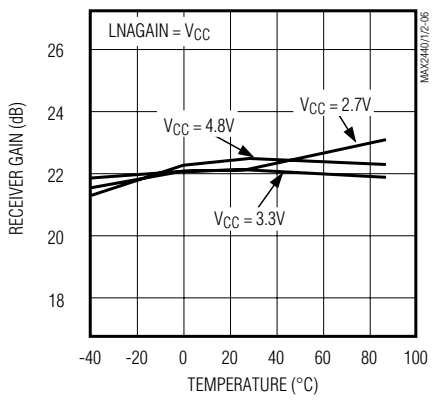
RECEIVER INPUT IP3 vs. $V_{LNAGAIN}$



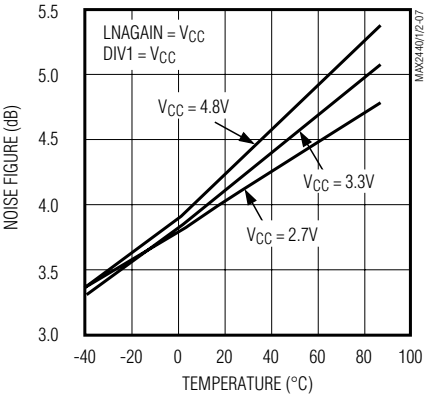
RECEIVER NOISE FIGURE vs. LNAGAIN



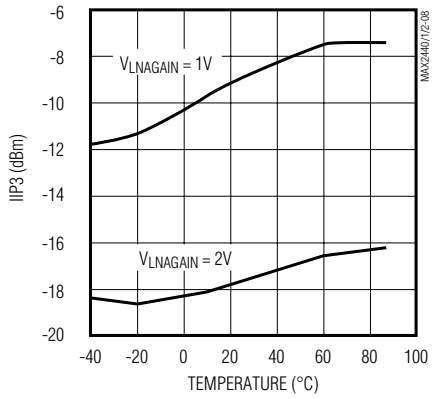
MAX2440 RECEIVER GAIN vs. TEMPERATURE



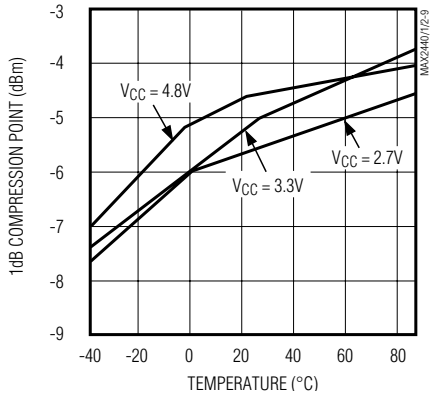
RECEIVER NOISE FIGURE vs. TEMPERATURE AND SUPPLY VOLTAGE



RECEIVER INPUT IP3 vs. TEMPERATURE



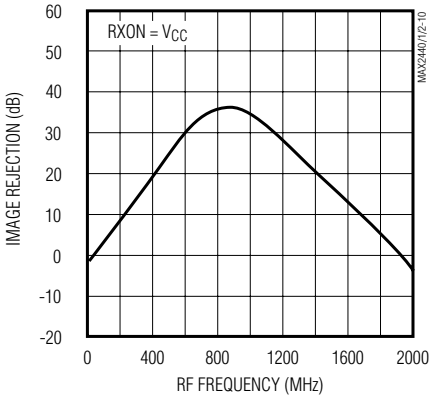
MAX2440 RXOUT 1dB COMPRESSION POINT vs. TEMPERATURE



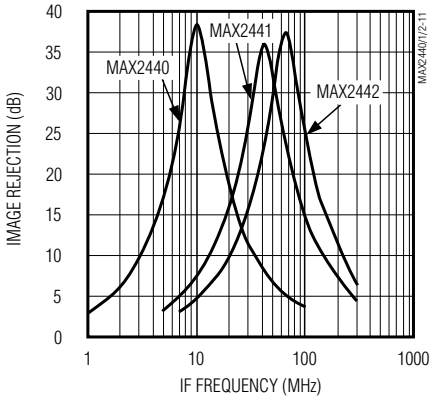
Typical Operating Characteristics (continued)

(MAX242X/MAX246X EV kit, V_{CC} = +3.3V; f_{LO} = 925.7MHz (MAX2440), f_{LO} = 961MHz (MAX2441), f_{LO} = 985MHz (MAX2442), f_{RXIN} = 915MHz; P_{RXIN} = -35dBm; $V_{LNAGAIN}$ = 2V; V_{VCOON} = 2.4V; RXON = V_{CC}; MOD = DIV1 = PREGND = GND; T_A = +25°C, unless otherwise noted.)

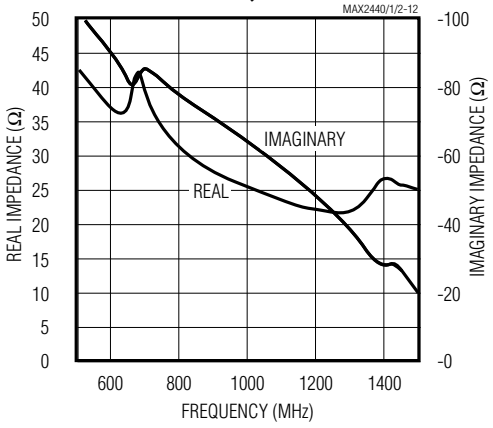
RECEIVER IMAGE REJECTION vs. RF FREQUENCY



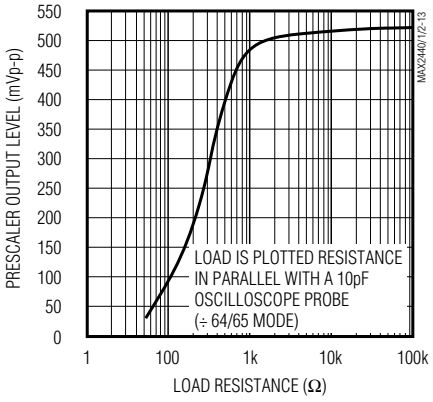
RECEIVER IMAGE REJECTION vs. IF FREQUENCY



RXIN INPUT IMPEDANCE vs. FREQUENCY



PRESCALER OUTPUT LEVEL vs. LOAD RESISTANCE



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Supply-Voltage Input for Master Bias Cell. Bypass with a 47pF low-inductance capacitor and 0.1µF to GND (pin 28 recommended).
2	CAP1	Receive Bias Compensation Pin. Bypass with a 47pF low-inductance capacitor and 0.01µF to GND. Do not make any other connections to this pin.
3	RXOUT	Single-Ended, 330Ω IF Output. AC couple to this pin.
4, 9, 12–15	GND	Ground Connection
5	RXIN	Receiver RF Input, single-ended. The input match shown in Figure 1 maintains an input VSWR of better than 2:1 from 902MHz to 928MHz.
6	V_{CC}	Supply Voltage Input for Receive Low-Noise Amplifier. Bypass with a 47pF low-inductance capacitor to GND (pin 7 recommended).
7	GND	Ground Connection for Receive Low-Noise Amplifier. Connect directly to ground plane using multiple vias.
8	GND	Ground Connection for Signal-Path Blocks, except LNA. Connect directly to ground plane.
10	LNAGAIN	Low-Noise Amplifier Gain-Control Input. Drive this pin high for maximum gain. When LNAGAIN is pulled low, the LNA is capacitively bypassed and the supply current is reduced by 4.5mA. This pin can also be driven with an analog voltage to adjust the LNA gain in intermediate states. Refer to the Receiver Gain vs. LNAGAIN Voltage graph in the *Typical Operating Characteristics,* as well as Table 1.
11	V_{CC}	Supply Voltage Input for Signal-Path Blocks, except LNA. Bypass with a 47pF low-inductance capacitor and 0.01µF to GND (pin 8 recommended).
16	RXON	Driving RXON with a logic high enables the LNA, receive mixer, and IF output buffer. VCOON must also be high.
17	VCOON	Driving VCOON with a logic high turns on the VCO, phase shifters, VCO buffers, and prescaler. The prescaler can be selectively disabled by floating the PREGND pin.
18	DIV1	Driving DIV1 with a logic high disables the divide-by-64/65 prescaler and connects the PREOUT pin directly to an oscillator buffer amplifier, which outputs -8dBm into a 50Ω load. Tie DIV1 low for divide-by-64/65 operation. Pull this pin low when in shutdown to minimize off current.
19	MOD	Modulus Control for the Divide-by-64/65 Prescaler: high = divide-by-64, low = divide-by-65. Note that the DIV1 pin must be at logic low when using the prescaler mode.
20	PREGND	Ground connection for the Prescaler. Tie PREGND to ground for normal operation. Leave floating to disable the prescaler and the output buffer. Tie MOD and DIV1 to ground and leave PREOUT floating when disabling the prescaler.
21	PREOUT	Prescaler/Oscillator Buffer Output. In divide-by-64/65 mode (DIV1 = low), the output level is 500mVp-p into a high-impedance load. In divide-by-1 mode (DIV1 = high), this output delivers -8dBm into a 50Ω load. AC couple to this pin.
22	V_{CC}	Supply-Voltage Input for Prescaler. Bypass with a 47pF low-inductance capacitor and 0.01µF to GND (pin 20 recommended).
23	V_{CC}	Supply-Voltage Input for VCO and Phase Shifters. Bypass with a 47pF low-inductance capacitor to GND (pin 26 recommended).
24	$\overline{TANK}$	Differential Oscillator Tank Port. See *Applications Information* for information on tank circuits or on using an external oscillator.
25	TANK	Differential Oscillator Tank Port. See *Applications Information* for information on tank circuits or on using an external oscillator.

Pin Description (continued)

PIN	NAME	FUNCTION
26	GND	Ground Connection for VCO and Phase Shifters
27	GND	Ground (substrate)
28	GND	Ground Connection for Master Bias Cell

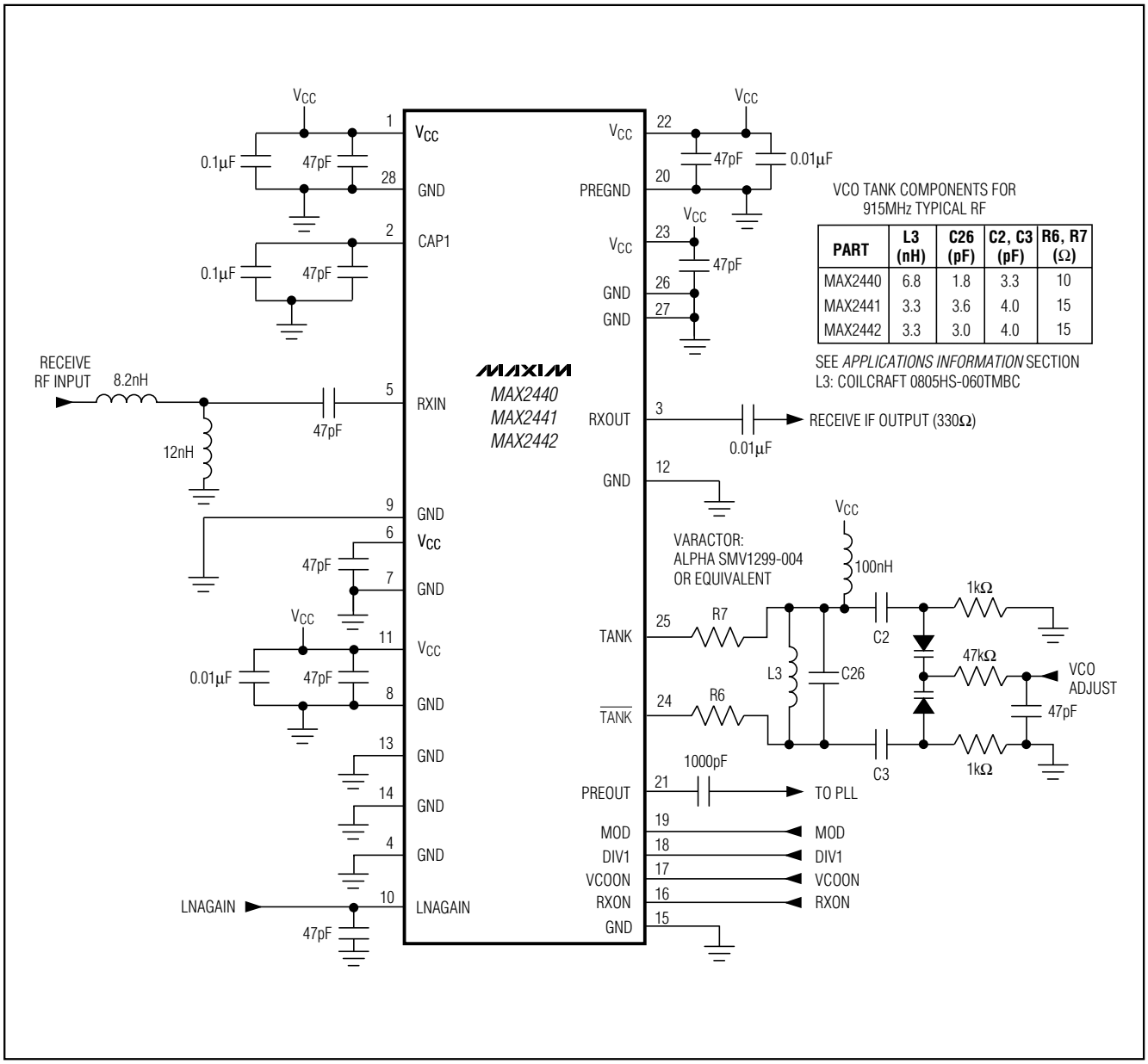


Figure 1. Typical Operating Circuit

Detailed Description

The following sections describe each of the blocks shown in the *Functional Diagram.*

Receiver

The MAX2440/MAX2441/MAX2442's receive path consists of a 900MHz low-noise amplifier, an image-reject mixer, and an IF buffer amplifier.

The LNA's gain and biasing are adjustable via the LNAGAIN pin. Proper operation of this pin can provide optimum performance over a wide range of signal levels. The LNA can be placed in four modes by applying a DC voltage on the LNAGAIN pin. See Table 1, as well as the relevant *Typical Operating Characteristics* plots.

At low LNAGAIN voltages, the LNA is shut off, and the input signal capacitively couples directly into the mixer to provide maximum linearity for large-signal operation (receiver close to transmitter). As the LNAGAIN voltage is raised, the LNA begins to turn on. Between 0.5V and 1V at LNAGAIN, the LNA is partially biased and behaves like a Class C amplifier. Avoid this operating mode for applications where linearity is a concern. As the LNAGAIN voltage reaches 1V, the LNA is fully biased into Class A mode, and the gain is monotonically adjustable at LNAGAIN voltages above 1V. See the Receiver Gain, Receiver IP3, and Receiver Noise Figure vs. LNAGAIN plots in the *Typical Operating Characteristics* for more information.

The downconverter is implemented using an image-reject mixer consisting of an input buffer with two outputs, each of which is fed to a double-balanced mixer. The local-oscillator (LO) port of each mixer is driven from a quadrature LO. The LO is generated from an on-chip oscillator and an external tank circuit. Its signal is buffered and split into phase shifters, which provide 90° of phase shift across their outputs. This pair of LO signals is fed to the mixers. The mixers' outputs are then passed through a second pair of phase shifters, which provide a 90° phase shift across their outputs. The resulting mixer outputs are then summed together. The final phase relationship is such that the desired signal is reinforced and the image signal is canceled. The downconverter mixer output appears on the RXOUT pin, a single-ended 330Ω output.

Table 1. LNA Modes

LNAGAIN VOLTAGE (V)	MODE
0 < V ≤ 0.5	LNA capacitively bypassed, minimum gain, maximum IP3
0.5 < V < 1.0	LNA partially biased. **Avoid this mode**—the LNA operates in a Class C manner
1.0 < V ≤ 1.5	LNA gain is monotonically adjustable
1.5 < V ≤ V_{CC}	LNA at maximum gain (remains monotonic)

Phase Shifters

MAX2440/MAX2441/MAX2442 devices use passive networks to provide quadrature phase shifting for the receive IF and LO signals. Because these networks are frequency selective, proper part selection is important. Image rejection degrades as the IF and RF move away from the designed optimum frequencies. Refer to the *Selector Guide* on the front page of this data sheet.

Local Oscillator (LO)

The on-chip LO is formed by an emitter-coupled differential pair. An external LC resonant tank sets the oscillation frequency. A varactor diode is typically used to create a voltage-controlled oscillator (VCO). See the *Applications Information* section and Figure 2 for an example VCO tank circuit.

The LO may be overdriven in applications where an external signal is available. The external LO signal should be about 0dBm from 50Ω, and should be AC coupled into either the TANK or $\overline{TANK}$ pin. Both TANK and $\overline{TANK}$ require pull-up resistors to V_{CC}. See the *Applications Information* section and Figure 3 for details.

The local oscillator resists LO pulling caused by changes in load impedance that occur as the part is switched from standby mode. The amount of LO pulling will be affected if there is power at the RXIN port due to imperfect isolation in an external transmit/receive (T/R) switch.

Prescaler

The on-chip prescaler can be used in two different modes: as a dual-modulus divide-by-64/65, or as oscillator buffer amplifier. The DIV1 pin controls this function. When DIV1 is low, the prescaler is in dual-modulus divide-by-64/65 mode; when it is high, the prescaler is disabled and the oscillator buffer amplifier is enabled. The buffer typically outputs -8dBm into a 50Ω load. To minimize shutdown supply current, pull the DIV1 pin low when in shutdown mode.

In divide-by-64/65 mode, the division ratio is controlled by the MOD pin. When MOD is high, the prescaler is in divide-by-64 mode; when it is low, it divides the LO frequency by 65. The DIV1 pin must be at a logic low in this mode.

To disable the prescaler entirely, leave PREGND and PREOUT floating. Also tie the MOD and DIV1 pins to GND. Disabling the prescaler does not affect operation of the VCO stage.

Power Management

MAX2440/MAX2441/MAX2442 supports three different power-management features to conserve battery life. The VCO section has its own control pin (VCOON), which also serves as a master bias pin. When VCOON is high, the LO, quadrature LO phase shifters, and prescaler or LO buffer are all enabled. The VCO can be powered up prior to receiving to allow it to stabilize. With VCOON high, bringing RXON high enables the receive path, which consists of the LNA, image-reject mixers, and IF output buffer. When this pin is low, the receive path is inactive.

To disable all chip functions and reduce the supply current to typically less than 0.5µA, pull VCOON, DIV1, MOD, and RXON low.

Applications Information

Oscillator Tank

The on-chip oscillator requires a parallel-resonant tank circuit connected across TANK and $\overline{TANK}$. Figure 2 shows an example of an oscillator tank circuit. Inductor L4 provides DC bias to the tank ports. Inductor L3, capacitor C26, and the series combination of capacitors C2, C3, and both halves of the varactor diode capacitance set the resonant frequency, as follows:

$$f_r = \frac{1}{2\pi\sqrt{(L3)(C_{EFF})}}$$

$$C_{EFF} = \frac{1}{\left(\frac{1}{C2}+\frac{1}{C3}+\frac{2}{C_{D1}}\right)} + C26$$

where C_{D1} is the capacitance of one varactor diode.

Choose tank components according to your application needs, such as phase-noise requirements, tuning range, and VCO gain. High-Q inductors, such as air-core micro springs, yield low phase noise. Use a low-tolerance inductor (L3) for predictable oscillation frequency. Resistors R6 and R7 can be chosen from 0 to 20Ω to reduce the Q of parasitic resonance due to series package inductance (L_T). Keep R6 and R7 as small as possible to minimize phase noise, yet large enough to ensure oscillator start-up in fundamental mode. Oscillator start-up will be most critical with high tuning bandwidth (low tank Q) and high temperature. Capacitors C2 and C3 couple in the varactor. Light coupling of the varactor is a way to reduce the effects of high varactor tolerance and increase loaded Q. For a wider tuning range; use larger values for C2 and C3 or a varactor with a large capacitance ratio. Capacitor C26 is used to trim the tank oscillator frequency. Larger values for C26 will help negate the effect of stray PCB capacitance and parasitic inductor capacitance (L3). Choose a low tolerance capacitor for C26.

For applications that require a wide tuning range and low phase noise, a series coupled resonant tank may be required, as shown in Figure 4. This tank will use the package inductance in series with inductors L1, L2, and capacitance of varactor D1 to set the net equivalent inductance which resonates in parallel with the internal oscillator capacitance. Inductors L1 and L2 may be implemented as microstrip inductors, saving component cost. Bias is provided to the tank port through chokes L3 and L5. R1 and R3 should be chosen large enough to de-Q the parasitic resonance due to L3 and L5, but small enough to minimize the voltage drop across them due to bias current. Values for R1 and R3 should be kept between 0Ω and 50Ω. Proper high-frequency bypassing (C1) should be used for the bias voltage to eliminate power-supply noise from entering the tank.

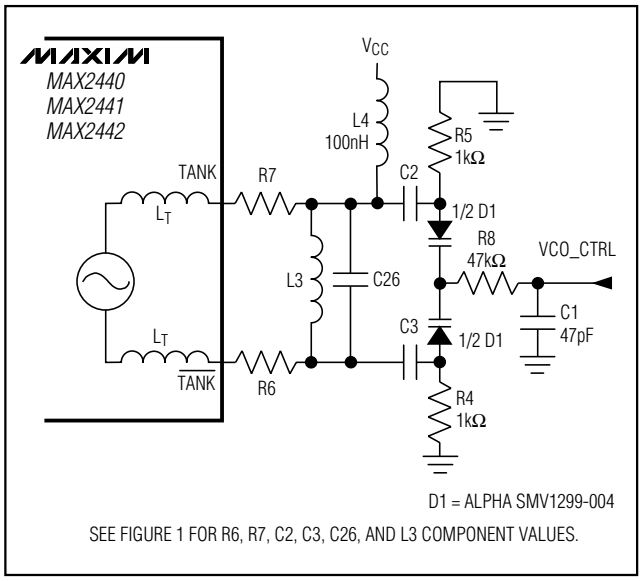


Figure 2. Oscillator Tank Schematic, Using the On-Chip VCO

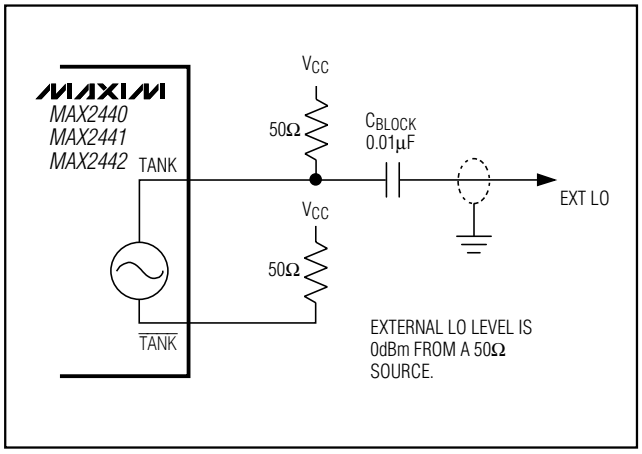


Figure 3. Using an External Local Oscillator

Oscillator-Tank PC Board Layout

The parasitic PC board capacitance, as well as PCB trace inductance and package inductance, can affect oscillation frequency, so be careful in laying out the PC board for the oscillator tank. Keep the tank layout as symmetrical, tightly packed, and close to the device as possible to minimize LO feedthrough. When using a PC board with a ground plane, a cut-out in the ground plane (and any other planes) below the oscillator tank will reduce parasitic capacitance.

Using an External Oscillator

If an external 50Ω LO signal source is available, it can be used as an input to the TANK or $\overline{TANK}$ pin in place of the on-chip oscillator (Figure 3). The oscillator signal is AC coupled into the TANK pin and should have a level of about 0dBm from a 50Ω source. For proper biasing of the oscillator input stage, TANK and $\overline{TANK}$ must be pulled up to the V_{CC} supply via 50Ω resistors.

If a differential LO source such as the MAX2620 is available, AC couple the inverting output into $\overline{TANK}$.

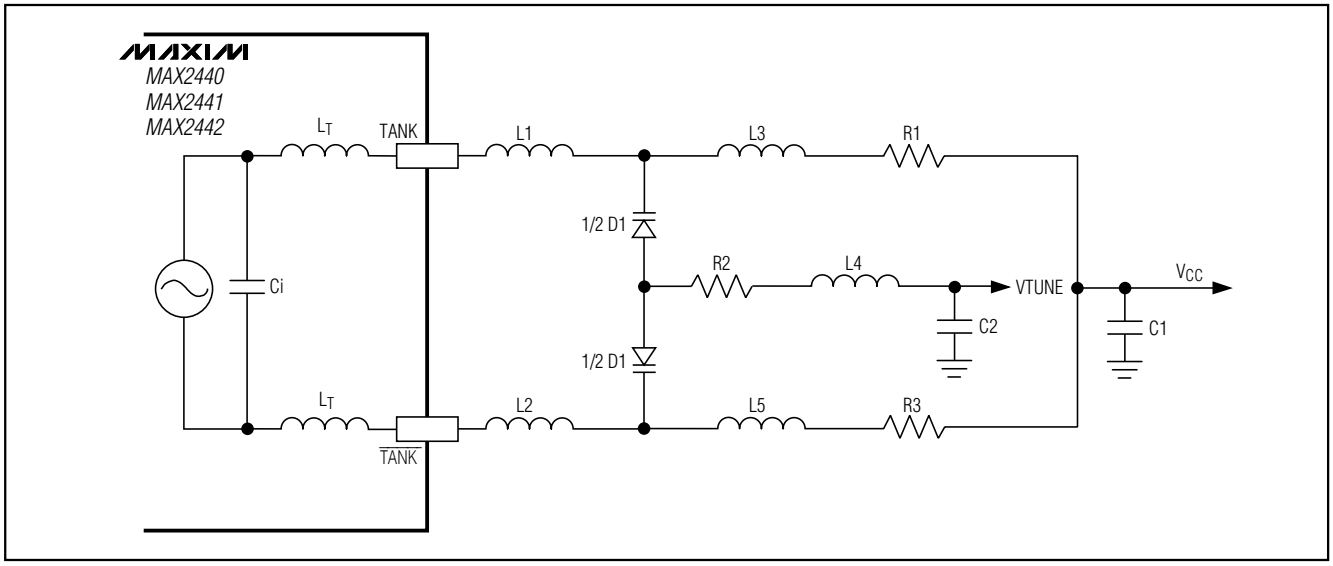


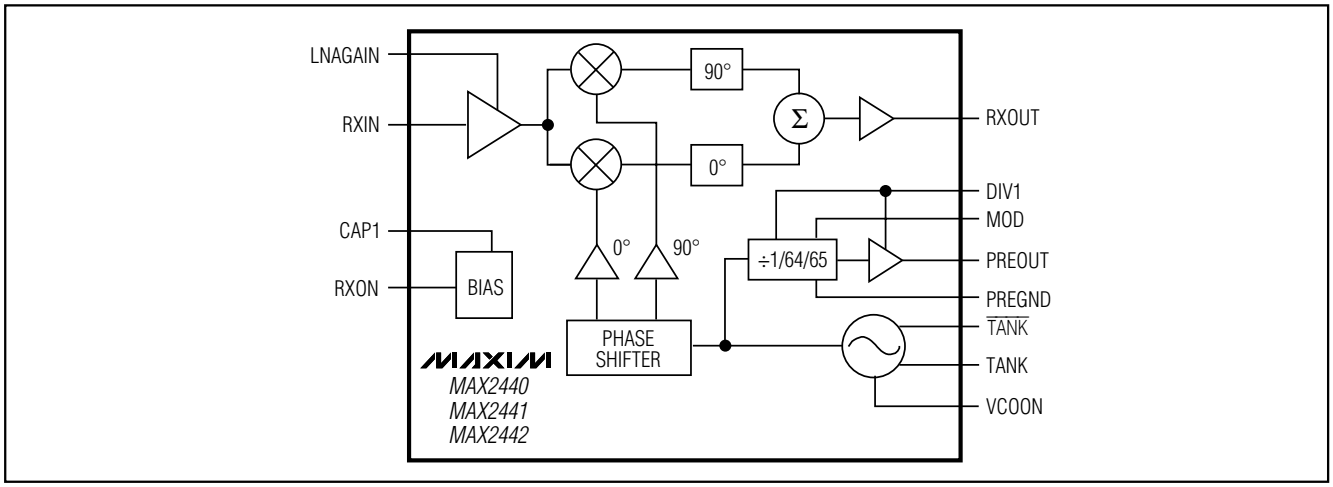
Figure 4. Series Coupled Resonant Tank for Wide Tuning Range and Low Phase Noise

Chip Information

TRANSISTOR COUNT: 2802

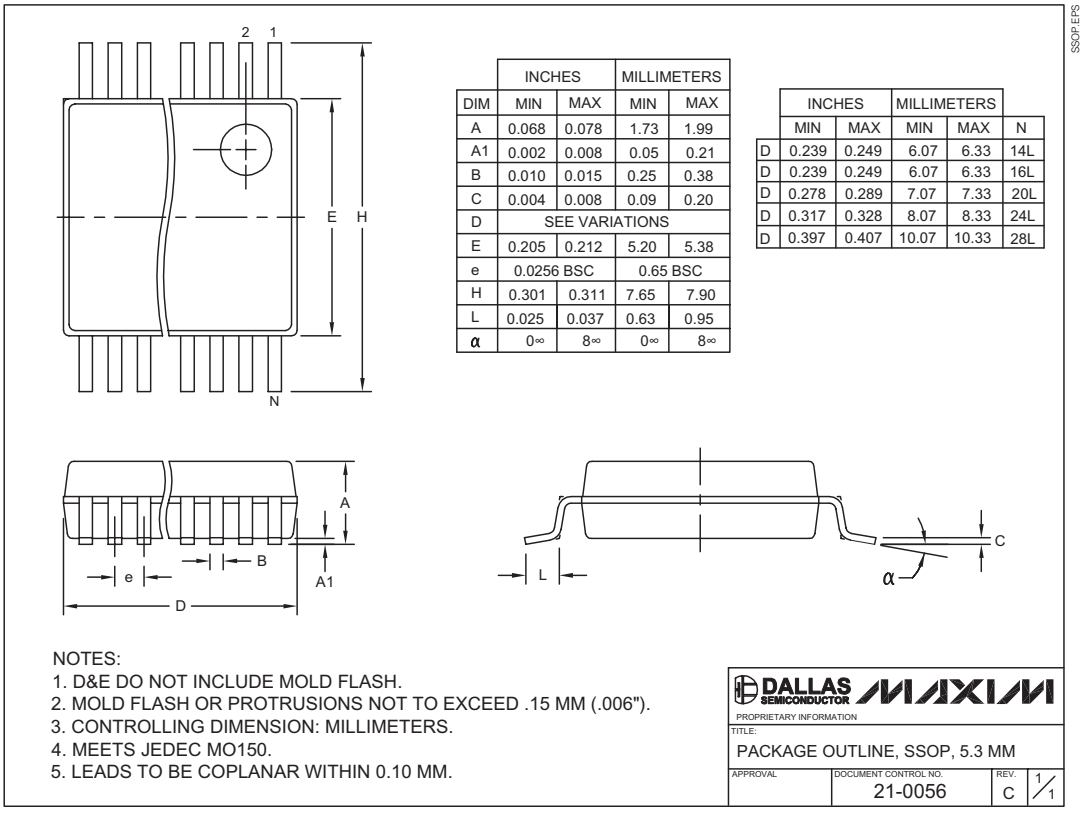
900MHz Image-Reject Receivers

Functional Diagram



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0056 | REV. C | 1/1

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