

SN54HCT374, SN74HCT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS005D – MARCH 1984 – REVISED AUGUST 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 22$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Eight D-Type Flip-Flops in a Single Package
- Full Parallel Access for Loading

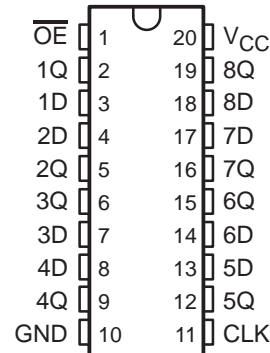
description/ordering information

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

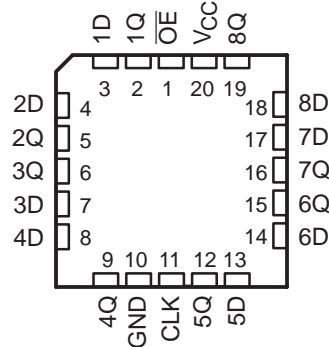
The eight flip-flops of the 'HCT374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

An output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

SN54HCT374 . . . J OR W PACKAGE
SN74HCT374 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT374 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 20 | SN74HCT374N | SN74HCT374N |
| | SOIC – DW | Tube of 25 | SN74HCT374DW | HCT374 |
| | | Reel of 2000 | SN74HCT374DWR | |
| | SOP – NS | Reel of 2000 | SN74HCT374NSR | HCT374 |
| | SSOP – DB | Reel of 2000 | SN74HCT374DBR | HT374 |
| | TSSOP – PW | Tube of 70 | SN74HCT374PW | HT374 |
| Reel of 2000 | | SN74HCT374PWR | | |
| Reel of 250 | | SN74HCT374PWT | | |
| -55°C to 125°C | CDIP – J | Tube of 20 | SNJ54HCT374J | SNJ54HCT374J |
| | CFP – W | Tube of 85 | SNJ54HCT374W | SNJ54HCT374W |
| | LCCC – FK | Tube of 55 | SNJ54HCT374FK | SNJ54HCT374FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HCT374, SN74HCT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS005D – MARCH 1984 – REVISED AUGUST 2003

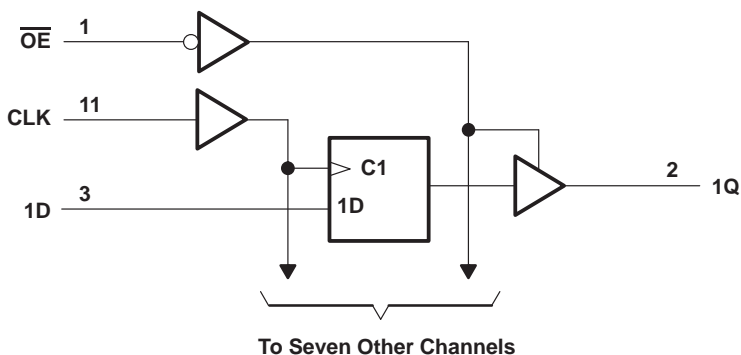
description/ordering information (continued)

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 35 mA |
| Continuous current through V_{CC} or GND | ± 70 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| DB package | 70°C/W |
| DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HCT374, SN74HCT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS005D – MARCH 1984 – REVISED AUGUST 2003

recommended operating conditions (see Note 3)

| | | SN54HCT374 | | | SN74HCT374 | | | UNIT |
|-----------------|---------------------------------|----------------------------------|-----------------|-----|------------|-----------------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 4.5 V to 5.5 V | | 2 | 2 | | | V |
| V _{IL} | Low-level input voltage | V _{CC} = 4.5 V to 5.5 V | | 0.8 | | 0.8 | | V |
| V _I | Input voltage | 0 | V _{CC} | | 0 | V _{CC} | | V |
| V _O | Output voltage | 0 | V _{CC} | | 0 | V _{CC} | | V |
| Δt/Δv | Input transition rise/fall time | 500 | | | 500 | | | ns |
| T _A | Operating free-air temperature | -55 | 125 | | -40 | 85 | | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HCT374 | | SN74HCT374 | | UNIT |
|--------------------|--|--------------------------|-------------------|-----------------------|-------|-------|------------|-------|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | V | |
| | | I _{OH} = -6 mA | | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 4.5 V | | | 0.001 | 0.1 | | 0.1 | V | |
| | | I _{OL} = 6 mA | | | | 0.17 | 0.26 | | 0.4 | | 0.33 |
| I _I | V _I = V _{CC} or 0 | | 5.5 V | ±0.1 | ±100 | | | ±1000 | ±1000 | nA | |
| I _{OZ} | V _O = V _{CC} or 0 | | 5.5 V | ±0.01 | ±0.5 | | | ±10 | ±5 | μA | |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 5.5 V | | | 8 | | 160 | 80 | μA | |
| ΔI _{CC} † | One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC} | | 5.5 V | | 1.4 | 2.4 | | 3 | 2.9 | mA | |
| C _i | | | 4.5 V to 5.5 V | | 3 | 10 | | 10 | 10 | pF | |

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HCT374 | | SN74HCT374 | | UNIT |
|--------------------|---------------------------------|-----------------|-----------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 4.5 V | 31 | | 21 | | 25 | | MHz |
| | | 5.5 V | 36 | | 23 | | 28 | | |
| t _w | Pulse duration, CLK high or low | 4.5 V | 16 | | 24 | | 20 | | ns |
| | | 5.5 V | 14 | | 22 | | 18 | | |
| t _{su} | Setup time, data before CLK↑ | 4.5 V | 20 | | 30 | | 25 | | ns |
| | | 5.5 V | 17 | | 27 | | 23 | | |
| t _h | Hold time, data after CLK↑ | 4.5 V | 10 | | 10 | | 10 | | ns |
| | | 5.5 V | 10 | | 10 | | 10 | | |



SN54HCT374, SN74HCT374
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCLS005D – MARCH 1984 – REVISED AUGUST 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HCT374 | | SN74HCT374 | | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 4.5 V | 31 | 36 | | 21 | | 25 | MHz | |
| | | | 5.5 V | 36 | 40 | | 23 | | 28 | | |
| t_{pd} | CLK | Any Q | 4.5 V | | 30 | 36 | | 54 | | 45 | ns |
| | | | 5.5 V | | 25 | 32 | | 49 | | 41 | |
| t_{en} | \overline{OE} | Any Q | 4.5 V | | 26 | 30 | | 45 | | 38 | ns |
| | | | 5.5 V | | 23 | 27 | | 41 | | 34 | |
| t_{dis} | \overline{OE} | Any Q | 4.5 V | | 23 | 30 | | 45 | | 38 | ns |
| | | | 5.5 V | | 22 | 27 | | 41 | | 34 | |
| t_t | | Any Q | 4.5 V | | 10 | 12 | | 18 | | 15 | ns |
| | | | 5.5 V | | 9 | 11 | | 16 | | 14 | |

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HCT374 | | SN74HCT374 | | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | CLK | Any Q | 4.5 V | | 40 | 46 | | 69 | | 58 | ns |
| | | | 5.5 V | | 35 | 41 | | 62 | | 52 | |
| t_{en} | \overline{OE} | Any Q | 4.5 V | | 34 | 40 | | 60 | | 50 | ns |
| | | | 5.5 V | | 29 | 36 | | 54 | | 45 | |
| t_t | | Any Q | 4.5 V | | 18 | 42 | | 63 | | 53 | ns |
| | | | 5.5 V | | 16 | 38 | | 57 | | 48 | |

operating characteristics, $T_A = 25^\circ\text{C}$

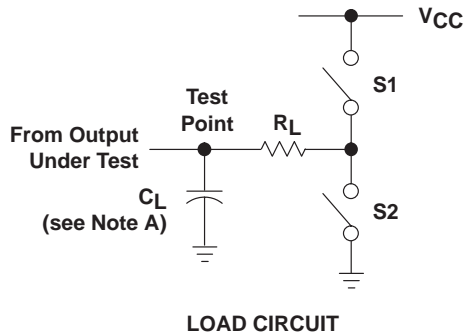
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance per flip-flop | No load | 85 | pF |



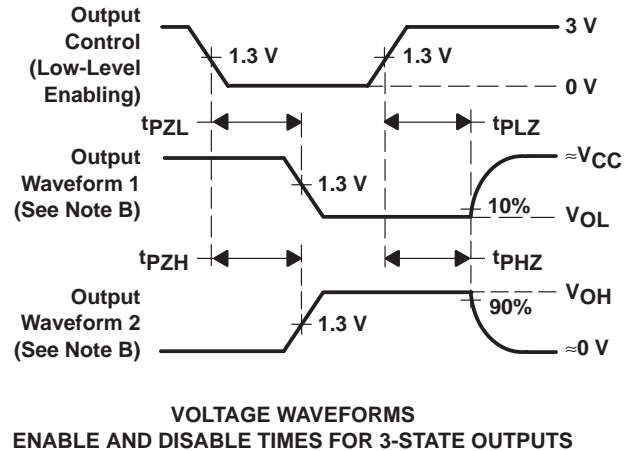
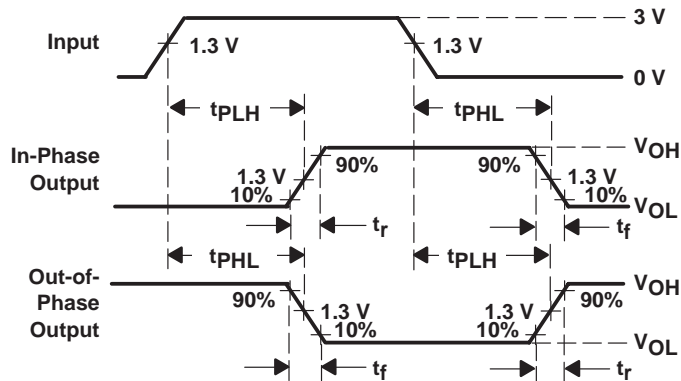
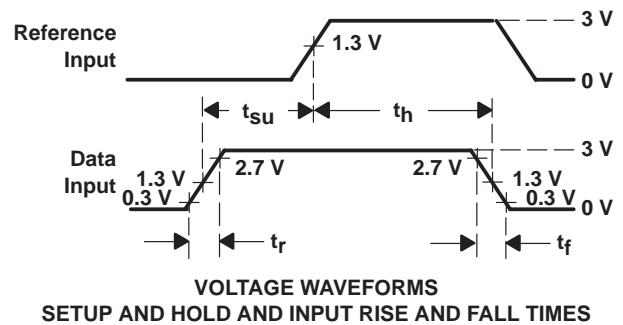
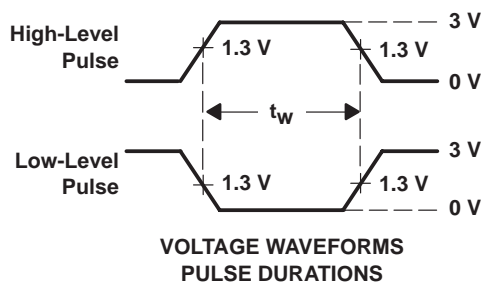
SN54HCT374, SN74HCT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS005D – MARCH 1984 – REVISED AUGUST 2003

PARAMETER MEASUREMENT INFORMATION



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | -- | 50 pF or 150 pF | Open | Open |



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - t_{pZL} and t_{pZH} are the same as t_{en} .
 - t_{pLH} and t_{pHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| 5962-8550701VRA | ACTIVE | CDIP | J | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| 5962-8550701VSA | ACTIVE | CFP | W | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| 85507012A | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| 8550701RA | ACTIVE | CDIP | J | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/65652BRA | ACTIVE | CDIP | J | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SN54HCT374J | ACTIVE | CDIP | J | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SN74HCT374DBR | ACTIVE | SSOP | DB | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HCT374DW | ACTIVE | SOIC | DW | 20 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HCT374DWR | ACTIVE | SOIC | DW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HCT374N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74HCT374N3 | OBSOLETE | PDIP | N | 20 | | None | Call TI | Call TI |
| SN74HCT374NSR | ACTIVE | SO | NS | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HCT374PW | ACTIVE | TSSOP | PW | 20 | 70 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HCT374PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HCT374PWT | ACTIVE | TSSOP | PW | 20 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SNJ54HCT374FK | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54HCT374J | ACTIVE | CDIP | J | 20 | 1 | None | Call TI | Level-NC-NC-NC |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| Products | | Applications | |
|------------------|--|---------------------|--|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265