CD54HC688, CD74HC688, CD54HCT688, CD74HCT688

Data sheet acquired from Harris Semiconductor
SCHS196C

High-Speed CMOS Logic 8-Bit Magnitude Comparator

September 1997 - Revised August 2003

Features

- **Cascadable**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{o}C to 125^{o}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The ’HC688 and ’HCT688 are 8-bit magnitude comparators designed for use in computer and logic applications that require the comparison of two 8-bit binary words. When the compared words are equal the output (Y) is low and can be used as the enabling input for the next device in a cascaded application.

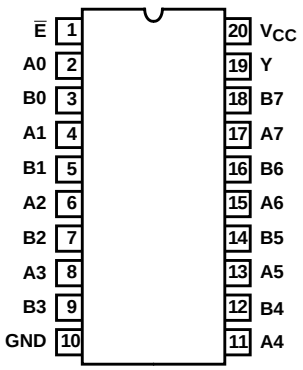
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD54HC688F3A	-55 to 125	20 Ld CERDIP
CD54HCT688F3A	-55 to 125	20 Ld CERDIP
CD74HC688E	-55 to 125	20 Ld PDIP
CD74HC688M	-55 to 125	20 Ld SOIC
CD74HC688M96	-55 to 125	20 Ld SOIC
CD74HC688NSR	-55 to 125	20 Ld SOP
CD74HC688PWR	-55 to 125	20 Ld TSSOP
CD74HC688PWT	-55 to 125	20 Ld TSSOP
CD74HCT688E	-55 to 125	20 Ld PDIP
CD74HCT688M	-55 to 125	20 Ld SOIC
CD74HCT688M96	-55 to 125	20 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC688, CD54HCT688 (CERDIP)
CD74HC688 (PDIP, SOIC, SOP, TSSOP)
CD74HCT688 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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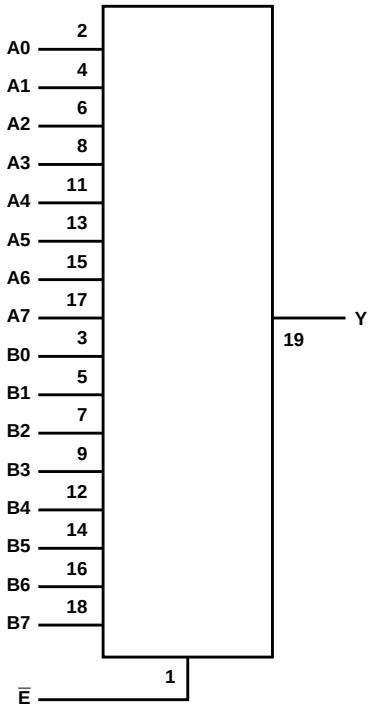
Functional Diagram

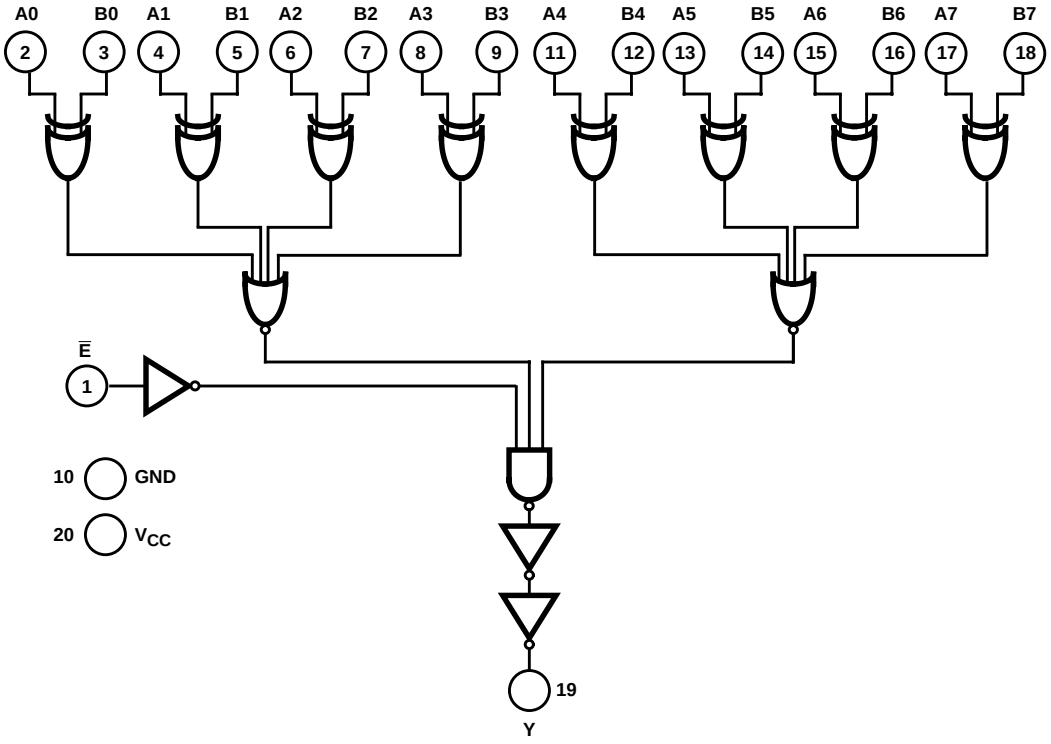


TRUTH TABLE

INPUTS		OUPUTS
A, B	**$\overline{E}$**	**Y**
A = B	L	L
A ≠ B	L	H
X	H	H

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

Logic Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	69
M (SOIC) Package	58
NSR (SOP) Package	60
PW (TSSOP) Package	83

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
Enable	0.7
Data Inputs	0.35

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay (Figure 1) An to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	170	-	210	-	255	ns
			4.5	-	-	34	-	42	-	51	ns
		C_L =15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	29	-	36	-	43	ns
Bn to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	170	-	210	-	255	ns
			4.5	-	-	34	-	42	-	51	ns
		C_L =15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	29	-	36	-	43	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{E}$ to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	120	-	150	-	180	ns
			4.5	-	-	24	-	30	-	36	ns
		C_L =15pF	5	-	9	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	20	-	26	-	30	ns
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	C_L =15pF	5	-	22	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay (Figure 1)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	34	-	42	-	51	ns
An to Output		C_L =15pF	5	-	14	-	-	-	-	-	ns
Bn to Output	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	34	-	42	-	51	ns
		C_L =15pF	5	-	14	-	-	-	-	-	ns
$\overline{E}$ to Output	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	24	-	30	-	36	ns
		C_L =15pF	5	-	9	-	-	-	-	-	ns
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	C_L =15pF	5	-	22	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per gate.
4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuit and Waveform

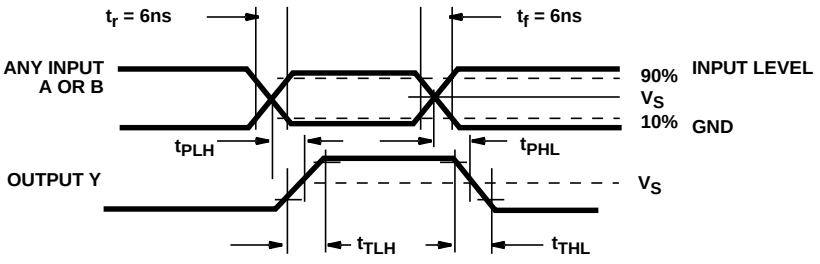


FIGURE 1. PROPAGATION DELAY AMD TRANSITION TIMES

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-8685701RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54HC688F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54HCT688F	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54HCT688F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD74HC688E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC688M	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74HC688M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74HC688NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74HC688PWR	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD74HC688PWT	ACTIVE	TSSOP	PW	20	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD74HCT688E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT688M	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74HCT688M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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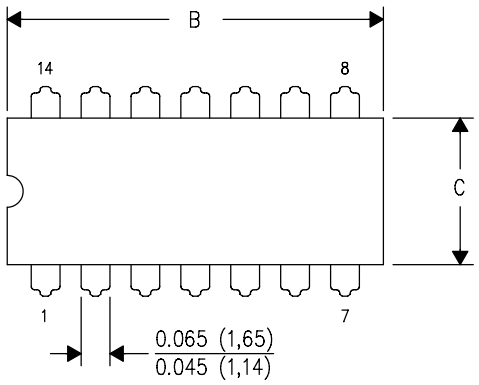
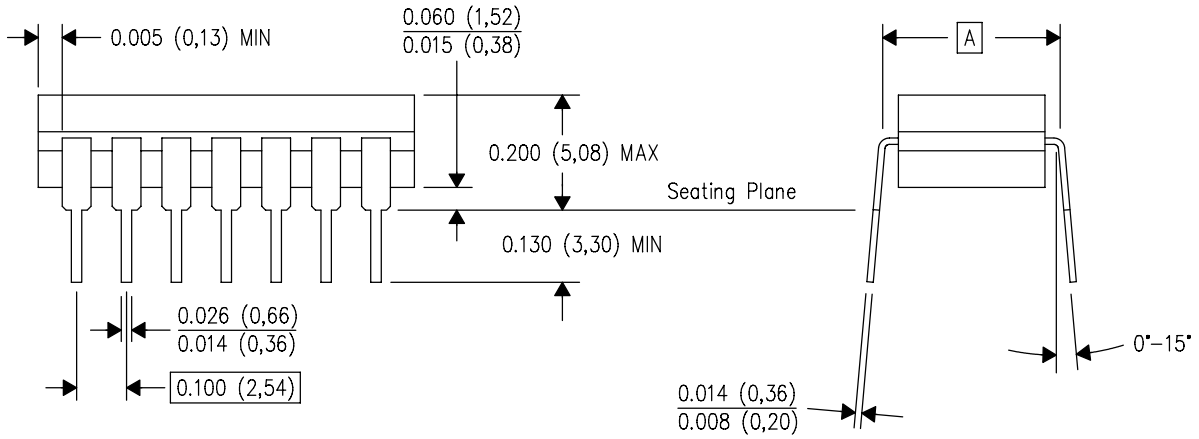
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



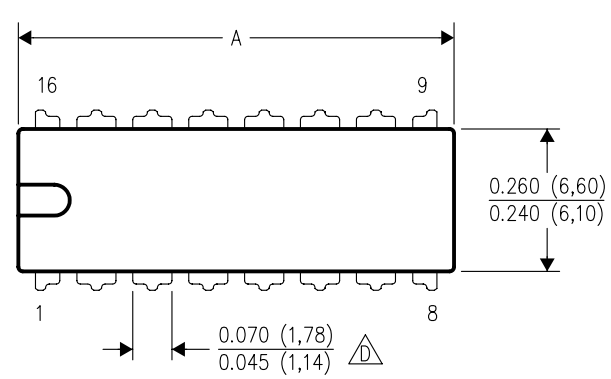
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

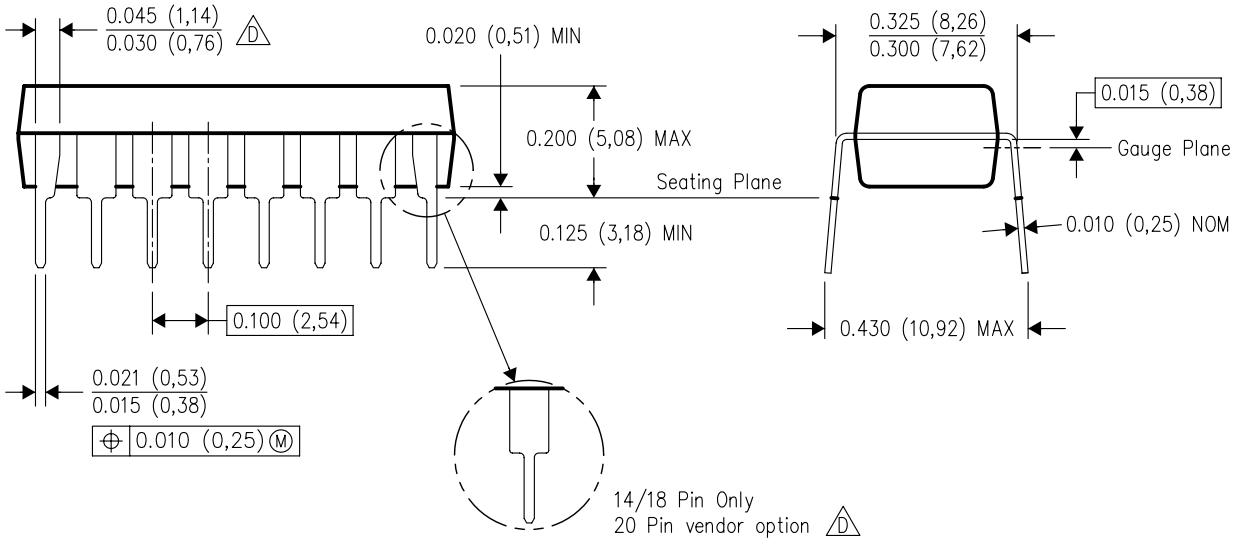
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



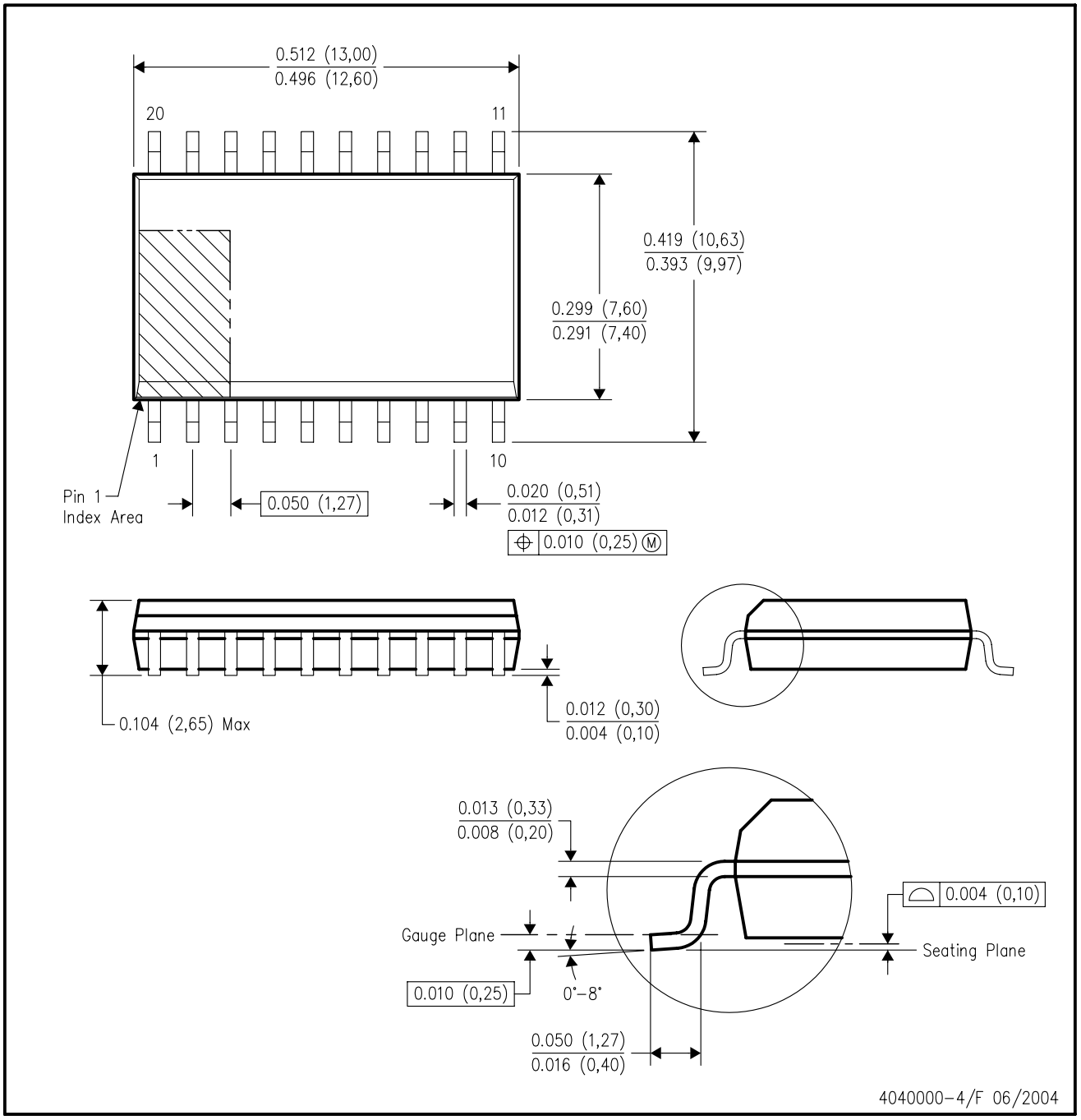
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

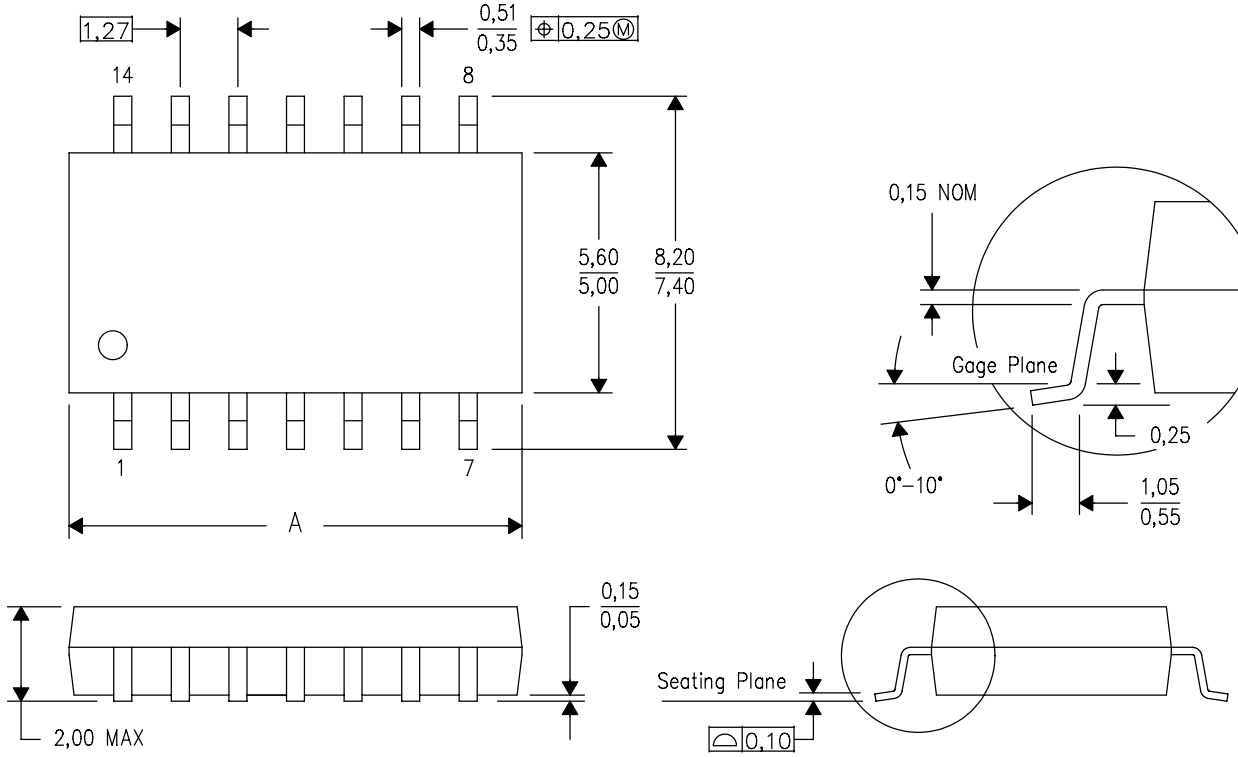


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



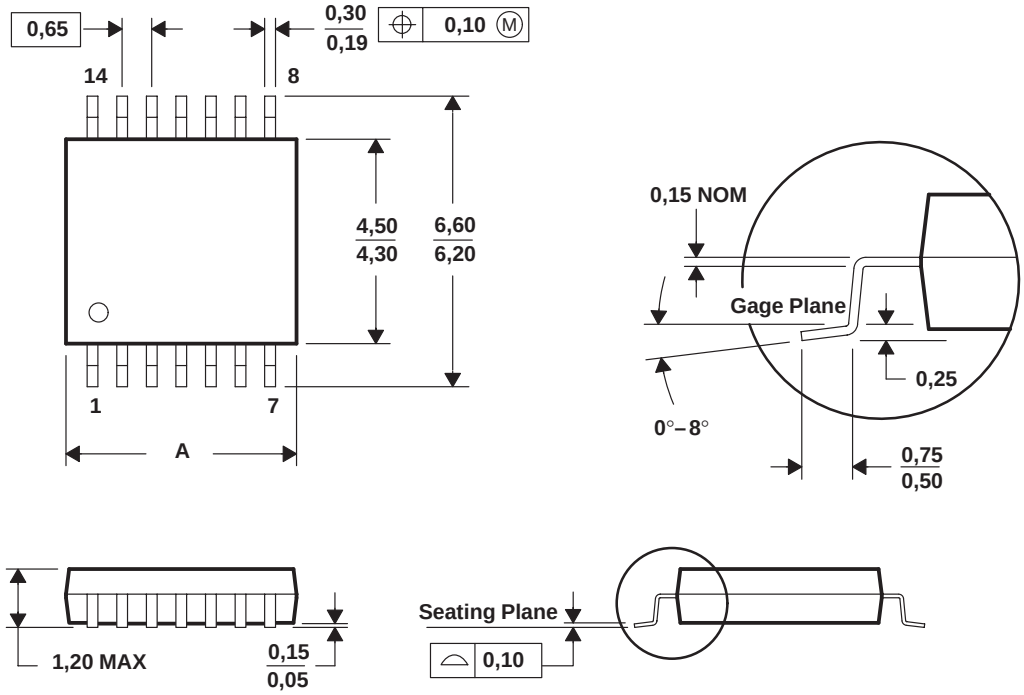
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
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